A Comparative Study of Tunneling FETs Based on Graphene and GNR Heterostructures

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***Abstract*— In this paper, for the first time device characteristics of field-effect tunneling transistors based on vertical graphene-hBN heterostructure (VTGFET) and vertical graphene nanoribbon (GNR)-hBN heterostructure (VTGNRFET) are theoretically investigated and compared. An atomistic simulation based on the nonequilibrium Green's function (NEGF) formalism is employed. The results indicate that due to the presence of an energy gap in GNRs, the I_{ON}/I_{OFF} ratio of VTGNRFET can be much larger than that of VTGFET, which renders VTGNRFETs as promising candidates for future electronic applications. Furthermore, it can be inferred from the results that due to smaller density of states and as a result smaller quantum capacitance of GNRs in comparison with that of graphene, better switching and frequency response can be achieved for VTGNRFETs.**

***Index Terms*— Graphene, graphene heterostructures, graphene nanoribbon (GNR), nonequilibrium Green's function (NEGF), tunneling transistors.**

I. Introduction

OVER the past decade graphene has been widely studied due to the excellent electronic, optical, and mechanical properties [1]. Monolayer and bilayer graphene have been utilized as the channel material for field-effect transistors (FETs) [2], where the monolayer nature of graphene results in excellent gate control over the channel. The application of graphene FETs (GFETs) for digital applications, however, is limited due to the absence of an energy bandgap. The largest achieved I_{ON}/I_{OFF} ratio for GFETs is smaller than 10 [3] which is not sufficient for digital applications.

Some possible methods for inducing an energy gap in graphene include patterning graphene into nanoribbons (GNRs), with I_{ON}/I_{OFF} ratios up to 10^6 for ribbons narrower than 5 nm [4], and the use of bilayer graphene with a transverse electric field [5]. However, the performance of GNRFETs is limited due to the undesirable effect of line-edge disorder [6], [7]. On the other hand to induce a reasonable bandgap of about 250 meV in bilayer graphene, one needs to apply an extremely large transverse electric field of about 3×10^7 V/cm [5], [8], which is difficult to achieve in integrated circuits.

Fundamental problems of conventional GFETs have motivated researchers to focus on new structures such as tunneling FETs. In these structures tunneling between source and drain is controlled by the gate-source voltage. In comparison with conventional FETs, tunneling FETs have some advantages such as having subthreshold swings smaller than 60 mV/dec and higher I_{ON}/I_{OFF} ratios [9]–[11].

Graphene-based heterostructures such as graphene-hexagonal boron nitride (hBN) have attracted the attention of scientists [12]–[15]. Recently, a graphene tunneling FET based on a vertical graphene heterostructure has been proposed [16]. In this structure source and drain are composed of a monolayer of graphene and hBN or MoS_2 are used as a tunneling barrier [16]. Vertical graphene-hBN heterostructures (VTGFETs) exhibit room-temperature switching ratios of $\approx$50 and $\approx$10 000 for hBN and MoS_2, respectively [16]. The operation of this device is based on the voltage tunability of the density of states (DOS) in graphene and of the effective height of the tunneling barrier [16]. Using WS_2 as a tunneling barrier leads to a flexible and transparent device which provides the possibility of switching between tunneling and thermionic transport regime and yield a relatively high I_{ON}/I_{OFF} ratio of about (10^6) and a much larger I_{ON} than their counterparts [17].

In this paper, the device characteristics of tunneling FETs based on a vertical graphene nanoribbon (GNR)-hBN heterostructure (VTGNRFET) are studied and benchmarked against VTGFET. The dependencies of device characteristics and I_{ON}/I_{OFF} ratio on the geometrical parameters are investigated and discussed. Furthermore, the subthreshold swing, cutoff frequency and intrinsic gate-delay time of VTGFET and VTGNRFET structures are also studied. This paper is organized as follows: after a brief introduction in Section I, the device structure and the operational principle are explained in Section II. In Section III, the models are described. The results are discussed in Section IV and concluding remarks are presented in Section V.

II. Device Operation Principle

The sketch of a VTGFET/VTGNRFET is shown in Fig. 1(a) where the source and drain contacts are made from monolayers of graphene/GNR. A few layers of hBN (three to seven layers) serve as the tunneling barrier between the source and drain

Manuscript received June 10, 2013; revised November 13, 2013; accepted November 14, 2013. Date of publication December 3, 2013; date of current version December 20, 2013. This work was partly supported by the Iran National Science Foundation. The review of this paper was arranged by Editor R. K. Lake.

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Digital Object Identifier 10.1109/TED.2013.2291788

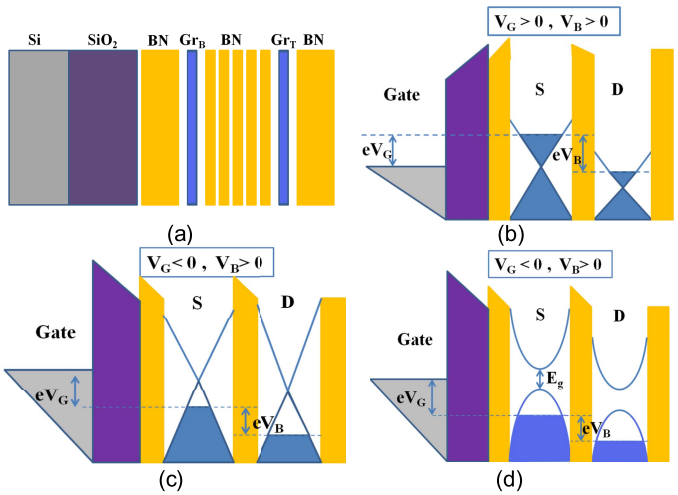

Fig. 1. (a) Sketch of a VTGFET and VTGNRFET. The band structure and operation principle for a VTGFET in the (b) off state and (c) on state. (d) The band structure and operation principle for a VTGNRFET in the on state. The source and drain are denoted by *S* and *D*, respectively.

TABLE I
TIGHT-BINDING PARAMETERS FOR HETEROSTRUCTURE OF GRAPHENE AND hBN [22], [23]. ALL PARAMETERS ARE EXPRESSED IN TERMS OF ELECTRON-VOLT

C_{onsite}	B_{onsite}	N_{onsite}	t_{CC}	t_{BN}	$t_{\perp_{\text{GrBN}}}$	$t_{\perp_{\text{BNBN}}}$
0	3.34	-1.4	2.64	2.79	0.43	0.6

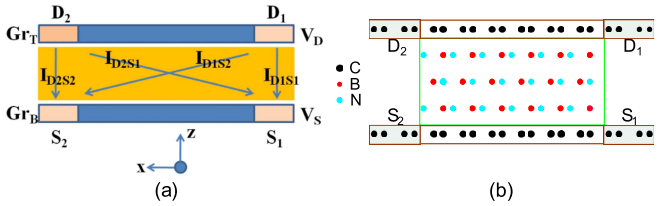

Fig. 2. (a) Sketch of the simulated structures (VTGFET and VTGNRFET) which consist of two source and drain contacts for improved electrical characteristics. (b) Atomistic diagram of the studied structure. All layers are stacked in Bernal (AB) order. In a VTGFET the graphene sheet is infinitely extended along the transverse direction.

contacts. The gate oxide is a 300 nm layer of SiO_2. To avoid the degradation of the electronic properties of the source and drain graphene/GNR sheets, two thick layers of hBN (20−50 nm) are assumed as the buffer layer. The energy barrier between the graphene Dirac point and the top of the hBN valence band (≈1.4 eV) is much smaller than that from the bottom of the conduction band (≈3.34 eV) [18]. This implies that the tunneling barrier for holes is smaller than that for electrons. Since the tunneling barrier is much larger than thermal energy, the device characteristics is approximately independent of temperature.

It is assumed that at zero bias voltages, the Dirac points of the graphene sheets are aligned with the work-function of the gate. By applying a gate voltage, the Fermi level and the carrier concentration of the source contact are modulated. Due to the atomic thickness and also relatively small concentration of carrier in graphene/GNR, the source contact only weakly screens the gate electric field. As results, the Fermi level and the carrier concentration of the drain contact are also modulated by the gate voltage. A positive gate-source voltage increases the concentration of electrons and results in n-type operation corresponding to off state, see Fig. 1(b), whereas a negative gate-source voltage results in a p-type device operation and switches on the device, see Fig. 1(c). The applied gate voltage is limited by the gate oxide breakdown which is about 1V/nm for SiO_2. The drain-source bias voltage V_B gives rise to the tunneling current through the hBN layer.

Operation of nanotransistors based on 1-D and 2-D materials, such as nanoribbons and graphene, allows access to the so-called quantum capacitance limit wherein the potential within the channel is determined mostly by the gate potential rather than the charge in the channel [19]. As a result, strong modulation of the Fermi levels of graphene/GNR sheets, and therefore, the change in barrier heights lead to relatively large tunneling currents and steep subthreshold slopes [20], [21].

In this paper, we propose using armchair GNRs instead of graphene as the base material for the source and drain contacts. In VTGNRFETs the base materials for the source and drain contacts are GNRs. As shown in Fig. 1(d), a similar operation principle holds for such devices except the presence of an energy gap along with a parabolic dispersion relation. Due to the presence of an energy bandgap in GNRs, one expects the I_{OFF} of VTGNRFETs should be smaller than that of VTGFETs which can result in a higher $I_{\text{ON}}/I_{\text{OFF}}$ ratio.

III. MODELING

A. Bandstructure and Transport Equations

An atomistic tight-binding model is used to describe the electronic bandstructure of the heterostructure of graphene and hBN (Table I). We employed the nonequilibrium Green's Function (NEGF) formalism [24] for a quantum mechanical description of carrier transport in VTGFET and VTGNRFET. In a recently fabricated VTGFET, the graphene sheets of the source and drain are in contact with several metallic electrodes [16], which provides better electrical characteristics. As shown in Fig. 2(a), a similar structure is used here. The atomistic diagram of the studied structure is sketched in Fig. 2(b). Two graphene/GNR layers at the top and the bottom are separated by hBN, all arranged in the Bernal (AB) stacking.

To study, VTGFET where the source and drain graphene sheets are infinitely extended along the transverse direction, Bloch periodic boundary condition with a period equal to $\sqrt{3}a_{\text{cc}}$, where $a_{\text{cc}} = 1.42$ Å is the carbon-carbon bonding length, is imposed [25]. The Hamiltonian of a single layered graphene/hBN in the device region can be written as

$$H_{\text{L}} = \begin{pmatrix} \beta & \alpha & 0 & 0 \\ \alpha^T & \beta^T & \alpha & 0 \\ 0 & \alpha^T & \beta & \alpha \\ 0 & 0 & \alpha^T & \ddots \end{pmatrix} + \begin{pmatrix} U_1 & 0 & 0 & 0 \\ 0 & U_2 & 0 & 0 \\ 0 & 0 & U_3 & 0 \\ 0 & 0 & 0 & \ddots \end{pmatrix} \tag{1}$$

with

$$\alpha = \begin{pmatrix} 0 & 0 \\ t & 0 \end{pmatrix} \qquad \beta = \begin{pmatrix} 0 & t_y \\ t_y^{\dagger} & 0 \end{pmatrix}. \tag{2}$$

U_i is the potential of the ith atom and is equal to the sum of on-site energy (see Table I) and the electro-static potential energy which is obtained from the capacitive model described in Section III-B. t is the hopping parameter between two nearest-neighbor carbon atoms on the graphene sheet and between two nearest-neighbor boron and nitrogen atoms on the hBN sheet. t_y is given by

$$t_y = t + te^{ik_y a_0} \tag{3}$$

For an armchair ribbon configuration, a box-boundary condition is imposed to the Dirac equation. This results in a transverse momentum which can be expressed as [26]

$$k_y = \left(\frac{2\pi}{3a_0} + \frac{2\pi n}{2W}\right) \pm \frac{2\pi}{3a_0} \tag{4}$$

where W is the width of the device and n is an integer. The last term which accounts for the momentum of the Dirac points, K and K', is used with $\pm$ sign when n is even/odd, respectively.

The device Hamiltonian can be formed as a block matrix with H_{L} blocks as diagonal elements and interlayer hopping parameter $t_\perp$ as off diagonal elements. Therefore, the device Hamiltonian is expressed as

$$H = \begin{pmatrix} \beta & \alpha & 0 & 0 & \gamma & 0 & \cdots \\ \alpha^T & \beta^T & \alpha & 0 & 0 & \gamma & \cdots \\ 0 & \alpha^T & \beta & \alpha & 0 & 0 & \cdots \\ 0 & 0 & \alpha^T & \beta^T & \alpha & 0 & \cdots \\ \gamma & 0 & 0 & \alpha^T & \beta & \alpha & \cdots \\ 0 & \gamma & 0 & 0 & \alpha^T & \beta^T & \cdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \ddots \end{pmatrix} + U \tag{5}$$

with

$$\gamma = \begin{pmatrix} 0 & 0 \\ 0 & t_\perp \end{pmatrix} \qquad U = \begin{pmatrix} U_1 & 0 & 0 \\ 0 & U_2 & 0 \\ 0 & 0 & \ddots \end{pmatrix}. \tag{6}$$

The retarded Green's function of the device with four contacts can be written as

$$G(E, k_y) = \big[EI - H(k_y) - \Sigma_{\mathrm{S1}}(E) - \Sigma_{\mathrm{S2}}(E) - \Sigma_{\mathrm{D1}}(E) - \Sigma_{\mathrm{D2}}(E)\big]^{-1} \tag{7}$$

where $\Sigma_{\mathrm{S1,S2}}$ and $\Sigma_{\mathrm{D1,D2}}$ are self-energies of the source and drain contacts. Knowing the retarded Green's function, the transmission function between some contacts j and k is evaluated as

$$T_{jk}(E) = \sum_{k_y} \mathrm{Trace}\big[\Gamma_j(E) G(E, k_y) \Gamma_k(E) G^\dagger(E, k_y)\big] \tag{8}$$

with $j = S_1, S_2, k = D_1, D_2$, and $\Gamma(E) = i[\Sigma(E) - \Sigma^\dagger(E)]$ is the broadening function of the respective contact. The summation in (8) is performed on 64 equidistant grid points for the transverse wavevector k_y. Finally, the current between the some contacts j and k is given by

$$I_{jk} = \frac{2q^2}{h} \int T_{jk}(E)\big(f_j(E) - f_k(E)\big) dE \tag{9}$$

The total current between the source and drain contact is $I = \sum_{j,k} I_{jk}$.

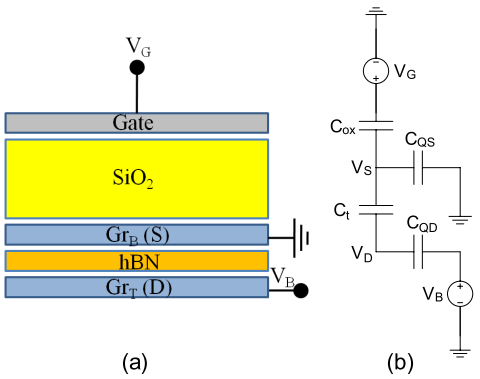

Fig. 3. (a) Device structure and (b) corresponding equivalent capacitive circuit model.

B. Self-Consistent Simulation

For an accurate analysis of VTGFETs and VTGNRFETs it is necessary to solve the transport equation self consistently with the Poisson equation. For this purpose, we use the capacitive device model described in [27]. The equivalent capacitive circuit model of the studied structures is shown in Fig. 3. C_{ox} and C_{t} are the gate insulator and tunneling barrier capacitances, respectively. These two capacitances are simply given by $C_{\mathrm{ox}} = \varepsilon / t_{\mathrm{ox}}$ and $C_{\mathrm{t}} = \varepsilon / t_{\mathrm{BN}}$, where t_{ox} is the sum of the thickness of the SiO_2 and hBN buffer layer and t_{BN} is the thickness of the hBN dielectric. The dielectric constants of both the gate insulator and the tunneling barrier are assumed to be the same and equal to $\varepsilon \approx 4\varepsilon_0$. C_{QS} and C_{QD} represent the quantum capacitances of the source and drain graphene sheets, respectively

$$C_{\mathrm{QS/D}} = \frac{\partial Q_{\mathrm{S/D}}}{\partial V_{\mathrm{S/D}}} \tag{10}$$

where $Q_{\mathrm{S/D}} = \mathrm{q}(p_{\mathrm{S/D}} - n_{\mathrm{S/D}})$ is the charge density of the source/drain contacts. One can write the electron density in graphene or GNR sheets of the source and drain contacts as

$$n_{\mathrm{S/D}} = \int f(E - E_{\mathrm{fS/D}} - \mathrm{q}V_{\mathrm{S/D}}) g(E) dE \tag{11}$$

where $g(E)$ is the DOS of graphene or GNR, depending on the contact base material. $E_{\mathrm{fS}} = 0$ and $E_{\mathrm{fD}} = E_{\mathrm{fS}} - qV_{\mathrm{B}}$ are Fermi levels of the source and drain contacts, respectively. $-qV_{\mathrm{S}}$ and $-qV_{\mathrm{D}}$ are the Dirac point potential energy of the source and drain graphene/GNR sheets, respectively, and V_{B} is the drain-source bias voltage. Assuming charge neutrality condition, V_{S} and V_{D} can be obtained from the following relations:

$$C_{\mathrm{ox}}(V_{\mathrm{G}} - V_{\mathrm{S}}) = C_{\mathrm{t}}(V_{\mathrm{S}} - V_{\mathrm{D}}) + \frac{C_{\mathrm{QS}}}{2}\left(V_{\mathrm{S}} + \frac{E_{\mathrm{fS}}}{q}\right) \tag{12}$$

$$C_{\mathrm{t}}(V_{\mathrm{S}} - V_{\mathrm{D}}) = \frac{C_{\mathrm{QD}}}{2}\left(V_{\mathrm{D}} + \frac{E_{\mathrm{fD}}}{q}\right). \tag{13}$$

One can self-consistently solve (12) and (13) along with (10) and obtain the source and drain potentials. The potential distribution along the gate oxide and hBN layers can be approximated by a linear function.

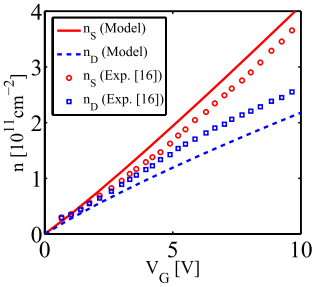

Fig. 4. Carrier concentrations of the source and drain contacts extracted from the capacitive model and experimental data of [16].

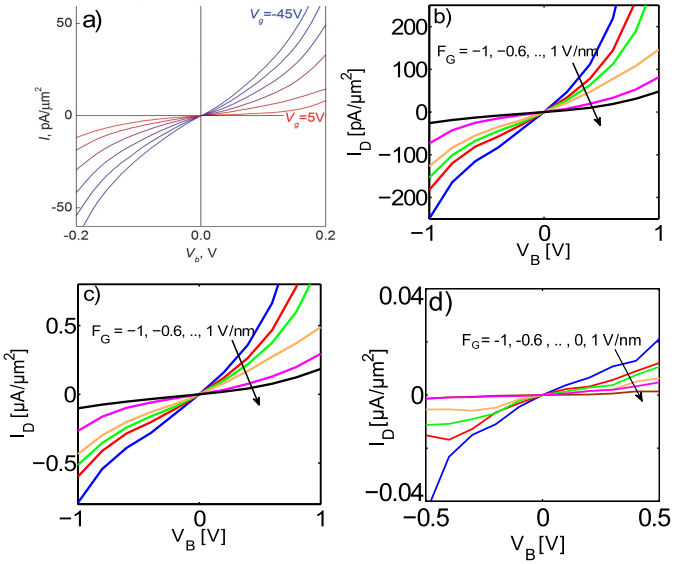

Fig. 5. Drain current as a function of the drain-source bias (V_B) based on (a) experimental data of [16], (b) atomistic simulation results for a VTGFET with $t_{\perp \mathrm{GrBN}} = 0.054$ eV regarded as a fitting parameter with experimental results, (c) atomistic simulation results for a VTGFET with $t_{\perp \mathrm{GrBN}}$ from [23], and (d) atomistic simulation results for a VTGNRFET with a GNR width of about 5 nm and seven layers of hBN. $F_G = V_G/t_{ox}$ is the gate electric field.

IV. Results and Discussion

The structure shown in Fig. 2 is studied for both VTGFET and VTGNRFET structures. VTGNRFETs are investigated at various GNR widths. For all devices three, five, and seven layers of hBN in Bernal (AB) stacking are examined. Assuming an interlayer distance of 3.5Å [22], the thickness of the hBN dielectric lies between 1 and 3 nm. For a fair comparison with experimental results [16], a 300 nm layer of SiO_2 is used as a gate oxide. The applied gate voltage is limited by the gate oxide breakdown which is about 1 V/nm for SiO_2. The bias voltage is applied between drain and source electrodes and is limited to about 1.5 V.

Fig. 4 compares the carrier concentrations of the source and drain contacts of a VTGFET at zero drain-source bias voltage evaluated from the capacitive model with that from experimental results [16], where excellent agreement verifies the accuracy of our model. The results indicate that the screening by the source graphene sheet results in a lower carrier concentration in the drain graphene sheet, especially at high carrier concentration of the source contact.

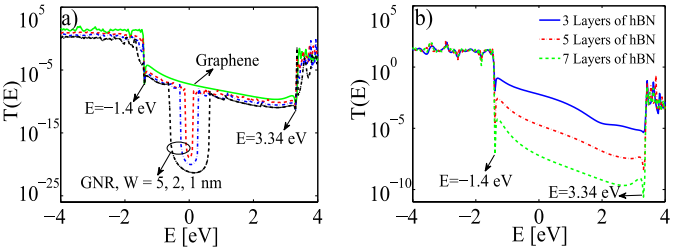

Fig. 6. Transmission probability of (a) VTGNRFET with GNR widths of 1, 2, and 5 nm compared with that of a VTGFET with seven layers of hBN and (b) VTGFET with three, five, and seven layers of hBN.

Fig. 5(a) shows the drain current as a function of the drain-source bias voltage at various gate voltages in a VTGFET based on the experimental data of [16]. Unlike conventional FETs, the current-voltage characteristics of VTGFETs is not saturated. In this structure the drain-source bias voltage significantly modulates the tunneling barrier which results in the lack of saturation in the drain current [28]. Fig. 5(b) and (c) are our numerical results for the same structure with different inter-layer hopping parameter. The results shown in Fig. 5(b) are obtained by considering the hopping parameter between the graphene and hBN sheet as a fitting parameter, where by using $t_{\perp \mathrm{GrBN}} = 0.054$ eV excellent quantitative and qualitative agreement with experimental data can be achieved. Theoretical studies [23], however, predict a much larger value for the inter-layer hopping parameter. This discrepancy can be attributed to the miss-alignment of graphene over the hBN sheet. A number of causes can also contribute to this discrepancy, such as parasitic resistances, defects, imperfections, and various scattering mechanisms. As shown in Fig. 5(c) using a larger value for $t_{\perp \mathrm{GrBN}}$ mostly affects the magnitude of the tunneling current whereas the trend of the current remains nearly the same. Throughout this paper, the inter-layer hopping parameter of [23] has been employed, see Table I.

Fig. 5(d) depicts the drain current as a function of the drain-source bias voltage for a VTGNRFET with a GNR width of 5 nm and seven layers of hBN. Apparently, the I_{ON} of the VTGNRFET is smaller than that of the VTGFET because of the presence of a nonzero bandgap of the GNR. This can be well understood by considering the transmission probability as a function of energy at various GNR widths [Fig. 6(a)]. In a VTGNRFET, because of the presence of an energy bandgap a sharp drop of the transmission probability can be observed. The width of this region depends on the energy bandgap of the GNR which is inversely proportional to the ribbon's width. The decrease of the transmission probability within the energy gap results in a smaller tunneling current of VTGNRFETs in comparison with VTGFETs.

On the other hand in a VTGFET the only degree of freedom which can affect the transmission probability is the thickness of the tunneling barrier. Fig. 6(b) shows the transmission probability of the VTGFET with three, five, and seven layers of hBN at flat band condition. The valence band and conduction band edges of hBN are at energies of -1.4 eV and 3.34 eV, respectively. The current of carriers with energies smaller than -1.4 eV and larger than 3.34 eV is due to thermionic emission

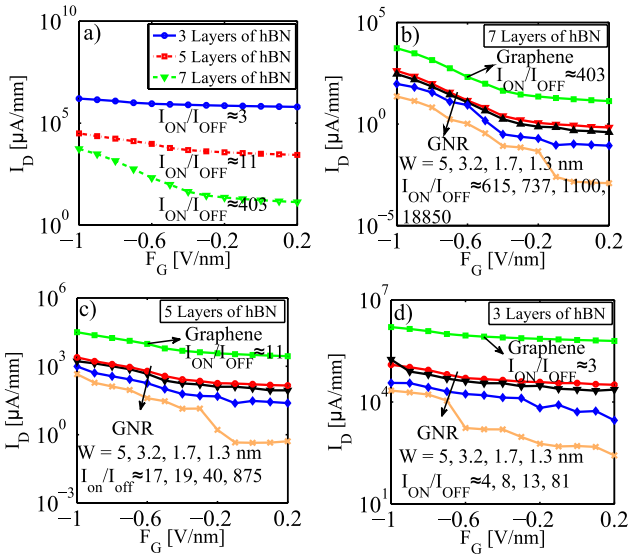

Fig. 7. (a) Drain current as a function of the applied gate electric field in VTGFET with three, five, and seven layers of hBN. Drain current as a function of the applied gate electric field in VTGNRFET at various GNR widths in comparison with that of VTGFET with (b) seven, (c) five, and (d) three layers of hBN. V_B is equal to 1.5 V.

and is nearly independent of the number of hBN layers. However, at energies between these two limits, the current is due to tunneling of carriers and exponentially decreases as the number of hBN layers increases.

VTGNRFET shows a smaller tunneling current in both the on and off state in comparison with the VTGFET, however, it exhibits a significantly larger I_{ON}/I_{OFF} ratio. Fig. 7(a)–(d) compare the drain current as a function of the applied gate electric field for VTGFET and VTGNRFET at different numbers of hBN layers and various GNR widths. As can be seen in these figures for an electric field with a magnitude of about 1 V/nm, the dependency of the tunneling current on the number of hBN layers and the width of the ribbon is weaker than that for smaller electric fields indicating that the contribution of the thermionic current increases in this regime.

Interestingly, the I_{ON}/I_{OFF} ratio for VTGNRFETs are significantly larger than that of the VTGFET. This can be understood by comparing the transmission probabilities of the VTGFET with that of the VTGNRFET (Fig. 6). While the transmission probability of a VTGFET is nearly flat close to 0 eV, the transmission probability of a VTGNRFET undergoes a sharp variation in this region due to the presence of an energy bandgap. Therefore, as the GNR width decreases the I_{ON}/I_{OFF} ratio increases due to the increase of the energy gap.

Another important figure of merit for FETs, is the subthreshold swing defined as

$$SS = \frac{dV_G}{d\left(\log(I_D)\right)}. \tag{14}$$

In available experimental data a gate oxide of 300 nm is used which results in a relatively large subthreshold swing. By employing a thin and high-κ dielectric one can significantly reduce the subthreshold swing. To gain an insight into the intrinsic limit of the VTGNRFET and VTGFETs, the variation of the source instead of the voltage is considered in (14).

TABLE II
INTRINSIC SUBTHRESHOLD SWINGS FOR VTGFET AND VTGNRFET AT DIFFERENT NUMBERS OF hBN LAYERS AND VARIOUS GNR WIDTHS. ALL PARAMETERS EXPRESSED IN TERMS OF mV/dec

		7 Layers of hBN	5 Layers of hBN	3 Layers of hBN
VTGFET		198	558	1534
VTGNRFET	4.3 nm	184	484	1297
	3.2 nm	178	463	1073
	1.7 nm	170	388	1038

The intrinsic subthreshold swings for VTGFET and VTGNRFET at different numbers of hBN layers and various GNR widths are listed in Table II. It should be noted that large I_{ON}/I_{OFF} ratios occur at large gate voltages which are much larger than the supply voltage required for the next-generation devices ($V_{DD} < 0.7$ V). The partial screening of the gate bias voltage by the graphene source contact leads to poor electrostatic control of gate voltage on the tunneling barrier. In comparison with the subthreshold swing of about 90 mV/dec in modern MOSFETs, and the ideal value of 60 mV/dec, this structure has a larger subthreshold swing. Table II shows that the subthreshold swing of the VTGNRFET is smaller than that of the VTGFET. The lower DOS and therefore smaller quantum capacitance of VTGNRFET, result in weaker screening effect in VTGNRFET structure. The increase of the numbers of hBN layers, which corresponds to a wider barrier, leads to a smaller subthreshold swing. Further improvement in the subthreshold swing is observed as the ribbon's width decreases.

For fair comparison between VTGFET and VTGNRFET, one can investigate the gate-delay time with respect to the I_{ON}/I_{OFF} ratio [29]. The intrinsic gate-delay time can be obtained as [29]

$$\tau = \frac{C_G \Delta V_G}{I_{ON}}. \tag{15}$$

C_G is extracted from the slope of the total charge in the channel with respect to the top gate voltage, I_{ON} is the on-state current and ΔV_G is equal to the difference between the I_{ON}- and I_{OFF}-state gate voltages.

Fig. 8(a) compares the intrinsic gate-delay time as a function of the I_{ON}/I_{OFF} ratio of VTGFET structures with different numbers of hBN layers. VTGFETs with thinner hBN dielectric have a much larger I_{ON}, see Fig. 7(a). As a result, smaller intrinsic gate-delay time at the cost of a lower I_{ON}/I_{OFF} ratio can be achieved for devices with three layers of hBN. In the conventional MOSFET transistors, as the I_{ON}/I_{OFF} ratio increases, the intrinsic gate-delay time increases due to the saturation of the drain current [29]. However, in VTGFET the drain current is not saturated and, therefore, an increase in I_{ON}/I_{OFF} ratio leads to a smaller and more desirable intrinsic gate-delay time. This is an important advantage of this structure in comparison with conventional MOSFET transistors.

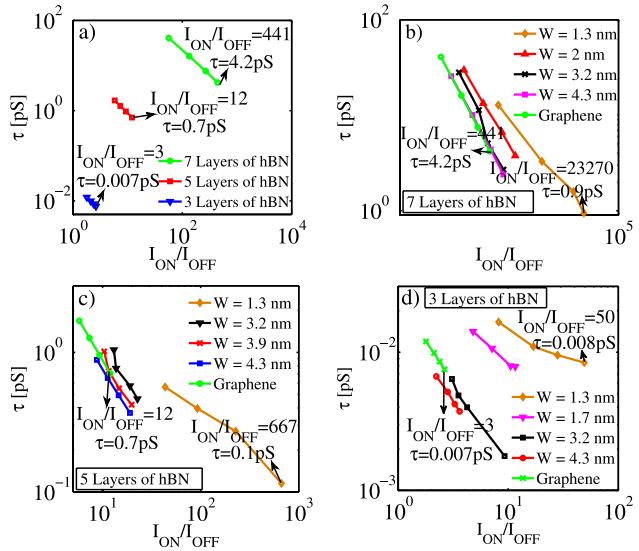

Fig. 8. (a) Intrinsic gate-delay time of a VTGFET with three, five, and seven layers of hBN. The comparison between the intrinsic gate-delay time of VTGNRFETs at various GNR widths and that of a VTGFET with (b) seven, (c) five, and (d) three layers of hBN. V_B is equal to 1.5 V.

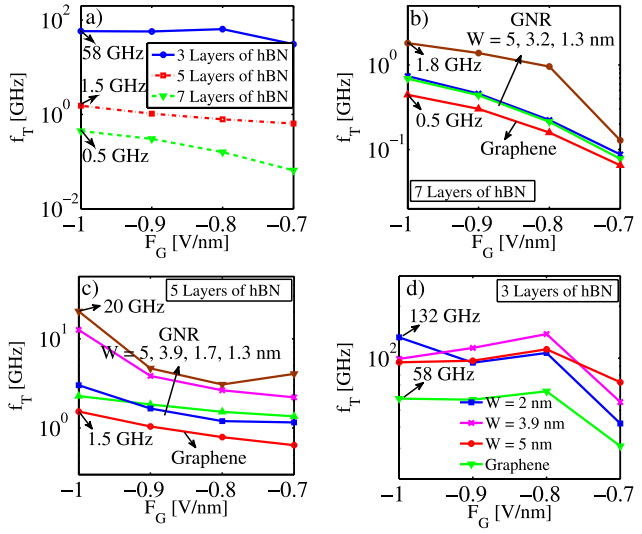

Fig. 9. (a) Cutoff frequency of VTGFET with three, five, and seven layers of hBN. The cutoff frequency of VTGNRFETs at various GNR widths in comparison with that of a VTGFET with (b) seven, (c) five, and (d) three layers of hBN. V_B is equal to 1.5 V.

Fig. 8(b)–(d) depicts the intrinsic gate-delay time of VTGFET and VTGNRFET with different numbers of hBN layers and various GNR widths. In comparison with VTGFET, VTGNRFET has a smaller I_{ON} and a smaller gate capacitance. In most cases the effect of these two terms in (15) are cancelled and an intrinsic gate-delay time similar to that of VTGFET is observed for VTGNRFETs except for those with ribbons narrower than 2 nm.

For analog applications, the cutoff frequency f_T is an important figure of merit. Assuming a quasi-static condition the cutoff frequency is given by [21]

$$f_T = \frac{g_m}{2\pi C_G} \tag{16}$$

with $g_m = \partial I_D/\partial V_G$ and $C_G = C_{GS} + C_{GD}$, where C_{GS} and C_{GD} are the gate-source and gate-drain capacitances. To focus on the intrinsic response, parasitic capacitances are neglected and only the gate insulator, tunneling barrier, and quantum capacitances are considered [21], $C_G = \partial Q/\partial V_G$, where Q is the total charge in the channel.

The cutoff frequency of VTGFET with different number of hBN layers is shown in Fig. 9(a). The cutoff frequency is inversely proportional to the hBN layer thickness. As the hBN layer becomes thinner, the control of gate voltage over the channel increases, as a result, g_m and f_T increase. The cutoff frequency of VTGFET with three layers of hBN can reach to about 60 GHz.

Fig. 9(b)–(d) benchmark the cutoff frequency of VTGNRFETs at various GNR widths and different numbers of hBN layers with that of a VTGFET. Smaller intrinsic capacitances of GNRs results in larger cutoff frequencies of VTGNRFETs in comparison with that of VTGFET. The highest cutoff frequency can reach to 130 GHz for a device with GNR width of 2 nm and three layers of hBN. Because of the presence of subbands and their dependence on GNR width, nonsmooth behavior is observed in the transconductance and as a result in the cutoff frequency, see Fig. 9(b)–(d). Due to strong modulation of the Fermi levels and carrier concentration in VTGNRFETs with three layers of hBN, the curves for such devices are more nonsmooth. As seen in Fig. 9(d), the cutoff frequency has a local peak at a gate electric field of about −0.8 V/nm, where E_{fS} moves from the valence to the conduction band which in turn increases the transconductance and cutoff frequency.

V. Conclusion

In this paper, device characteristics of VTGFETs and VTGNRFETs are investigated and compared, employing an atomistic tight-binding band structure model based on the NEGF formalism. The potential distribution is self-consistently obtained based on an accurate capacitive model. The results indicate that because of the presence of an energy gap in GNRs, the I_{ON} of VTGNRFETs is smaller than that of VTGFETs, however, the I_{ON}/I_{OFF} ratio of VTGNRFETs can be a significantly larger than that of VTGFETs. As the ribbon width increases the I_{ON} of a VTGNRFET increases at the cost of a lower I_{ON}/I_{OFF} ratio. Partial screening of the gate electric field by the source graphene contact can degrade the subthreshold swing and cutoff frequency of these structures. However, because of having smaller quantum capacitances, this problem is partially compensated in VTGNRFETs. The evaluated figures of merits for VTGNRFETs indicate that such devices can be considered as promising candidates for future electronic applications.

References

[1] A. K. Geim and K. S. Novoselov, "The rise of graphene," *Nat. Mater.*, vol. 6, no. 3, pp. 183–191, 2007.

[2] Y. M. Lin, A. V. Garcia, S. J. Han, D. B. Farmer, I. Meric, Y. Sun, *et al.*, "Wafer-scale graphene integrated circuit," *Science*, vol. 332, no. 6035, pp. 1294–1297, 2011.

[3] F. Schweirz, "Graphene transistors," *Nat. Nanotechnol.*, vol. 5, no. 7, pp. 487–496, 2010.
[4] X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai, "Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors," *Phys. Rev. Lett.*, vol. 100, no. 20, pp. 206803-1–206803-4, 2008.
[5] E. V. Castro, K. S. Novoselov, S. V. Morozov, N. M. R. Peres, J. M. B. L. dos Santos, J. Nilsson, *et al.*, "Biased bilayer graphene: Semiconductor with a gap tunable by the electric field effect," *Phys. Rev. Lett.*, vol. 99, no. 21, pp. 216802-1–216802-4, 2007.
[6] A. Y. Goharrizi, M. Pourfath, M. Fathipour, and H. Kosina, "A numerical study of line-edge roughness scattering in graphene nanoribbons," *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 433–440, Feb. 2012.
[7] A. Y. Goharrizi, M. Pourfath, M. Fathipour, and H. Kosina, "Device performance of graphene nanoribbon field-effect transistors in the presence of line-edge roughness," *IEEE Trans. Electron Devices*, vol. 59, no. 12, pp. 3527–3532, Dec. 2012.
[8] P. Gava, M. Lazzeri, A. M. Saitta, and F. Mauri, "Ab-initio study of gap opening and screening effects in gated bilayer graphene," *Phys. Rev. B*, vol. 79, no. 16, pp. 165431-1–165431-13, 2009.
[9] M. Pourfath, H. Kosina, and S. Selberherr, "Tunneling CNTFETs," *J. Comput. Electron.*, vol. 6, no. 1, pp. 243–246, 2007.
[10] P. Zhao, J. Chauhan, and J. Guo, "Computational study of tunneling transistor based on graphene nanoribbon," *Nano Lett.*, vol. 9, no. 2, pp. 684–688, 2009.
[11] G. Fiori and G. Iannaccone, "Ultralow-voltage bilayer graphene tunnel FET," *IEEE Electron Device Lett.*, vol. 30, no. 10, pp. 1096–1098, Oct. 2009.
[12] G. Fiori, A. Betti, S. Bruzzone, and G. Iannaccone, "Lateral graphene-hBCN heterostructures as a platform for fully two-dimensional transistors," *ACS Nano*, vol. 6, no. 3, pp. 2642–2648, 2012.
[13] L. Ci, L. Song, C. Jin, D. Jariwala, D. Wu, Y. Li, *et al.*, "Atomic layers of hybridized boron nitride and graphene domains," *Nat. Mater.*, vol. 9, no. 5, pp. 430–435, 2010.
[14] A. Sciambi, M. Pelliccione, M. P. Lilly, S. R. Bank, A. C. Gossard, L. N. Pfeiffer, *et al.*, "Vertical field-effect transistor based on wave-function extension," *Phys. Rev. B*, vol. 84, no. 8, pp. 085301-1–085301-5, 2011.
[15] W. Mehr, J. C. Scheytt, J. Dabrowski, G. Lippert, Y. H. Xie, M. C. Lemme, *et al.*, "Vertical graphene base transistor," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 691–693, May 2012.
[16] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, *et al.*, "Field-effect tunneling transistor based on vertical graphene heterostructures," *Science*, vol. 335, no. 6071, pp. 947–950, 2012.
[17] T. Georgiou, R. Jalil, B. D. Belle, L. Britnell, R. V. Gorbachev, S. V. Morozov, *et al.*, "Vertical field-effect transistor based on graphene-WS_2 heterostructures for flexible and transparent electronics," *Nat. Nanotechnol.*, vol. 8, no. 2, pp. 100–103, 2012.
[18] N. Kharche and S. K. Nayak, "Quasiparticle band gap engineering of graphene and graphone on hexagonal boron nitride substrate," *Nano Lett.*, vol. 11, no. 12, pp. 5274–5278, 2011.
[19] S. Luryi, "Quantum capacitance devices," *Appl. Phys. Lett.*, vol. 52, no. 6, pp. 501–503, 1988.
[20] G. Fiori, A. Betti, S. Bruzzone, P. D'Amico, and G. Iannaccone, "Nanodevices in Flatland: Two-dimensional graphene-based transistors with high Ion/Ioff ratio," in *Proc. IEDM*, 2011, pp. 11.4.1–11.4.4.
[21] G. Fiori, S. Bruzzone, and G. Iannaccone, "Very large current modulation in vertical heterostructure graphene/hBN transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 268–273, Jan. 2013.
[22] R. M. Ribeiro and N. M. R. Peres, "Stability of boron nitride bilayers: Ground-state energies, interlayer distances, and tight-binding description," *Phys. Rev. B*, vol. 83, no. 23, pp. 235312-1–235312-6, 2011.
[23] J. Sławińska, I. Zasada, and Z. Klusek, "Energy gap tuning in graphene on hexagonal boron nitride bilayer system," *Phys. Rev. B*, vol. 81, no. 15, pp. 155433-1–155433-9, 2010.
[24] M. P. Anantram, M. S. Lundstrom, and D. E. Nikonov, "Modeling of nanoscale devices," *Proc. IEEE*, vol. 96, no. 9, pp. 1511–1550, Sep. 2008.
[25] T. Low, S. Hong, J. Appenzeller, S. Member, S. Datta, and M. S. Lundstrom, "Conductance asymmetry of graphene p-n junction," *IEEE Trans. Electron Devices*, vol. 56, no. 6, pp. 1292–1299, Jun. 2009.
[26] L. Brey and H. A. Fertig, "Electronic states of graphene nanoribbons studied with the Dirac equation," *Phys. Rev. B, Condens. Matter*, vol. 73, no. 23, pp. 235411-1–235411-5, 2006.
[27] P. Zhao, R. M. Feenstra, G. Gu, and D. Jena, "SymFET: A proposed symmetric graphene tunneling field-effect transistor," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 951–957, Mar. 2013.
[28] S. B. Kumar, G. Seol, and J. Guo, "Modeling of a vertical tunneling graphene heterojunction field-effect transistor," *Appl. Phys. Lett.*, vol. 101, no. 3, pp. 033503-1–033503-5, 2012.
[29] J. Guo, A. Javey, H. Dai, and M. Lundstrom, "Performance analysis and design optimization of near ballistic carbon nanotube field-effect transistors," in *Proc. IEDM*, 2004, pp. 703–706.

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