# An analytical approach for the determination of the lateral trap position in ultra-scaled MOSFETs

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We propose a new method to determine the lateral trap position in ultra-scaled MOSFETs with a precision of less than 1 nm. The method is based on an analytical model which links the surface potential in the presence of a discrete trap to the drain voltage. We demonstrate that the dependence between the surface potential in the damaged region of the channel and the drain voltage is quasi-linear. The unique slope of this dependence corresponds to a particular lateral trap position and can thus be used as a fingerprint to locate the trap. A high accuracy is reached due to a negligibly small impact of the random dopant fluctuations on the slope magnitude. To verify our analytical approach we employ standard technology computer aided design (TCAD) methods, including random discrete dopants for both n- and p-MOSFETs with various channel lengths.

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#### 1. Introduction

The impact of interface and oxide traps on MOSFET characteristics is crucial and still of fundamental importance. 1-13) Stress induced build-up of charged defects can heavily disturb the electrostatics of a MOSFET. During device operation each trap can be charged or discharged and the kinetics of this process is defined by capture and emission times.<sup>1)</sup> This results in a local perturbation of the surface potential, and, hence, in a threshold voltage shift. 1) Defects situated in different regions of the device have a different impact on the transistor performance. As such, the information about the spatial position of the trap is of great importance. Several papers devoted to the effect of the defect position on the MOSFET performance have been published so far.<sup>2-4)</sup> In some of them, however, the impact of random dopants and traps on the channel potential is not considered.<sup>2,3)</sup> Other authors mainly focus on the impact of the trap depth in the oxide. 4,14) In this work we present an analytical model which demonstrates that the lateral channel position of the trap  $X_T$  can be extracted from the dependence between the surface potential shift in the perturbed region  $\delta \psi_s^T$  and the drain voltage  $V_d$ . The impact of randomly distributed dopants, which are always present in real ultra-scaled devices, 15-18) is accounted for. However, it is shown that this effect has only a negligible impact on the extraction accuracy.

# 2. Model description

Several papers devoted to calculation of the surface potential distribution in a MOSFET channel based on the solution of the Poisson equation have been published so far.<sup>19–22)</sup> In this work we consider n- and p-MOSFETs with a single discrete interface trap and employ an analytical expression linking the local surface potential near the trap  $\psi_s^T$  to the lateral trap position  $X_T$  and the applied drain voltage  $V_d$ . This problem is a particular case of the one described in Ref. 21. In this paper the MOSFET channel is divided into three region (one perturbed and the other unperturbed) and the Poisson equation is solved in each of the considered channel regions. For the device with a damaged region of any finite length the surface potential can be written as<sup>21)</sup>

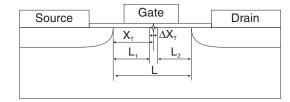


Fig. 1. Geometry of the MOSFET channel with a discrete trap at the interface

$$\psi_{\rm s}(x) = V_{\rm G} - V_{\rm FB} - \frac{Q_{\rm dep}}{C_{\rm ox}} - \frac{qN_{\rm f}}{C_{\rm ox}} + b_2 e^{kx} + c_2 e^{-kx},$$
 (2.1)

where  $V_{\rm G}$  is the gate bias,  $V_{\rm FB}$  the flat-band voltage,  $Q_{\rm dep}$  the total charge inside the depletion layer, and  $N_{\rm f}$  the density of interface charges. The coefficients  $b_2$  and  $c_2$  are extracted from the solution of the Poisson equation, while obtained from the boundary conditions k is

$$k = \sqrt{\frac{12C_{\text{ox}}}{(6\varepsilon_s + C_{\text{ox}}y_{\text{d}})y_{\text{d}}}},$$
 (2.2)

where  $\varepsilon_s$  is the dielectric constant of silicon and  $y_d$  the depth of the depletion region. The geometry of the MOSFET channel including a single discrete trap at the interface is sketched in Fig. 1. In order to adjust the model<sup>21)</sup> to our particular case of extremely small perturbed area (i.e., discrete trap) we use the following assumptions:

- 1) The lengths of the unperturbed regions are  $L_1 = X_{\rm T} 0.5\Delta X_{\rm T}$  and  $L_2 = L X_{\rm T} 0.5\Delta X_{\rm T}$  respectively. Here,  $\Delta X_{\rm T}$  is the dimension of the perturbed area, which is equal to the lateral size of the trap (typically around 0.1 nm). The distance  $\Delta X_{\rm T}$  is a perturbation of the second order and thus can be omitted, thereby resulting in  $L_2 = L X_{\rm T}$ .
- 2) The local surface potential corresponding to the trap position is obtained from (2.1) by setting  $x = X_T$ . For n-MOSFETs this point corresponds to the trap-induced potential minimum and for p-MOSFETs to the maximum.
- 3) The following approximation is used for the coordinate dependence of depletion depth  $y_d$ :

$$y_{\rm d}(x) = y_0 + y_1 \left(1 - \frac{x}{L}\right)^{5/2},$$
 (2.3)

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**Table I.** The fitting parameters used in the analytical model.

Parameter	n-MOSFET $(L = 35 \text{ nm})$	p-MOSFET $(L = 100 \mathrm{nm})$
<i>y</i> <sub>0</sub> (nm)	3.5	20
$y_1$ (nm)	20	9

where  $y_0$  and  $y_1$  are fitting parameters describing the junction depth dependence (their values are given in Table I).

With these assumptions the surface potential in the perturbed region can be written as follows:

$$\psi_{s}^{T}(X_{T}, V_{d}) = V_{G} - V_{FB} - \frac{Q_{dep}}{C_{ox}} - \frac{qN_{f}}{C_{ox}} + b(X_{T}, V_{d})e^{kX_{T}} + c(X_{T}, V_{d})e^{-kX_{T}}.$$
 (2.4)

The relations for the coefficients  $b(X_T, V_d)$  and  $c(X_T, V_d)$  are modified as compared to the case studied in Ref. 21 according to the assumptions above (see Appendix).

Equation (2.4) links the local potential near the trap  $\psi_s^T$  to the trap position  $X_T$  and the drain voltage  $V_d$ . This means that the shape of the  $\psi_s^T(V_d)$  characteristics is defined by the trap position  $X_T$ . This is the crucial assumption in our model because these characteristics can be simulated for different  $X_T$  and used to locate the trap in the channel. Evidently, in this context it is more convenient to consider only those parts of (2.4) which depend on the drain voltage  $V_d$ :

$$\delta \psi_s^T(X_T, V_d) = \psi_s^T(X_T, V_d) - \psi_s^T(X_T, V_d = 0).$$
 (2.5)

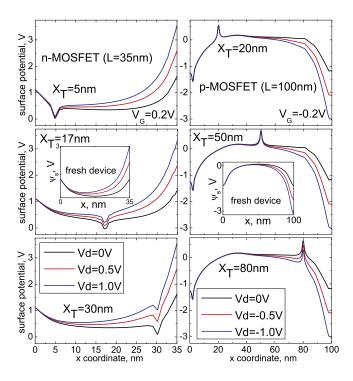
This equation describes the shift of the local surface potential  $\delta \psi_s^T$  which is completely defined by the applied drain voltage  $V_d$  for any fixed trap position  $X_T$ . For example,  $\delta \psi_s^T(V_d = 0) = 0$  for any  $X_T$ . The part independent off the drain voltage  $\psi_s^T(X_T, V_d = 0)$ , which is excluded from consideration at this stage, is affected by random dopant fluctuations as will be demonstrated below.

The described analytical model can be applied to devices with any channel length and doping. In order to assess the validity of our model, the results obtained will be compared with technology computer aided design (TCAD) simulations data.

## 3. Results and discussion

The TCAD simulations were performed on n-MOSFETs  $(N_{\rm A}=10^{18}\,{\rm cm^{-3}})$  and p-MOSFETs  $(N_{\rm D}=6\cdot 10^{17}\,{\rm cm^{-3}})$  with channel lengths of L=35 and  $100\,{\rm nm}$  respectively. Initially, the surface potential distribution along the Si/SiO<sub>2</sub> interface has been extracted for numerous lateral positions of discrete interface traps. The results for both n- and p-MOSFETS with three different positions of the interface traps are given in Fig. 2. The charged interface trap induces a local shift of the surface potential. The position of the potential minimum/maximum for an n-/p-MOSFET exactly corresponds to the trap position. In addition, one can see that the local surface potential shift depends on the applied drain voltage  $V_{\rm d}$  and that this dependence becomes stronger as the trap is shifted towards the drain.

For accurate results, the electron quantum correction potential has to be considered while modeling curves presented in Fig. 2. We use the density-gradient method<sup>23)</sup>



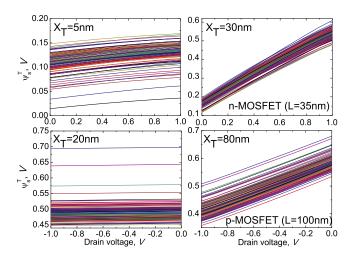
**Fig. 2.** (Color online) Surface potential distribution along the interface. Left: n-MOSFET, right: p-MOSFET. The insets illustrate the surface potential of the device without traps. Traps are located near the source (upper plots), in the center of the device (center plots) and close to the drain (lower plots).

as implemented in our device simulator Minimos-NT<sup>24</sup>) which is calibrated against our Schrödinger–Poisson solver VSP.<sup>25</sup>) This is done in order to minimize the dependence of the local surface potential near the trap  $\psi_s^T$  on the grid meshing.<sup>4</sup>) However, in the following discussion we will ignore the quantum corrections since it only weakly depends on the drain voltage and thus has no considerable impact on the differential  $\delta \psi_s^T(V_d)$  characteristics, which are used to determine the trap position.

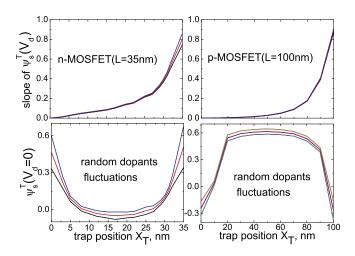
TCAD simulations have been performed for a case of weak inversion ( $V_{\rm G} \sim V_{\rm th}$ ). The trap position  $X_{\rm T}$  has been varied along the channel (i.e., between  $X_{\rm T}=0$  and L) with a step 2–3 nm for a device with L=35 and 10 nm step for L=100 nm. For each trap position hundred different random dopant configurations have been examined and typical results for n- and p-channel devices with different trap positions are given in Fig. 3. The obtained  $\psi_{\rm s}^T(V_{\rm d})$  characteristics have been linearly parameterized as follows:

$$\psi_s^T(X_T, V_d) = p(X_T)V_d + \psi_s^T(X_T, V_d = 0).$$
 (3.1)

The coefficients  $p(X_T)$  and  $\psi_s^T(X_T, V_d = 0)$  as a function of  $X_T$  are plotted in Fig. 4 (top), where the standard deviations due to random dopants are considered. One can see that the slope  $p(X_T)$  is practically not affected by random dopants, especially for devices with longer channel. The slope also strongly increases if the interface trap position is changed from the source towards the drain. In contrast, the extracted  $\psi_s^T(X_T, V_d = 0)$  may be different for similar devices with different random dopant configurations and also symmetrical with respect to the middle of the channel, Fig. 4 (bottom). For this reason extraction of the trap position based on this



**Fig. 3.** (Color online)  $\psi^T_s(V_d)$  characteristics for the different trap positions. Top: n-MOSFET, bottom: p-MOSFET.

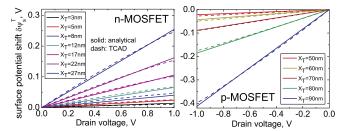


**Fig. 4.** (Color online) Slope (top) and intercept (bottom) of  $\psi_s^T(V_d)$  characteristics versus  $X_T$  for both devices. The impact of random dopants is illustrated.

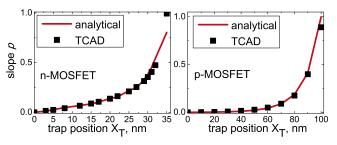
characteristic appears to be problematic. Rather, only the  $V_{\rm d}$ -induced shift of the local surface potential  $\delta \psi_{\rm s}^T$  can be used in order to determine the trap position reliably. The surface potential perturbation is

$$\delta \psi_s^T(X_T, V_d) = p(X_T)V_d. \tag{3.2}$$

This linear behavior of  $\delta \psi^T_s$  is in a good agreement with the analytical results obtained using Eq. (2.5). In Fig. 5 one can see that the  $\delta \psi^T_s(V_d)$  characteristics extracted from TCAD simulations are reasonably well reproduced by those obtained with the analytical approach for both n- and p-MOSFETs with different channel lengths. The behavior of the slope p versus  $X_T$  obtained using the analytical approach is in good agreement with the simulation results given in Fig. 6. This demonstrates the soundness of our analytical model and shows that it allows to obtain the  $X_T$ -dependent  $\delta \psi^T_s(V_d)$  characteristics for devices with different parameters without running time consuming TCAD simulations. The abrupt growth of p versus  $X_T$  allows us to determine the trap position with very high precision. In the drain side of the channel it can reach values of less than 1 nm which is



**Fig. 5.** (Color online)  $\delta \psi_s^{\Gamma}(V_d)$  characteristics for different trap positions. The analytical result obtained using Eq. (2.5) are overlaid on the data extracted from TCAD and linearly fitted with Eq. (3.2). Left: n-MOSFET. Right: p-MOSFET.



**Fig. 6.** (Color online) Slope of  $\delta \psi_s^T(V_d)$  versus trap position. Analytical results are fitted with TCAD data.

especially valuable for the characterization of traps induced by hot carrier degradation.<sup>23,26,27)</sup> It is very important that the precision of our method is not limited by the effects of random dopants, which render a practical application of some other techniques described in the literature (e.g., Ref. 3) unuseable.

#### 4. Possible experimental validation

Scanning probe microscopy techniques have developed rapidly during the last years and may be used to validate the proposed method experimentally. The setup for this can be realized using Kelvin probe force microscopy (KPFM) equipment<sup>28–30)</sup> with the possibility to apply  $V_d$ , as shown in Fig. 1 from.<sup>29)</sup> There it is assumed that the potential measurements can be performed on the edges of the device. Thus the measured profiles will contain the information about all traps situated within several nanometers into the bulk, depending on the channel doping level. For example, our TCAD simulations show that for the devices with  $N_{\rm D} = 6 \times 10^{17} \, {\rm cm}^{-3}$  one should be able to detect the traps situated up to 2-3 nm from the edges and for  $N_{\rm D} = 3 \times 10^{18} \, {\rm cm}^{-3}$  up to 4–5 nm. Although the potential spikes corresponding to the traps situated farther from the edges will be less pronounced, the slope of  $\delta \psi_s^T(V_d)$ characteristics will be independent on the width position. One should also note that although it is rather difficult to detect the traps situated far in the bulk of the device, the characterization of near-edge traps for numerous devices will give a good statistic on the trap distribution in the corresponding set of devices.

However, the measured potential profiles may also contain the spikes induced by random dopants and it is thus very important to separate them from the ones corresponding to the traps. In order to do this one should repeat the measurements several times and see which spikes have a trap-like behavior versus time (i.e., being unstable, thereby indicating charging and discharging). Then the  $\psi_s^T(V_d)$ dependencies have to be extracted only for those spikes which correspond to the traps. After this the background potential  $\psi_s^T(V_d = 0)$  has to be subtracted in order to obtain the  $\delta \psi_s^T(V_d)$  characteristics and their slope values. Finally, the slope values extracted from the experimental data have to be overlaid on similar analytical data in order to obtain  $X_T$ . Note that the extraction of the lateral trap position from the  $\delta \psi_s^T(V_d)$  dependencies may give a higher accuracy than the direct extraction of  $X_T$  from the measured potential profiles. The reason for this is that the lateral resolution of the KPFM technique for potential measurements is typically limited to around 10 nm.<sup>28)</sup> From the other side the potential magnitudes versus  $V_{\rm d}$  containing all the information about the trap positions can be measured with a very high accuracy (up to several mV). Also, taking into account the simplicity of our analytical model one can simulate the similar dependencies versus the source voltage  $V_s$  and measure the corresponding potential profiles. This will allow to increase the accuracy of the  $X_{\rm T}$  evaluation in the source side of the channel and also may be useful to solidify the results obtained using  $V_{\rm d}$ dependencies.

#### 5. Conclusions

An analytical expression linking a trap-induced surface potential shift to the applied drain voltage and trap position has been derived. The results obtained from the proposed model are in a good agreement with TCAD simulations for n-and p-MOSFETs with different channel lengths. It has been demonstrated that the lateral position of the charged interface traps in MOSFETs can be estimated precisely from the drain voltage dependence of the trap-induced surface potential shift. The main advantage of the method is that the random dopant fluctuations have only a negligibly small impact on its accuracy. The proposed method has a high potential of practical realization using modern scanning probe microscopy techniques.

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## **Appendix**

The coefficients  $b(X_T, V_d)$  and  $c(X_T, V_d)$  which are used in the analytical model are given by

$$b(X_{\rm T}, V_{\rm d}) = \frac{d_3(X_{\rm T})d_5(X_{\rm T}) - d_2(X_{\rm T})d_6(X_{\rm T}, V_{\rm d})}{d_1(X_{\rm T})d_5(X_{\rm T}) - d_2(X_{\rm T})d_4(X_{\rm T})}, \quad (A \cdot 1)$$

$$c(X_{\rm T}, V_{\rm d}) = \frac{d_1(X_{\rm T})d_6(X_{\rm T}, V_{\rm d}) - d_3(X_{\rm T})d_4(X_{\rm T})}{d_1(X_{\rm T})d_5(X_{\rm T}) - d_2(X_{\rm T})d_4(X_{\rm T})},$$
(A·2)

$$d_1(X_{\mathsf{T}}) = (1 - \tanh kX_{\mathsf{T}})e^{kX_{\mathsf{T}}},\tag{A.3}$$

$$d_2(X_{\rm T}) = (1 + \tanh kX_{\rm T})e^{-kX_{\rm T}},$$
 (A·4)

$$d_3(X_{\rm T}) = \frac{qN_{\rm f}}{C_{\rm ox}} + \frac{V_{\rm bi} - V_{\rm G} + V_{\rm FB} + \frac{Q_{\rm dep}}{C_{\rm ox}}}{\cosh kX_{\rm T}},$$
 (A·5)

$$d_4(X_T) = (1 + \tanh k(L - X_T))e^{kX_T},$$
 (A·6)

$$d_5(X_{\rm T}) = (1 - \tanh k(L - X_{\rm T}))e^{-kX_{\rm T}},$$
 (A·7)

$$d_6(X_{\rm T}, V_{\rm d}) = \frac{qN_{\rm f}}{C_{\rm ox}} + \frac{V_{\rm d} - V_{\rm bi} - V_{\rm G} + V_{\rm FB} + \frac{Q_{\rm dep}}{C_{\rm ox}}}{\cosh k(L - X_{\rm T})}.$$
 (A·8)

- T. Grasser, B. Kaczer, W. Goes, H. Reisinger, T. Aichinger, P. Hehenberger, P.-J. Wagner, F. Schanovsky, J. Franco, M. Toledano-Luque, and M. Nelhiebel, IEEE Trans. Electron Devices 58, 3652 (2011).
- S. Lee, H.-J. Cho, Y. Son, D. S. Lee, and H. Shin, IEDM Tech. Dig., 2009, p. 763.
- 3) E. R. Hsieh, Y. L. Tsai, S. S. Chung, C. H. Tsai, R. M. Huang, and C. T. Tsai, IEDM Tech. Dig., 2012, 19.2.1.
- A. Asenov, R. Balasubramaniam, A. R. Brown, and J. H. Davies, IEEE Trans. Electron Devices 50, 839 (2003).
- M. Toledano-Luque, B. Kaczer, Ph. Roussel, M. J. Cho, T. Grasser, and G. Groeseneken, J. Vac. Sci. Technol. B 29, 01AA04 (2011).
- 6) P. M. Lenahan, Microelectron. Eng. 69, 173 (2003).
- T. Grasser, H. Reisinger, P.-J. Wagner, D. Kaczer, F. Schanowsky, and W. Gös, Proc. IRPS, 2010, p. 16.
- B. Kaczer, P. J. Roussel, T. Grasser, and G. Groeseneken, IEEE Electron Device Lett. 31, 411 (2010).
- M. Toledano-Luque, B. Kaczer, T. Grasser, P. J. Roussel, J. Franco, and G. Groeseneken, J. Vac. Sci. Technol. B 31, 01A114 (2013).
- R. Dreesen, K. Croes, J. Manca, W. De Ceuninck, L. De Schepper, A. Pergoot, and G. Groeseneken, Microelectron. Reliab. 41, 437 (2001).
- T. Grasser, K. Rott, H. Reisinger, P.-J. Wagner, W. Goes, F. Schanovsky, M. Waltl, M. Toledano-Luque, and B. Kaczer, Proc. IRPS, 2013, p. 1.
- J. Franco, B. Kaczer, M. Toledano-Luque, M. F. Bukhori, P. J. Roussel, T. Grasser, A. Asenov, and G. Groeseneken, IEEE Electron Device Lett. 33, 779 (2012).
- 13) E. R. Hsieh and S. S. Chung, Appl. Phys. Lett. 101, 223505 (2012).
- 14) P. Fang, K. K. Hung, P. K. Ko, and C. Hu, IEEE Electron Device Lett. 12, 273 (1991).
- T. Mizuno, J. Okumtura, and A. Toriumi, IEEE Trans. Electron Devices 41, 2216 (1994).
- 16) P. A. Stolk and D. B. Klaassen, IEDM Tech. Dig., 1996, p. 627.
- 17) H. S. Wonga and Y. Taur, IEDM Tech. Dig., 1993, p. 705.
- T. Cochet, T. Scotnicki, G. Ghibaudo, and A. Poncet, ESSDERC Tech. Dig., 1999, p. 680.
- 19) C.-Y. Wu and S.-Y. Yang, Solid-State Electron. 27, 651 (1984).
- C.-Y. Wu, G.-S. Huang, and H.-H. Chen, Solid-State Electron. 29, 387 (1986).
- 21) Y.-S. Jean and C.-Y. Wu, IEEE Trans. Electron Devices 44, 441 (1997).
- 22) K. Y. Huang, C. S. Ho, M. Tang, and J. Liou, ICSE Proc., 2004, p. 601.
- M. G. Ancona, N. S. Saks, and D. McCarthy, IEEE Trans. Electron Devices 35, 2221 (1988).
- 24) T. Binder, K. Dragosits, T. Grasser, R. Klima, M. Knaipp, H. Kosina, R. Mlekus, V. Palankovski, M. Rottinger, G. Schrom, S. Selberherr, and M. Stockinger, MINIMOS-NT User's Guide, Institute for Microelectronics, TU Wien, Austria.
- 25) M. Karner, A. Gehring, S. Holzer, M. Pourfath, M. Wagner, W. Goes, M. Vasicek, O. Baumgartner, C. Kernstock, K. Schnass, G. Zeiler, T. Grasser, H. Kosina, and S. Selberherr, J. Comput. Electron. 6, 179 (2007).
- 26) A. Bravaix and V. Huard, Proc. ESREF, 2010, tutorial.
- S. E. Tyaginov, I. Starkov, H. Enichlmair, J. M. Park, C. Jungemann, and T. Grasser, ECS Trans. 35 [4], 321 (2011).
- 28) W. Melitz, J. Shen, A. C. Kummel, and S. Lee, Surf. Sci. Rep. 66, 1 (2011).
- K. Matsunami, T. Takeyama, T. Usunami, S. Kishimoto, K. Maezawa, T. Mizutani, M. Tomizawa, P. Schmid, K. M. Lipka, and E. Kohn, Solid-State Electron. 43, 1547 (1999).
- I. R. Jankov, I. D. Goldman, and R. N. Szente, Rev. Bras. Ensino Fis. 22, 503 (2000).