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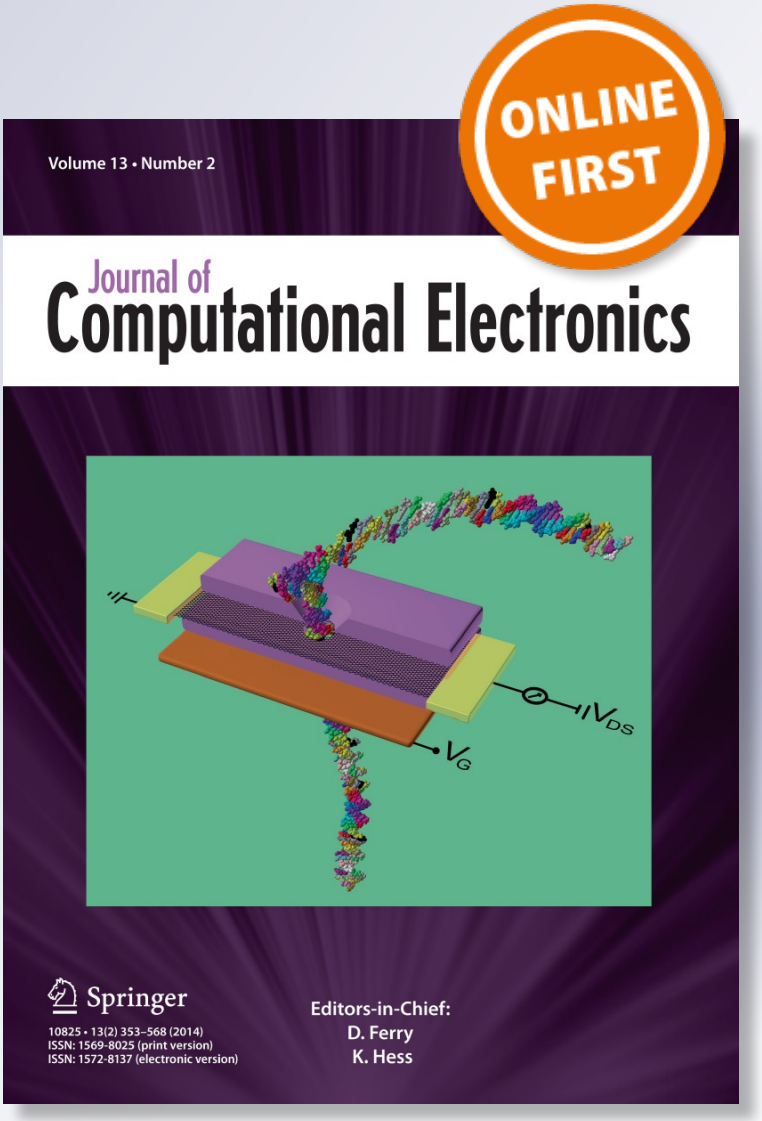

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Modeling of deep-submicron silicon-based MISFETs with calcium fluoride dielectric

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Abstract We model the main characteristics of metal-insulator-silicon field-effect transistors (MISFETs) with different gate insulators using the carrier energy distribution function calculated with a Spherical Harmonics Expansion method. In addition to standard devices with Silicon Dioxide or Oxynitride we study a hypothetical MISFET with a rather new crystalline dielectric-Calcium Fluoride. The real physical parameters of the CaF_2/Si tunnel barrier are used in our simulations. The obtained characteristics of the transistors with CaF_2 are, in some details, better than those of the devices with traditional oxides. Being a step forward in the context of the industrial implementation of fluorite, this work opens the possibility of simulating the characteristics of different silicon-based devices with crystalline insulators.

Keywords Calcium fluoride · Gate insulator · Electron energy distribution function · MISFET · Boltzmann transport equation

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1 Introduction

Molecular-beam-epitaxy technology achievements of the last years made the fabrication of high-quality thin crystalline calcium fluoride (CaF_2) layers on Si (111) surfaces possible [1]. Physically, this is due to the matching of the CaF_2 lattice constant to the one of Silicon. Nevertheless, decades of work were necessary to overcome growth problems, including formation of pinholes. While the quality of the earlier fabricated fluorite films was sufficient only for demonstrations, today one can speak about attainment of a device-relevant quality. As the most promising device application for CaF_2, barrier layers in resonant-tunneling diodes [2] and super-lattices [3] are considered and, in part, even already fabricated [4]. Another possible employment of fluorite films may be as a gate insulator in field-effect transistors [5]. This perspective may be even more attractive if combined with an old idea of three-dimensional integration by depositing silicon layers on top of the gate, maybe made of silicide, again owing to lattice-constant matching. Long ago, the authors of [6] have fabricated a metal-insulator-silicon field-effect transistor (MISFET) with CaF_2, which, however, was of considerably lower quality than films available today.

Along with a necessity for further film growth optimization, there appears a demand for better modeling capabilities. In this work we study the ordinary characteristics of a hypothetical MISFET with fluorite gate dielectric material. So far this will be a purely theoretical study. The goals are twofold. First, it is necessary to demonstrate a possibility of performing simulations of this kind using professional software, instead of home-made tools. So far, this has never been done for fluorite MISFETs. Secondly, it is important to study the differences compared to devices based on silicon dioxide or other oxides; this will concern mostly hot electron leakage modeling. Under consideration will be CaF_2 films having a

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thickness about 1-3 nm as this is the most promising range for modern MISFETs. Beyond the simulation of drain current, an analysis of hot carrier injection, also in context of insulator degradation, will be made.

2 Simulations with Minimos-NT and ViennaSHE: brief summary

Simulation of the basic characteristics of MISFETs with fluorite has been performed using Minimos-NT [7] which has already been successfully applied to wide spectra of different effects relevant in industrial devices. However the range of experimental problems solvable by this simulator is limited to near-equilibrium carrier transport which is described by shifted Boltzmann statistics. For this reason the simulations of the effects associated with hot carriers have been performed using ViennaSHE software [8], which is a deterministic solver for the Boltzmann transport equation self-consistently coupled with the Poisson equation employing the Spherical Harmonics Expansion (SHE) method [9]. The main advantages are a possibility to account for such effects as generation/recombination, quantum corrections and Electron-Electron Scattering (EES). A proper consideration of the EES effects allows to obtain the non-equilibrium carrier distribution functions (DFs) with a high accuracy. From the other side the use of a deterministic approach enables to avoid a stochastic noise typical for Monte-Carlo simulators [10] and also to reduce the simulation time. This software has already been applied for simulations of hot-carrier degradation (HCD) effects in the transistors of traditional configurations [11,12].

3 Fluoride/silicon barrier parameters

Reliable knowledge of the MIS barrier parameters is a key prerequisite for adequate simulation of a MISFET with the corresponding material combination, since a MIS structure is nothing else than the transistor gate cross-section (Fig. 1). Both voltage partitioning and gate tunneling are strongly sensitive to which numeric values are adopted.

As of today, the Si/CaF_2 barrier parameterization is not yet completed, but the convergence of measurement data is already good. So, a conduction-band offset at the Si/CaF_2 interface is $\chi_e = 2.38$ eV, and a valence band offset is $\chi_h = 8.6$ eV. The effective carrier mass for both allowed bands of the fluoride is $m_e = m_h = 1.0m_0$ within a parabolic law. The dielectric constant of fluorite is $\varepsilon_I = 8.43$, the bandgap $E_{gI} = 12.1$ eV and the electron affinity 1.67 eV.

An example of the band diagram of $Au/CaF_2/Si$ structure is given in Fig. 1. Due to a strong asymmetry of the barrier the tunneling into the gate from any band of Silicon in all cases

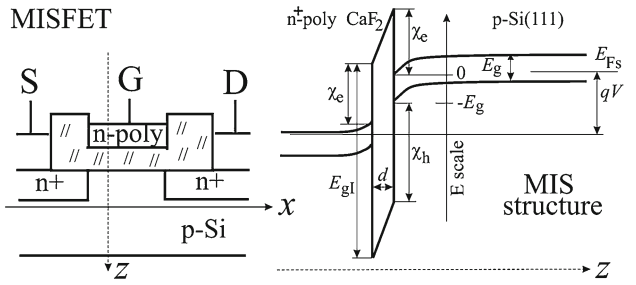

Fig. 1 Drawing of a MISFET under consideration and the band diagram of the MIS gate cross section

proceeds through the top barrier, and its probability can be written as:

$$T(E, k_\perp^2) = \exp\left[-2\hbar^{-1}\int\sqrt{2m_e\left(E_{cI}(z) - E + \hbar^2 k_\perp^2/2m_e\right)}dz\right] \quad (1)$$

Here E is a carrier energy, $k_\perp$ is a transverse momentum and E_{cI} is a coordinate-dependent energy of the conduction band edge of CaF_2. Considering a large effective-mass value, low gate currents may be expected.

4 Output characteristics of a MISFET with CaF_2

The most important MISFET characteristic is the drain current vs. drain bias, $I_d(V_d)$ curves for several values of the gate voltage V_g. As usual, the source (s), together with the back substrate contact, is suggested to be grounded. In the range of relatively low V_d, while the hot-carrier effects do not come into play, they have been simulated using Minimos-NT. The device architecture has been modeled based on the standard *imec* template of MISFET with SiON gate insulator using the Sentaurus Process [13].

The simulations were performed for the fluorite thickness $d = 2.5$ nm (i.e. effective oxide thickness EOT = 5.3 nm). The decrease of mobility due to scattering and quantization at the Si/CaF_2 interface has been described by the Hänsch model [7,14]. Also an impact of rather high surface trap concentration N_{it} has been incorporated by using the standard model implemented into Minimos-NT:

$$\tilde{\mu} = \frac{\mu_0}{1 + \theta N_{it}\exp(-r/r_{ref})} \quad (2)$$

where μ_0 is the mobility at the ideal interface, θ and r_{ref} are the parameters determining the strength of effect and the length at which the carrier situated at the distance r from the interface is affected by the interface trap. The concentration N_{it} was extracted from the measured capacitance-voltage

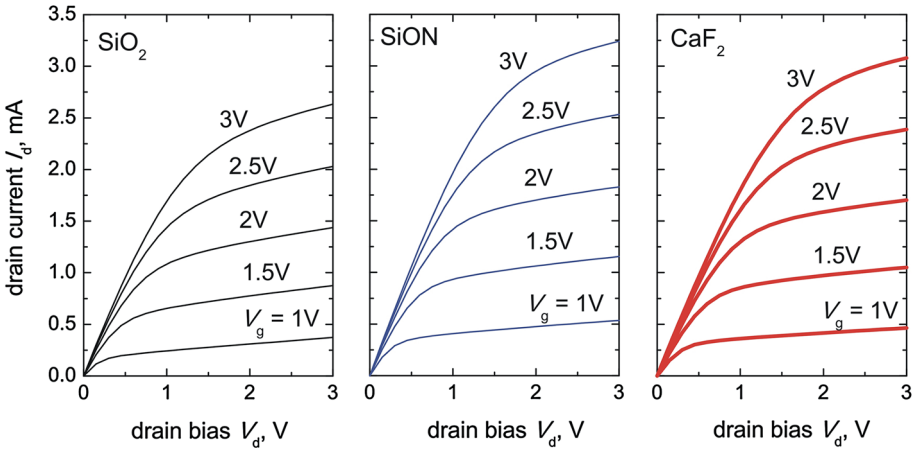

Fig. 2 Simulated output characteristics of a MISFET with CaF_2 gate dielectric in comparison with similar characteristics of the MOSFETs with SiO_2 and SiON (gate length $L_g = 65$ nm; width 44 nm)

characteristics and for CaF_2/Si(111) interface it is around 10^{12} cm^{-2}.

The set of such characteristics, as simulated by Minimos-NT, is given in Fig. 2 for the MISFETs with CaF_2 and also for the devices of similar architecture employing SiO_2 and SiON as gate insulator. The effective oxide thickness has been the same in all three cases. In the latter two situations the simulation parameters have been adjusted to fit the characteristics with their experimental counterparts.

The output characteristics obtained for the MISFET with CaF_2 look very similar to those of the regular MISFET with silicon dioxide and SiON. Particularly, the transconductance reaches nearly the same values and even slightly higher than for the devices with SiO_2.

5 Implementation of tunneling model for crystalline insulator

In the most of industrial simulators, the electron tunneling current is found as

$$j_e = \frac{4\pi q v_\perp m_\perp}{h^3} \int_0^{+\infty} \xi(E)\left(f_s(E) - f_g(E)\right) \times \int_0^E T^*(E, E_\perp) dE_\perp dE \tag{3}$$

where f_g and f_s are the carrier distribution functions for poly-gate and Si substrate. Through $E_\perp$ the part of electron energy associated with a motion in the surface plane is denoted, while $m_\perp$ and $v_\perp$ are for the electron mass in Si in that plane and the valley degeneracy. T^* is an "effective" tunneling probability. More refined models, e.g. in Ref. [15], explicitly account for surface-state quantization by adding a sum of leakages from discrete levels (and changing the lower E-limit from 0 to the Si band bending $q\phi_s$). However, in simulators, instead, a quantum correction factor $\xi(E)$ is inserted (anyway $\xi \to 0$ if $E \to 0$ and $\xi = 1$ for $E \geq q\phi_s$ or $E < -E_g$) reducing the density of states near the bottom of quantum well. The formula (3) may be rewritten also for the valence-band component j_h by appropriate resetting the integral limits for E and $E_\perp$.

Strictly speaking, the tunneling probability must be written not as function of E and $E_\perp$, but as function of E and $k_\perp$, see Eq. (1). But in many cases a trivial substitution $k_\perp^2 = 2m_\perp E_\perp \hbar^{-2}$, i.e. $T^*(E, E_\perp) = T(E, 2m_\perp E_\perp \hbar^{-2})$, can be made – in particular, for carrier transport from the Si valence band or from two conduction band valleys of Si(100). In the case of tunneling through the amorphous dielectric (e.g. SiO_2) this substitution is typically deemed acceptable. However, for the electron tunneling current through the crystalline fluorite grown on the Si substrate with (111) orientation such an approach is incorrect because the minima k_0 of all six electron valleys (shifted by $2\pi/a\Delta$ in k-space from the Γ-point, where a is the lattice constant of Si and $\Delta = 0.85$) have a huge transversal projection $k_{0\perp}$, contrary to the (100) substrate. In such a case one should either abandon Eq. (3) employing more sophisticated formulae with integrals over of E and $k_\perp$, or still keep on Eq. (3) but perform a probability averaging over the states with the given full and transverse energies [16,17]. These states are fixed with a parameter α ("angle") and thus the effective tunneling probability is given as:

$$T^* = \left\langle T\left(E, k_\perp^2(E, E_\perp, \alpha)\right)\right\rangle_\alpha \tag{4}$$

An asterisk appended to T in Eqs. (3,4) denotes the difference to "T" in Eq. (1). Both integration over E and $k_\perp$ and averaging approaches were used in our calculations, yielding

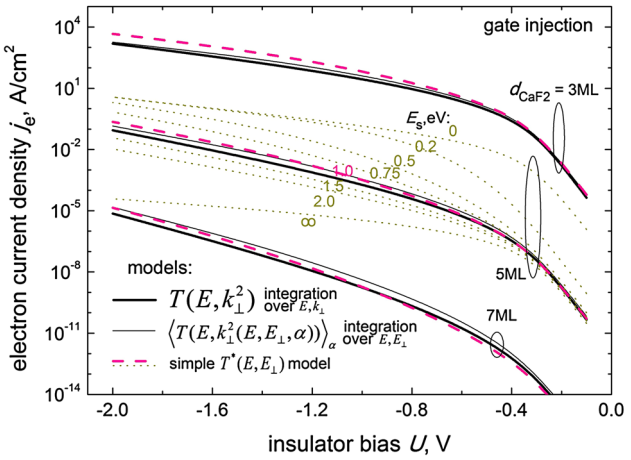

Fig. 3 Determination of a parameter of the optimized model of tunneling from Si(111) through a comparison with the more precise models. 1ML (monolayer) = 0.315 nm

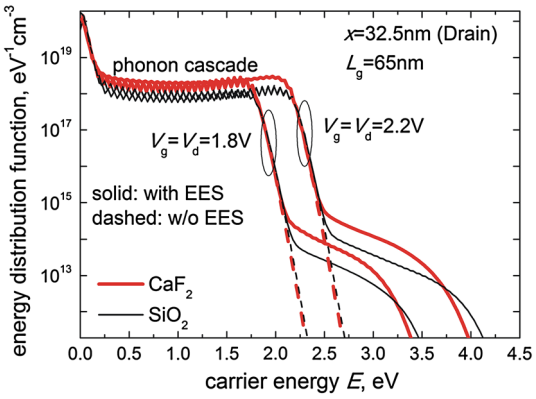

Fig. 4 The non-equilibrium electron energy distribution functions simulated for transistors of an identical architecture with different gate insulators: SiO_2 and CaF_2

quite close results [16,17]. However for implementation of the tunneling probability into the industrial simulator all this is too complex and it is worth to employ an optimized model, maybe even artificial.

Such a model can be introduced if we assume that the presence of different $k_\perp$ for the states with the given E and $E_\perp$ is roughly equivalent to some shift ΔE of the tunneling electron energy. The largest shift magnitude ($\Delta E_0 = 2.44$ eV) is achieved for $E = E_\perp = 0$, while with increasing energy the behavior is approaching to that in a direct bandgap case ($\Delta E \to 0$). Thus, the tunneling probability for CaF_2/Si(111) can be written as

$$T^*(E,E_\perp) = \exp\left[-2\hbar^{-1}\int\sqrt{2m_e\left(E_{cI}(z)-E+m_\perp m_e^{-1}E_\perp+m_0 m_e^{-1}\Delta E(E)\right)}dz\right] \quad (5)$$

where $\Delta E(E)$ is given by an equation

$$\Delta E = \Delta E_0 \exp(-E/E_s) \quad (6)$$

The preliminary simulations compared to the exact reference results give the optimum value $E_s = 1.0$ eV for the fitting parameter (example of adjusting calculation s. in Fig. 3). These calculations were made for gold-gated structures outside framework of the main simulator. It can be claimed that agreement between the results of the adapted and the exact models is very good throughout the entire range of practically interesting conditions. The optimized model for the Si(111) tunneling requires not more resources than for (100); formally, the Si(100) case can be replicated setting $\Delta E = 0$ in Eq. (6) and used in the simulator.

6 Electron heating in a channel of the CaF_2 MISFET

At the drain-source biases high enough to heat the electrons in the MISFET channel the gate leakage will be very different from the one which would be without heating in equilibrium case. As an example for simulations of electron heating, we used an ultra-scaled transistor with a gate length of $L_g = 65$ nm (*imec* design). The gate insulator physical thickness is 2.5 nm. For simulations we used two types of the devices, i.e. with SiO_2 and CaF_2 materials as gate dielectric. In the former case the substrate orientation is (100). All other device parameters – such as the doping profiles, spacer layout, etc. – are identical.

To simulate the non-equilibrium carrier energy DF (DF) dn/dE in each position x at the silicon/insulator interface we use the deterministic solver of the Boltzmann transport equation ViennaSHE [8]. This simulator incorporates such energy exchange mechanisms as scattering at ionized impurities, impact ionization, electron-phonon and electron-electron scattering. The latter mechanism, EES, is of particular importance for ultra-scaled MISFETs and especially in the context of hot-carrier degradation (HCD) [12,18,19]. It is important to emphasize that such phenomena as tunneling of non-equilibrium carriers and HCD are very sensitive to high-energy tails of the DF. In order to reliably resolve these tails, information on the device doping profiles is essential, so that the Sentaurus process simulator [13] is coupled with the device simulator. The pair of these simulators is calibrated to represent experimental transfer and output characteristics of the transistor.

A family of the carrier DFs simulated with ViennaSHE for both types of devices and operating voltages of $V_g = V_d = 1.8$ and 2.2V is shown in Fig. 4 (the lateral position corresponds to the drain end of the gate). For comparison, also distribution functions evaluated disregarding EES are depicted. All the DFs in Fig. 4 substantially deviate from the equilibrium func-

tions and exhibit plateaus at moderate energies followed by high-energy tails. Electron-electron scattering substantially affects the shape of the DFs populating these high-energy tails. One can see that in the case of the CaF_2 transistor, the values of the DFs are higher almost in the whole energy range as compared to the MOSFET with SiO_2 film. This is because CaF_2 is characterized by a higher dielectric permittivity than SiO_2 (8.43 vs. 3.9), and hence, the field in the transistor channel is also higher in the former devices. As a consequence, carrier heating is more efficient in the channel of the CaF_2 based MISFET.

7 Hot electron gate leakage in CaF_2 MISFET

Simulations of the equilibrium tunnel leakages through thin fluorite layer have been reported in several works [16,17]. It is commonly known that the use of high-ε materials, one of which is CaF_2, leads to an essential decrease of the tunneling through the gate insulator, substantially softening the impact of equilibrium gate leakages on the device performance. On the other hand, it is known that non-equilibrium carriers play a key role in the damage processes of the conventional MOSFETs, leading to HCD [11,12,18]. Thus consideration of the hot carrier injection effect for CaF_2 MISFETs is also very important in context of reliability analysis of such devices.

The major difference between simulations of the leakage current with and without heating is that in case of the equilibrium carrier transport through the insulating layer in the equation (3) one has to use the Fermi-Dirac functions for f_g and f_s, while the hot electron transport requires an application of the non-equilibrium carrier energy DFs in the equation for the current density, namely:

$$f_s(E) = dn(E)/dE \cdot \rho_{3D}^{-1}(E) \cdot \xi^{-1}(E) \tag{7}$$

where ρ_{3D} is a usual density of states known from the Silicon band structure and proportional to $E^{1/2}$near the conduction band minimum. The energy distribution of electrons dn/dE is taken at the Si/CaF_2 interface. When approaching the equilibrium state, f_s transforms into the Fermi function. Note that the term DF is often used with respect to both dn/dE and f_s; this should, however, not cause a confusion as the units are evidently different, i.e. $cm^{-3}eV^{-1}$ and eV^{-1}, respectively.

In Figs. 5 and 6, the non-equilibrium leakage currents simulated for the devices with CaF_2 are compared to those plotted for the device with SiO_2, as obtained for $V_g = V_d = 1.8$ and 2.2 V, respectively. All the curves have roughly the same form – namely, from left to right, the local current density first decreases (due to the local insulator bias lowering) and then increases near the drain (the hot carrier effect overtakes the insulator bias effect). The values of the current density near the source, where heating does not matter, are of the

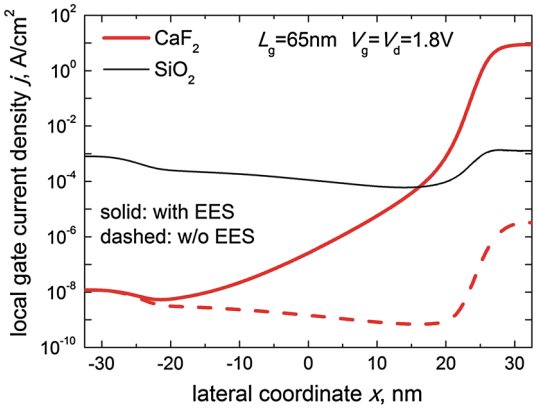

Fig. 5 The gate currents computed for CaF_2 and SiO_2 based transistors and for $V_g = V_d = 1.8$V. For comparison, currents were evaluated considering and ignoring the effect of electron-electron scattering

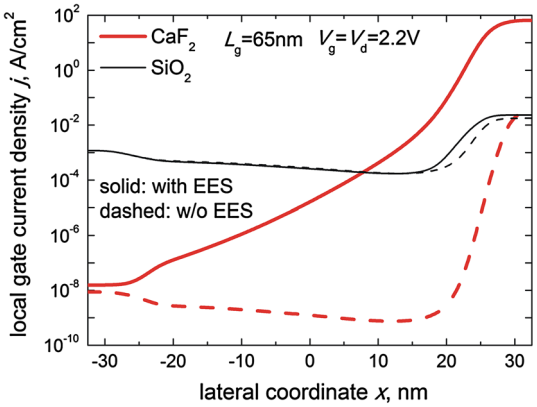

Fig. 6 The same as in Fig. 5 but simulated for $V_d = V_g = 2.2$V

same order as in our earlier simulations. Further is has been checked, also for the CaF_2 case, that the current j_h flowing between the Si valence band and the gate is much smaller than the conduction band component, i.e. one can assume $j = j_e + j_h \approx j_e$. Nevertheless, due to absence of the $k_{0\perp}$-effect (Sect. 5) for j_h, this current is, relatively, not as negligible as for the SiO_2 devices and may provide up to $\sim 10\%$ of the total current far from the drain.

One can see that near the source and in the center of the device the gate leakage is substantially lower in the CaF_2 based MISFET as compared to that simulated for the device with SiO_2. Near the drain, however, the gate current through the CaF_2 film appears to be higher. Such a trend is explained as a trade-off of two competing factors. On the one hand, the tunnel probability (calculated with a fixed carrier DF) is substantially suppressed in the CaF_2 film due to the higher dielectric permittivity ε_I, larger electron effective mass in CaF_2($1.0m_0$ compared to $0.42m_0$ in SiO_2) and also due to the transversal shift $k_{0\perp}$. On the other hand, a higher value ε_I for CaF_2 leads to a higher electric field in the channel of the CaF_2 based transistor, so that the carriers are hotter,

as compared to the device with SiO_2. The second tendency is further increased by EES which in the case of CaF_2 dramatically increases the gate current near the drain. Note also that at relatively high V_d a substantial fraction of the electrons collected by the gate electrode is being injected over the potential barrier. In the case of CaF_2, the height of the Si/dielectric barrier χ_e is lower than for SiO_2, which makes the effect even stronger.

8 Conclusion

In this work the first attempt to apply an industrial simulator to model the behavior of MISFETs with fluorite as a gate insulator have been carried out. In general, the simulations were organized inline with those for traditional oxides, although an adaptation of the tunneling current equations to the case of crystalline insulator on Si(111) was necessary. The real physical parameters of the tunnel barrier have been used. The transistor characteristics in some details are better than for the devices with traditional oxides. Being a step forward in the context of industrial implementation of CaF_2, this work opened a possibility to simulate the characteristics of different silicon-based devices with fluorite.

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