Modeling Carrier Mobility in Nano-MOSFETs in the Presence of Discrete Trapped Charges: Accuracy and Issues

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***Abstract*— This paper investigates the accuracy and issues of modeling carrier mobility in the channel of a nanoscaled MOSFET in the presence of discrete charges trapped at the channel/oxide interface. By comparing drift-diffusion (DD) and Monte Carlo (MC) simulation results, a quasi-local mobility model accounting for the complex scattering profile associated with a trapped carrier at the center of the channel is firstly derived. The accuracy of this model is evaluated on a test-bed 25-nm MOS transistor at low drain bias condition and for several applied gate biases. The issues in extending this mobility model to high drain biases regime and to the case of randomly positioned trapped charges are then discussed in the second part of this paper. Our findings show that DD simulations can maintain computational efficiency and accuracy at low drain biases, when a proper mobility model is used to describe the impact of discrete trapped charges. On the other hand, more complex corrections, that go beyond the simple mobility modification, are necessary to compensate the different carrier concentrations between DD and MC approaches at high drain biases.**

***Index Terms*— Charge trapping, mobility model, MOSFETs, reliability, semiconductor device modeling, variability.**

I. Introduction

In THE last few years, charge trapping phenomena in scaled MOSFETs have been intensively studied and identified as the root cause of several reliability issues such as random telegraph noise [1]–[6], bias temperature instabilities [7]–[12], and trap-assisted-tunneling gate leakage [13], [14]. 3-D drift-diffusion (DD) simulation studies the effects associated with charge trapping on the transistor threshold voltage V_T degradation have been recently published [2], [4], [12], [15]. The DD approach only captures the electrostatic effects that create a local exclusion of carriers in the channel around the trapped charge and reduce the overall current flowing through the device [16]. They are, therefore, perfectly apt to study the V_T degradation and variability in the subthreshold regime [15], where the electrostatic change of electron density fully governs the device behavior. However, when the object of study is the MOSFET ON-state behavior, then DD simulations become inaccurate to properly describe the short-range effects related to impurity-induced modification of carrier velocities and they lead to a severe underestimation of drain current variability [17]. In this case, Monte Carlo (MC) transport simulation has to be adopted to take into account not only the electrostatic effects, but also the scattering effects that make the impact of the trapped charge stronger and more delocalized [16]. This approach is computationally expensive. Therefore, models corrections that enable the DD approach to correctly capture the ON-current variability are highly desirable. A hierarchical approach that introduces a variability term in the bulk-mobility model has been proposed in [18]. However, this methodology does not offer a physics-based model applicable for generic cases. The aim of this paper is to derive, on the basis on MC simulation results, a quasi-local mobility model for DD simulations in the presence of discrete trapped charges. It is worth noting that, the nonlocality of the trap impact on charge transport [16], [17] enables us to seek for a mobility model that is not strongly confined around the trap position, avoiding therefore to invalidate the hypothesis of smooth mobility variations required in the derivation of DD approximated equations from the Boltzmann transport equation [19]. In the remaining of this paper, we will present our simulation methodology and a thorough derivation of a MC-corrected mobility model for DD simulation, evaluating its accuracy, and highlighting its limitations.

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II. Simulation Methodology

3-D DD numerical simulations were performed using the gold standard simulations atomistic simulator GARAND [20] on a well-scaled 25-nm template MOSFET, featuring

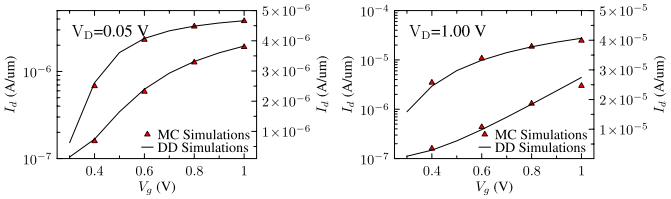

Fig. 1. DD and MC simulated I_D–V_G curves (V_D = 50 mV left, V_D = 1.0 V right) for the continuously doped MOSFET investigated in this paper. DD mobility models are calibrated to match MC results.

a thin SiO_2 oxide with thickness t_{ox} = 1.2 nm and a metal gate. Details of the structures are reported in [21]. Conventional models, namely Masetti for the doping dependence, Caughey–Thomas for the lateral field dependence, and Lombardi for the vertical field dependence [22] are used to modeling carrier mobility in the fresh (without oxide traps) device. The parameters of these models are calibrated to match the transfer characteristics obtained from the MC module of GARAND at low and high drain biases, as shown in Fig. 1. In this case, similar to other works in [23]–[25], the common scattering mechanisms (acoustic and optical phonon, surface roughness and continuous doping distributions) are included using a scattering rates table. To properly treat the scattering from the discrete trapped charges, we exclude the Coulomb scattering from the conventional scattering rate tables and introduce it through the real space trajectories of the electrons in the mesh resolved potential of the corresponding discrete charges adopting a particle-particle particle-mesh approaches [26]. In this case, the long-range component of the Coulomb interaction and the external driving electric force are properly taken into account through the mesh-based solution of Poisson's equation. However, at short range, the mesh force alone underestimates the magnitude of the Coulomb interaction between the scattering centers and an individual carrier. Therefore, the simulated mobility will be significantly overestimated. To avoid this artifact, a short-range force correction to the mesh force is employed using a well-tested analytical model [17]

$$E(r) = \frac{qr}{4\pi\epsilon_0\epsilon_r\left(r^2 + 2r_c^2\right)^{3/2}} \tag{1}$$

where r_c is a cutoff radius to which the correction reaches its maximum. Note that, at $r < r_c$ the field decreases to zero, removing the rapidly varying short-range component and the potential singularity created by the discrete trapped charge. In the following, we adopt r_c = 0.5 nm as a good compromise between the short-range scattering resolution and numerical efficiency [17]. Density gradient quantum corrections have been also incorporated in both DD and MC modules.

III. Quasi-Local Mobility Model

A. Low Drain Bias Regime

We started our analysis comparing DD and MC results obtained for the 25-nm test-bed device at low drain biases

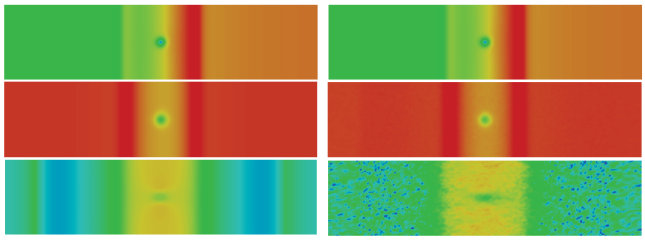

Fig. 2. DD (left) and MC (right) simulation of electrostatic potential (top), electron density (middle) and current density (bottom) for V_G = 0.8 V, V_D = 0.05 V, at 1 nm below the channel interface. A single charge is trapped at the channel/oxide interface in the middle of the channel.

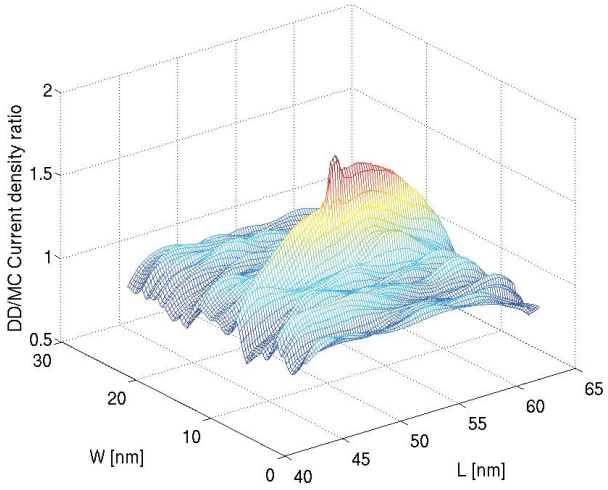

Fig. 3. Ratio between the DD and MC simulated current density at V_G = 0.8 V on a 2-D plane at 1 nm below the channel/oxide interface.

(V_D = 0.05 V). In this regime, nonequilibrium transport is minimized allowing a fair comparison between the two approaches. A single charge is trapped at the oxide interface in the middle of the channel. Fig. 2 shows the comparison between DD and MC simulation of potential, electron density, and current density in the channel for the 25-nm MOSFET template at V_G = 0.8 V. It is clear how DD simulation only captures the electrostatic effect of the trapped charge, while MC simulation is able to capture also the scattering effect associated with the trapped charge. In DD simulation, the current flow surrounds the defect: the influence of trapped charge is very local and confined. On the other hand, in MC simulation, the current flow is split in two main streams and, because of the scattering effects, the influence of the trapped charge extends far away toward the drain region. This is clearly shown in Fig. 3, where we plot the ratio between the current density obtained from DD simulation and the one obtained from MC simulation on a 2-D plane located 1 nm below the channel/oxide interface. Apart from the MC noise, the ratio is practically 1 far from the defect position. Immediately before the defect position, the DD simulation overestimates the current value. This is even more pronounced after the defect position, with a current ratio factor close to 2 is observed for more than 10 nm after the trapped charge. Please note that the device dimensions (25×25 nm^2) have been chosen to be

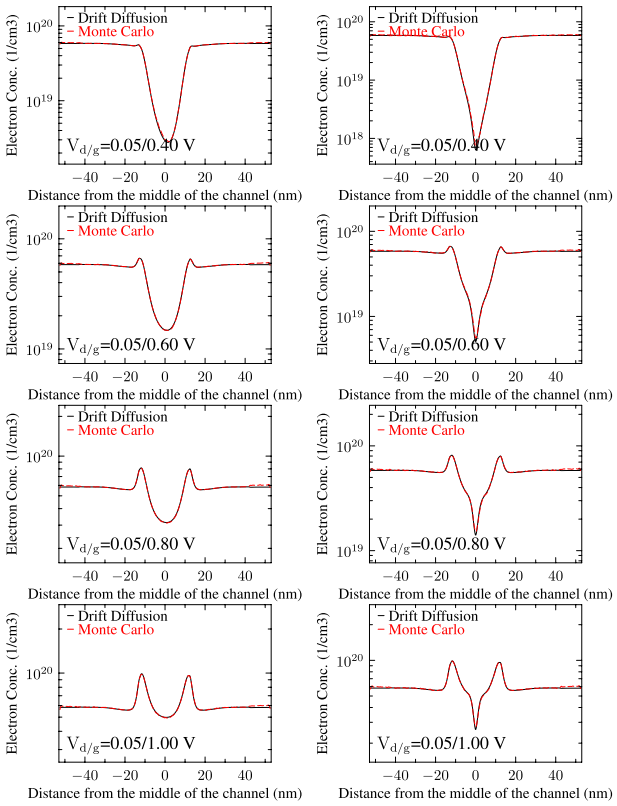

Fig. 4. DD and MC carrier concentration comparison along the channel length at 1 nm below the channel/oxide interface without (left) and with (right) trapped charge at $V_D = 0.05$ V.

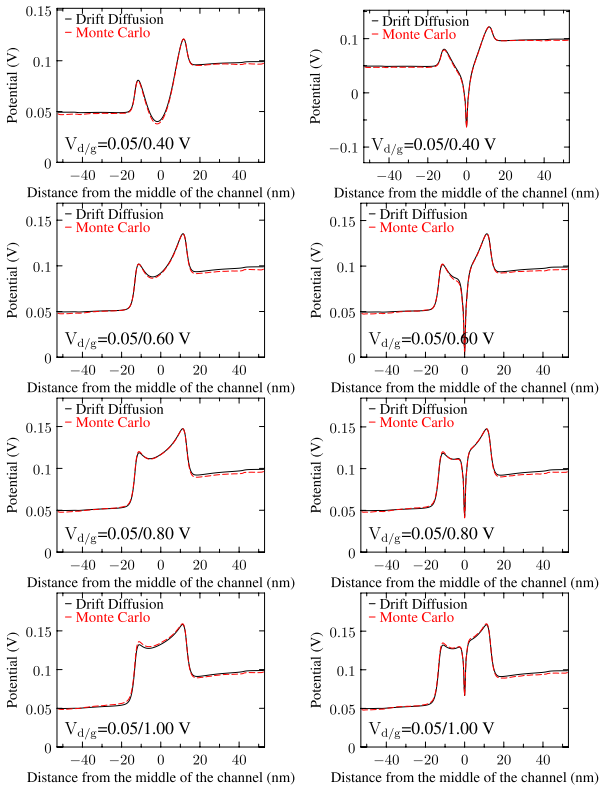

Fig. 5. DD and MC electrostatic potential comparison along the channel length at 1 nm below the channel/oxide interface without (left) and with (right) trapped charge at $V_D = 0.05$ V.

small enough to emphasize the trap impact, but large enough to avoid influence of boundary conditions on the scattering center.

To derive a mobility model able to correct DD simulations on the base of MC simulation in the presence of a discrete trapped charge, we need first of all to indentify the root cause leading to the difference between the two approaches. Because we are focusing our attention on the MOSFET ON-state regime, we can assume, with a good degree of accuracy, that the current density is mainly determined by its drift component, therefore neglecting the diffusion contribution, we have

$$\begin{cases} J_{\mathrm{DD}} \simeq q n_{\mathrm{DD}} v_{\mathrm{DD}} \\ J_{\mathrm{MC}} \simeq q n_{\mathrm{MC}} v_{\mathrm{MC}}. \end{cases} \tag{2}$$

The difference between DD and MC current densities can be due to both differences in carrier concentrations in the channel and carrier velocity fields. However, Fig. 4 shows that, at low drain voltages, n_{MC} is practically equal to n_{DD} (both with and without trapped charge), therefore the difference in the current densities is completely due to the different velocity field profile in DD and MC simulations. Moreover, expressing the velocity as product of mobility μ and electric field F and considering that the comparison of electrostatic potentials shown in Fig. 5 allows us to approximate $F_{\mathrm{DD}} \simeq F_{\mathrm{MC}}$, then we reformulate (2) as

$$\frac{J_{\mathrm{DD}}}{J_{\mathrm{MC}}} = \frac{\mu_{\mathrm{DD}}}{\mu_{\mathrm{MC}}}. \tag{3}$$

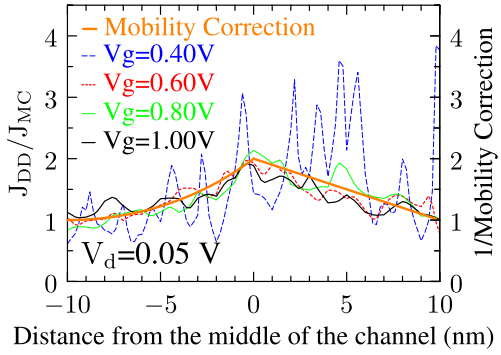

Fig. 6. Mobility correction factor along the channel length at 1 nm below the channel/oxide interface for several applied gate voltages at $V_D = 0.05$ V. An analytical approximation is also shown accordingly to (4).

In other words, the current density ratio shown in Fig. 3 shows already the inverse of the correction we should apply to the DD mobility field to match the MC results of trapped charge-induced drain current degradation. Of course, Fig. 3 shows a numerical ratio for one single applied gate voltage, while our aim is to find an analytical expression for a mobility correction valid for all the applied gate voltages above the transistor threshold. For this purpose, we show in Fig. 6, the DD/MC current density ratio along the channel length for several applied gate voltages: the ratio barely depends on the gate voltage and therefore an analytical expression for the mobility correction can easily be found. Please note that, the results at low overdrive voltage are intrinsically more noise

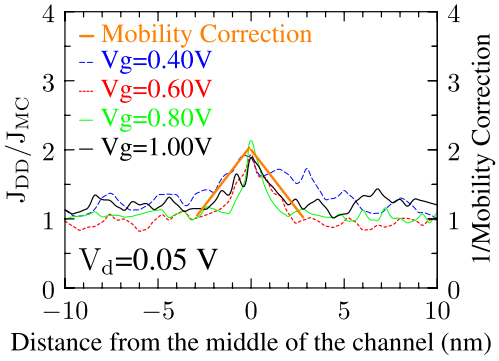

Fig. 7. Mobility correction factor along the channel width at 1 nm below the channel/oxide interface for several applied gate voltages at $V_D = 0.05$ V. An analytical triangular-shaped function approximation is also shown.

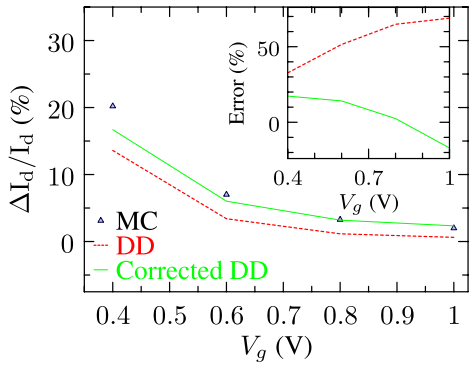

Fig. 8. Drain current degradation due to a single trapped charge at the center of the channel area as a function of applied gate voltage. DD, MC, and DD after correction simulations are reported. The relative error between DD and MC and between corrected-DD and MC are shown in the inset.

due to the stochastic nature of particle-based MC simulation. Here, we suggest a possible analytical phenomenological models for the mobility correction field Γ that can be read as

$$\Gamma = \begin{cases} \cosh(x/x_0) & x \le x_T \\ A * (x - x_T) + B & x > x_T. \end{cases} \quad (4)$$

This analytical fitting is shown in Fig. 3 together with the numerical results. Here, $x_0 = 7.6$, $A = -0.1$, and $B = 2$ are the fitting parameters, while x_T is the trap position along the channel length. Fig. 7 shows that the mobility correction factor along the channel width is well approximated by a 3-nm large triangular-shaped function, independent from the gate voltage. The same features are valid along the substrate depth direction where the mobility factor is approximated by a 1.5-nm large triangular-shaped function centered at 1 nm below the channel interface.

B. Accuracy on Drain Current Degradation

The analytical mobility model correction derived in the previous section has been implemented in GARAND and DD simulations have been carried on to evaluate the impact of a trapped charge on 25-nm MOSFET featuring a uniform doping and a single trapped charge at the center of the channel area. Fig. 8 shows the comparison between MC, DD, and corrected-DD simulation results. The relative drain degradation due to charge trapping decreases with increasing gate bias as a result of the increasing electrostatic screening effect. Due to the additional scattering effects, MC simulation predicts higher degradation with respect to DD approach. The relative error in underestimating the scattering effects is shown in the inset of Fig. 8 and increases from 30% to 70% with increasing the gate bias from 0.4 to 1.0 V. In the same figure is reported the current degradation obtained by corrected-DD: in this case, the relative error with respect MC results decreases less than 18% with much lower dependency on the applied gate voltage.

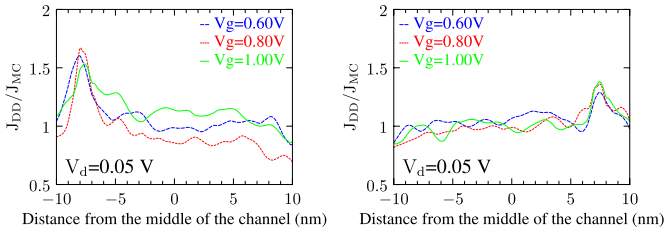

Fig. 9. Mobility correction factor along the channel length at 1 nm below the channel/oxide interface for several applied gate voltages and $V_D = 0.05$ V for a trap located close to source (left) and drain (right).

IV. Modeling Issues

In this section, we analyze and discuss the main issues that may limit the extension of this modeling approach to general MOSFETs operational conditions.

A. Impact of Trap Position

In a MOSFET featuring nanometric size, the channel electrostatics is strongly nonuniform due to the vicinity of source and drain regions. If a trap is located close to the source or drain region, then screening effects from these regions can reduce the impact of scattering of trapped charges. This is clearly shown in Fig. 9 where we report the mobility correction factor for a trap located in proximity of the source and drain regions. It is clear that the screening effect strongly reduces the long-range impact of scattering. The mobility correction factor is reduced from 2 to 1.6 (1.4) going from a trap location at the center of the channel to one at the source (drain) side. Therefore, particular care needs to be taken in the implementation of such quasi-local mobility models an appropriate envelope function needs to be applied to describe the change in the maximum correction factor with the trap position along the channel length.

B. Many Traps/Many Dopants Interactions

The analysis proposed in Section III has been carried on considering one single discrete trapped charge. A natural extension is considering the case in which many discrete charges (being them oxide trapped charge or channel dopants) are simultaneously present in the device active region. A first hurdle is represented by the overlap, at each mesh point, between the mobility correction factors coming from different

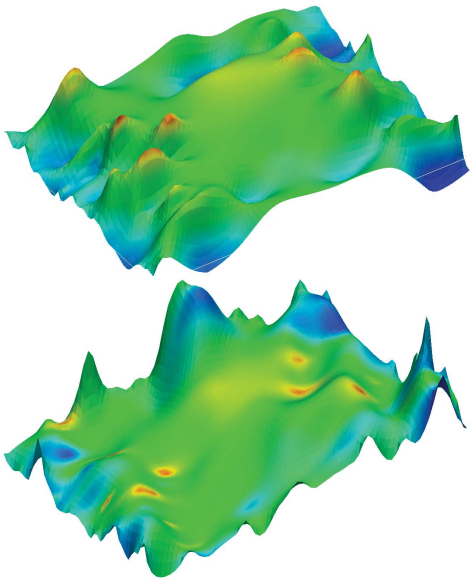

Fig. 10. Top: DD simulated current density (arbitrary units) on a 2-D plane at 1 nm below the channel/oxide interface for a MOSFET featuring many channel impurities. The locations of valleys are in correspondence of the discrete impurities positions. Bottom: ratio between DD and MC simulated current densities (arbitrary units). The map is colored according to the DD density on the top graph to show that the maxima of mobility correction are in correspondence of the discrete impurity positions. It is also highlighted that, for some impurities, the correction factor is not parallel to the source-to-drain direction but rather tilted by the disuniform electrostatic potential.

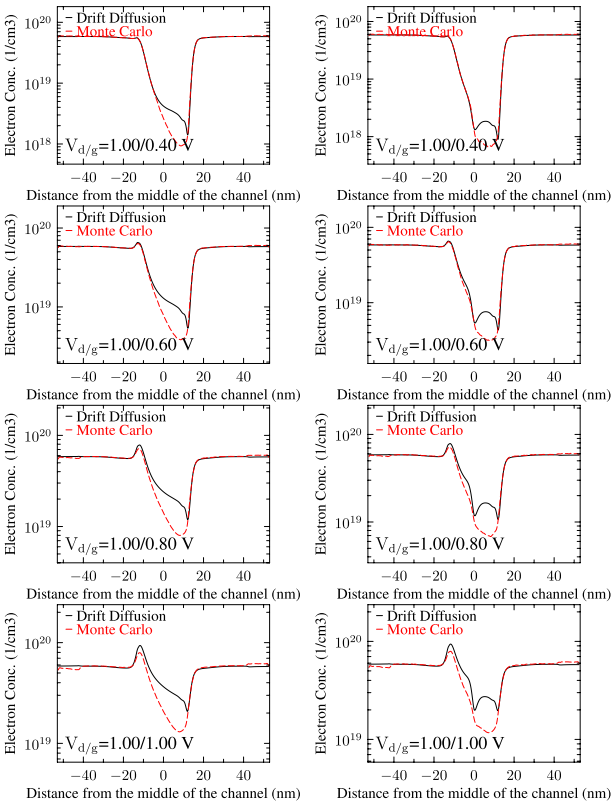

Fig. 11. DD and MC carrier concentration comparison along the channel length at 1 nm below the channel/oxide interface without (left) and with (right) trapped charge at $V_D = 1.0$ V.

discrete impurities. Fig. 10 shows the mobility correction over the channel area of a MOSFET featuring several discrete dopants in the channel. The shape of the correction between the neighbors impurities suggests that the contribution coming from each dopants cannot be computed as a direct sum but rather using a Matthiessen's rule-like sum such that, at each mesh point x_i

$$\frac{1}{\Gamma(x_i)} = \frac{1}{\Gamma_1(x_i)} + \frac{1}{\Gamma_2(x_i)} + \cdots + \frac{1}{\Gamma_N(x_i)} \tag{5}$$

where Γ_j is the mobility correction factor at the mesh point x_i coming from the jth discrete impurity.

A second hurdle is introduced by the fact that, electrostatic potential fluctuations given by many randomly placed impurities break the symmetry of the current flow observed in Fig. 3 along the channel width. Fig. 10 suggests that a mobility model correction centered at each impurity position can be still applied tilting the main axis along a direction related to the carrier velocity profile before and after the impurity. A full solution of these problematics, here highlighted, require an extensive computational and analytical study that is beyond the scope of this paper.

C. High Drain Bias Regime

Up to now, we have considered only the case in which very low voltages ($V_D = 0.05$ V) are applied to the drain contact. Much more attention needs to be paid to the case of high drain voltages, because nonequilibrium phenomena can completely change the carrier distribution obtained in MC simulation in respect to what is obtained by DD simulation. This can be clearly observed in Fig. 11, where we compare the carrier concentration along the channel length obtained from DD and MC simulations. While the DD simulation predicts a very localized drop of carriers close to the drain side due to the pinchoff effect, the MC simulation shows a more delocalized drop due to the proper treatment of nonequilibrium transport effect on the associated velocity overshoot near the drain. Moreover, the MC carrier concentration is lower, in general, all over the channel region with respect to DD results because the carrier velocity is not artificially limited by a saturation velocity parameter and ballistic transport is also possible: in the MC case, to have the same drain current given by DD simulations, a lower carrier concentration is compensated by a higher carrier velocity. As a consequence of this difference in the charge distributions, also the electrostatic potential and, in turns, the electric field obtained by MC simulation will differ from the DD ones, as shown in Fig. 12. Because of these nonequilibrium effects, the main hypotheses adopted to derive the mobility correction of (4) falls. In the high drain regime, we can still plot the ratio between DD and MC current densities, as shown in Fig. 13, but this ratio cannot be put anymore in direct correlation with the mobility ratio as done, for low drain condition, in Fig. 6. As expected, the current density ratio is strongly affected by the applied gate voltage and it may also depend on the device length. In this regime, more complex corrections, that go beyond the

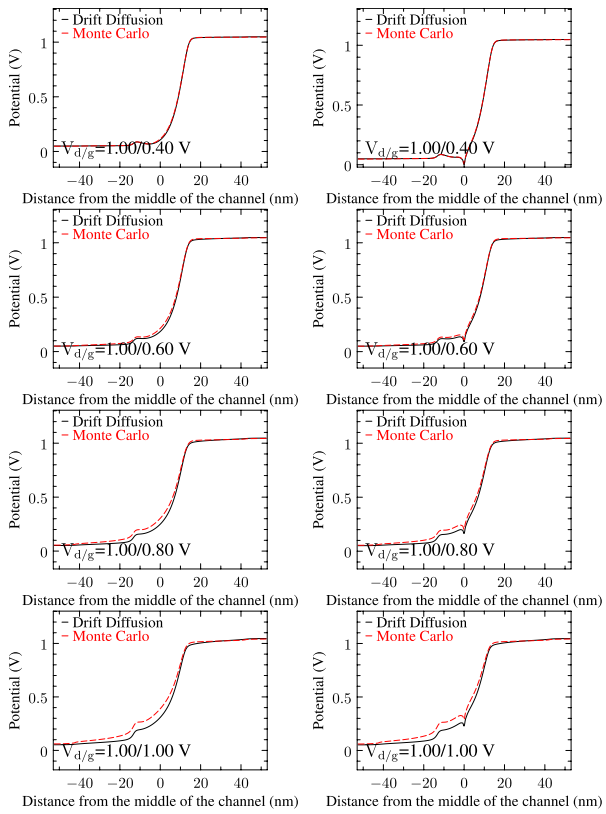

Fig. 12. DD and MC electrostatic potential comparison along the channel length at 1 nm below the channel/oxide interface without (left) and with (right) trapped charge at $V_D = 1.0$ V.

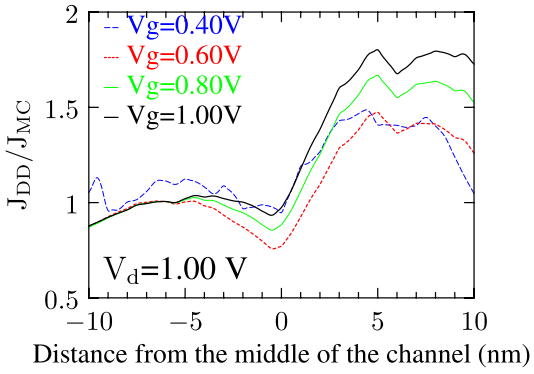

Fig. 13. Ratio between DD and MC simulated current densities along the channel length at 1 nm below the channel/oxide interface for several applied gate voltages at $V_D = 0.05$ V. In this case, the ratio cannot be put in direct correspondence with the mobility correction factor.

simple mobility modification, are necessary to compensate the different carrier concentrations between DD and MC approaches.

V. Conclusion

This paper presents a detailed comparison of DD and MC simulation of trapped charge-induced drain current degradation in a nanoscale MOSFET. A quasi-local mobility model accounting for the complex scattering profile offered by a discrete charge at the center of the channel has been proposed and its accuracy tested for several trap position, at low drain biases and for several applied gate biases. The issues in extending this mobility model to high drain biases regime and to the case of randomly positioned trapped charges have been discussed, showing that DD simulations offer computational efficiency and accuracy at low drain biases, whereas more investigation efforts are required to find reliable and physics-based modifications of the DD approach to study the impact of discrete traps on charge transport at high drain biases.

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