Drift Compensating Effect during Hot-Carrier Degradation of 130nm Technology Dual Gate Oxide P-Channel Transistors

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***Abstract*—We present hot-carrier measurement results on a 130nm dual gate oxide MOS transistor technology node which is used for automotive and analog applications with a nominal voltage of 3.3V. Transistors of several geometries have been stressed at various gate and drain voltage combinations at room and elevated (125°C) temperatures. The results show two main degradation effects with one drift type ($D_{\mathrm{Isub,max}}$) close to the traditional hot-carrier degradation worst-case condition and another ($D_{\Psi,\mathrm{max}}$) for $V_{\mathrm{ds}} = V_{\mathrm{gs}}$. Both effects compensate the drift after a specific stress time. The drifts and their compensation are clearly observable by analyzing the change of the substrate current characteristics over stress time. In the literature several mechanisms for hot-carrier degradation have been reported. The first effect is related to the bond dissociation caused by a single high energetic carrier while the second one is due to the multiple vibrational excitation of the bond by several "colder" carriers. The results underline the importance of that approach and provide a benchmark for device degradation simulations due to the good separability of the observed effects. Long term stress data show that even for low V_{gs} the drift type $D_{\mathrm{Isub,max}}$ will be compensated by $D_{\Psi,\mathrm{max}}$.**

I. Introduction

During the last decades hot-carrier degradation has become a very complex topic due to device shrinking, new technology features (like special implanting methods) and changing field conditions inside the transistor's channel. Starting with single "hot"-carriers which can break a $\mathrm{Si-H}$ bond through high energies gained by field acceleration [1]–[3] which could explain the effects observed in the late 1970's, today also "hot" fractions of particle ensembles are considered to cause the degradation at the drain region near the $\mathrm{Si-SiO_2}$ interface of MOS transistors. Furthermore, the superposition of these single-particle and multiple-particle processes has been discussed [4], [5].

To show the significance of this approach we present recent hot-carrier measurement results on a 130nm dual gate oxide MOS transistor technology which is used for automotive and analog applications and has a nominal voltage of 3.3V. A comprehensive picture of the voltage dependence of the degradation is obtained by choosing various gate and drain voltage combinations (fig. 1) for stressing the devices under test. Several transistors with different widths and lengths have been stressed to analyze the drift behavior with respect to their geometry. To capture the temperature effect on the degradation all measurements were performed at 25°C and 125°C. The results show two main degradation effects. One drift type ($D_{\mathrm{Isub,max}}$) is located close to the traditional worst-case condition for hot-carrier degradation ($\max(I_{\mathrm{sub}}\,(V_{\mathrm{gs}}))$ where the largest impact ionization rate is present [6]). Another ($D_{\Psi,\mathrm{max}}$) can be observed at $V_{\mathrm{gs}} = V_{\mathrm{ds}}$ where the carrier flux is maximal [7]–[10]. Both effects compensate the drift after a specific stress time and stress voltage combination. Here, the transition from $D_{\mathrm{Isub,max}}$ (which in this case leads to a smaller absolute threshold voltage) to $D_{\Psi,\mathrm{max}}$ occurs. We will show that these effects and their interacting drift compensation are clearly observable (e.g. for the threshold voltage drift) by analyzing the change of the substrate current characteristics over stress time.

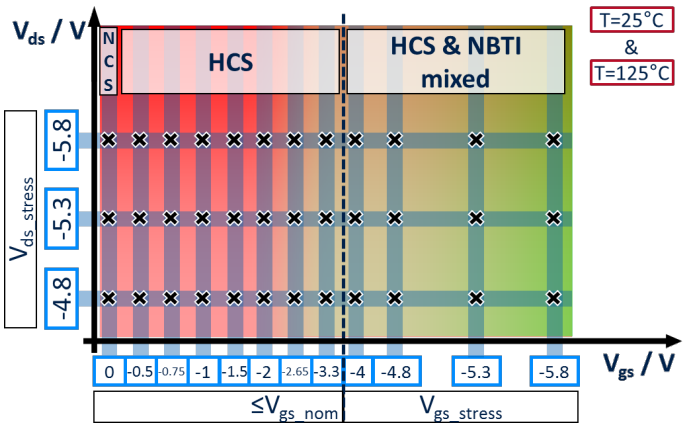

Fig. 1. The stress voltage matrix (2-dimensional parameter space with combinations of V_{ds} and V_{gs}). All experiments were performed at 25°C and 125°C. Crosses denote a measurement condition.

II. Samples

The measurements were performed on production quality pFETs with 5.2nm thick plasma nitrided dual gate oxides. The devices under test had eight different geometries (L =

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(0.37...30)µm, W = (0.4...30)µm) including short and wide, long and narrow as well as long and wide devices.

III. Measurements

The recorded data including $I_{\mathrm{ds}}(V_{\mathrm{gs}})$ and $I_{\mathrm{bs}}(V_{\mathrm{gs}})$ characteristics, operating points and threshold voltage have been obtained employing an Agilent® analyzer and a switching matrix which is used for parallel stressing the devices under test. The used measure-stress-measure technique enables us to derive the drift data for each readout. For this purpose additional 19 data sets at logarithmic equidistant readout times were recorded after the zero hour readout. The resulting cumulative stress time of each experiment was 10^4s. One additional long term measurement was extended to a cumulative stress time of 3.6×10^5s. Data from a wide range of drain and gate voltages (32 combinations) have been recorded ($V_{\mathrm{ds}} = -(4.8; 5.3; 5.8)$V, $V_{\mathrm{gs}} = (-5.8 \ldots 0)$V) to give a full picture of the device's drift behavior in the inversion region over a 2-dimensional stress voltage parameter space. To analyze the temperature influence on the presented effects (hot-carrier degradation is known to diminish at higher temperatures in long-channel devices and to become more severe in ultra-scaled counterparts [11]–[16]) all measurements have been performed at room temperature and at 125°C.

IV. Relevance of effect

For modern technologies with small channel lengths it is known that hot-carrier degradation cannot be described correctly by a substrate current based model which assumes the maximum degradation for $D_{\mathrm{Isub,max}}$ where $|V_{\mathrm{ds}}| > 3.3V \wedge V_{\mathrm{gs}} \approx V_{\mathrm{gs}}(\max(I_{\mathrm{bs}}))$ (e.g. "lucky electron model" [1], [2]) and is maximal for $D_{\Psi,\mathrm{max}}$ $V_{\mathrm{ds}} = V_{\mathrm{gs}}$ [7]–[10]. On the contrary, the recorded data show a relevant drift for $D_{\mathrm{Isub,max}}$ and a drift compensated regime between $D_{\mathrm{Isub,max}}$ and $D_{\Psi,\mathrm{max}}$. Therefore both effects and their interaction need to be taken into account for e.g. a voltage based transistor degradation model for realistic circuit simulations (especially for analog applications) where a full V_{ds} and V_{gs} dependence is needed. Because of that the tested device is a good candidate to show the two main degradation effects and their transition.

V. Results

The drift of the threshold voltage shows a decrease of the absolute threshold voltage around the region of $D_{\mathrm{Isub,max}}$ (fig. 2) for $V_{\mathrm{gs}} \approx -0.75$V and $|V_{\mathrm{ds}}| > 3.3$V. With increasing gate voltage this drift decreases and is fully compensated for $V_{\mathrm{gs}} \approx -1.75$V after 10^4s stress time. With $V_{\mathrm{gs}} \to V_{\mathrm{ds}}$ ($D_{\Psi,\mathrm{max}}$) the absolute threshold voltage is increasing to more than twice the absolute value of $D_{\mathrm{Isub,max}}$. For lower drain stress voltages this behavior is still well observable although the absolute drift attenuates.

To suppress the negative-bias temperature instability driven degradation the maximum gate voltage of all presented results is equal to the operating voltage of the devices under test (only fig. 1 and fig. 2 exceed this limitation).

Higher temperatures attenuate the drift type $D_{\mathrm{Isub,max}}$ and aggravate $D_{\Psi,\mathrm{max}}$ (fig. 2) to a 1:3 drift ratio. The drift compensation after 10^4s is not influenced by this and still located at $V_{\mathrm{gs}} \approx -1.75$V.

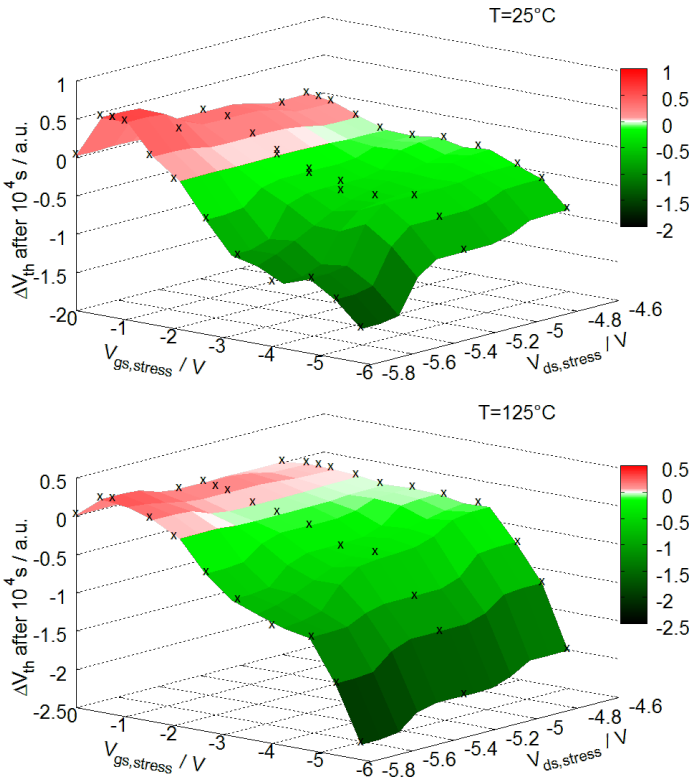

Fig. 2. Results of stress matrix showing the (absolute) threshold voltage drift after 10^4s at top) room temperature, bottom) 125°C. (x: measured data point)

For $D_{\mathrm{Isub,max}}$ with the maximum at $V_{\mathrm{ds,stress}} = -5.8$V and $V_{\mathrm{gs,stress}} = -0.5$V the substrate current characteristics show a decrease of $\max(I_{\mathrm{bs}})$ with stress time. The fresh device has a substrate current maximum located at -0.95V whereas for the aged device the maximum is at -0.85V resulting in a shift of 0.1V (fig. 3(a)).

The maximum of $D_{\Psi,\mathrm{max}}$ is observed at $V_{\mathrm{ds,stress}} = -5.8$V and $V_{\mathrm{gs,stress}} = -3.3$V (the negative-bias temperature instability is negligible because of the low temperature and $|V_{\mathrm{gs,stress}}| = 3.3\mathrm{V} = V_{\mathrm{nominal}}$) and shows a completely different behavior (fig. 4(a)). Initially the maximum substrate current increases with stress time from the fresh device with a maximum located at -0.95V up to a turning point at $\approx 3.6 \times 10^3$s for -1.20V and ends after 10^4s at -1.40V. The total shift of the $V_{\mathrm{gs}}(\max(I_{\mathrm{bs}}))$ is ≈ -0.25V (maximum of $D_{\Psi,\mathrm{max}}$) and ≈ -0.45V after 10^4s stress time.

The drift compensation ($\Delta V_{\mathrm{th}} = 0$ after 10^4s) due to both effects is best observable for $V_{\mathrm{ds,stress}} = -5.8$V and $V_{\mathrm{gs,stress}} = -1.5$V. The turning point at 1.3×10^3s is well correlated with the change of V_{th} (fig. 5). A third mechanism appears after the maximum of $D_{\Psi,\mathrm{max}}$ (fig. 4(a)) where $\max(I_{\mathrm{bs}})$ decreases and $V_{\mathrm{gs}}(\max(I_{\mathrm{bs}}))$ is shifted to a higher potential.

A comparison of the drift data from transistors with different

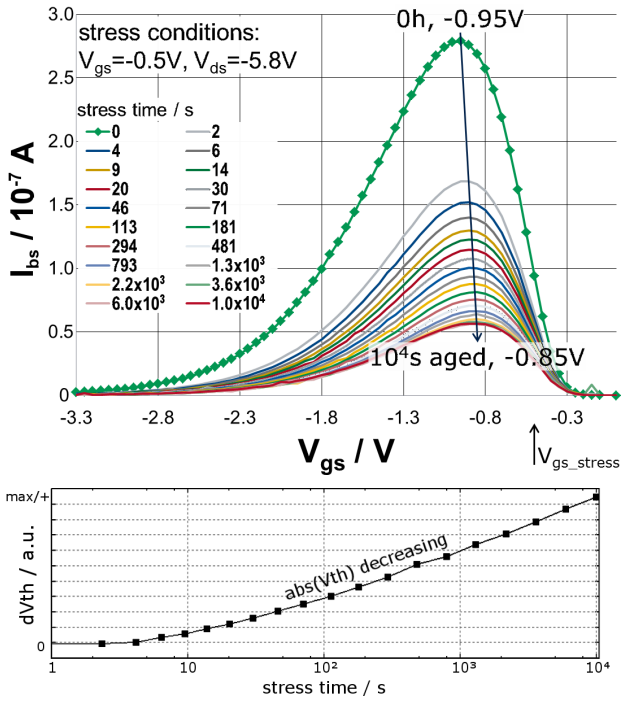

Fig. 3. Change of $I_{\mathrm{bs}}\,(V_{\mathrm{gs}})$ and V_{th} during aging at room temperature. Top: The drift type $D_{\mathrm{Isub,max}}$ is maximal for $V_{\mathrm{gs}} = -0.5\mathrm{V}$ and $V_{\mathrm{ds}} = -5.8\mathrm{V}$ after $1 \times 10^4\mathrm{s}$ and shows a constant decrease of $\max(I_{\mathrm{bs}})$. Bottom: $|V_{\mathrm{th}}|$ decreases with stress time.

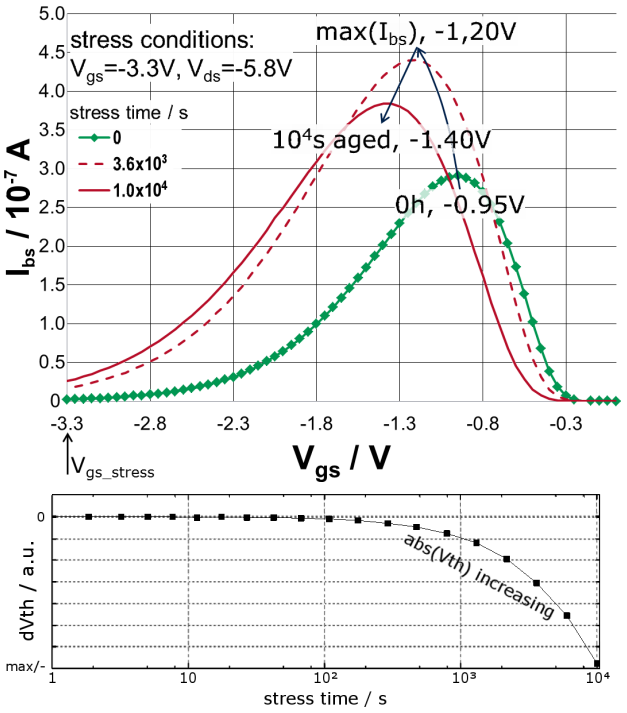

Fig. 4. Change of $I_{\mathrm{bs}}\,(V_{\mathrm{gs}})$ and V_{th} during aging at room temperature. Top: The drift type $D_{\Psi,\mathrm{max}}$ has it's maximum after $3.6 \times 10^3\mathrm{s}$ and results in a constant increase of $\max(I_{\mathrm{bs}})$. An additional effect is noticeable for larger stress times decreasing $\max(I_{\mathrm{bs}})$. Bottom: $|V_{\mathrm{th}}|$ increases with stress time.

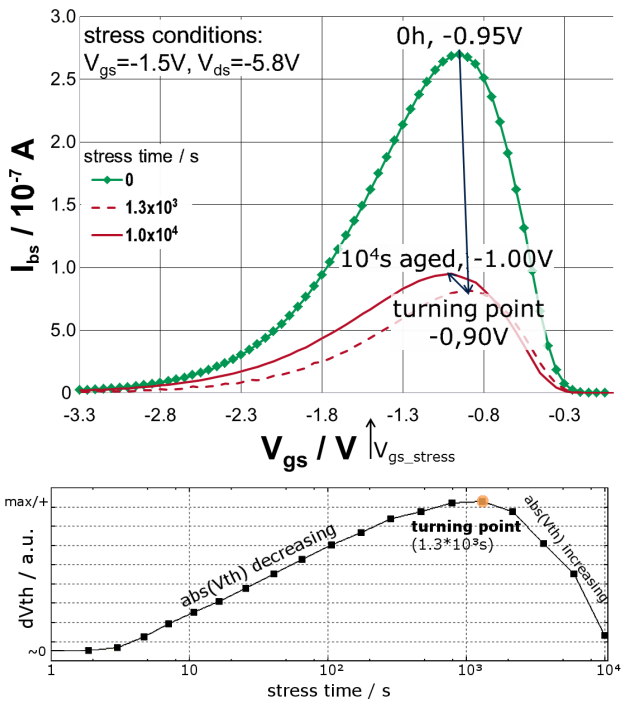

Fig. 5. The change of $I_{\mathrm{bs}}\,(V_{\mathrm{gs}})$ during aging shows a direct relation to the change of V_{th}, the common turning point is at $1.3 \times 10^3\mathrm{s}$ where $\Delta V_{\mathrm{th}} = \Delta \max(I_{\mathrm{bs}}) \approx 0$. Top: measured combination of drift types $D_{\mathrm{Isub,max}}$ and $D_{\Psi,\mathrm{max}}$. Bottom: First drift type $D_{\mathrm{Isub,max}}$ decreases $|V_{\mathrm{th}}|$ with the stress time until a turning point after which $D_{\Psi,\mathrm{max}}$ dominates the aging process leading to an increase of $|V_{\mathrm{th}}|$.

geometries indicates that the compensation is not influenced by the geometry and always located at $V_{\mathrm{gs}} \approx -1.75\mathrm{V}$. The drift ratio ($D_{\mathrm{Isub,max}}$:$D_{\Psi,\mathrm{max}}$) data (tab. I) show several groups of devices. On the one hand, there are short and wide channel transistors (1, 3, 4) with comparable drift ratio values. On the other hand, there are long and narrow devices (6, 7, 8) together with long and wide devices (2, 5) which have a very small drift in general for the applied stress time of $10^4\mathrm{s}$. Only higher temperatures show a recognizable drift of the threshold voltage for that group.

Both the room and elevated temperature data show an increase of the drift ratio up to $0.5\,\mu\mathrm{m}$ while the length is increasing. The $2\,\mu\mathrm{m}$ long device has the smallest drift ratio.

Analyzing the long term stress data at $3.6 \times 10^5\mathrm{s}$ for low gate

Table I
Drift ratio ($D_{\mathrm{Isub,max}}$:$D_{\Psi,\mathrm{max}}$) of several transistor geometries at room and elevated temperatures. n.d.: drift not detectable

Transistor	**L/µm**	**W/µm**	**ratio,** 25 °C	**ratio,** 125 °C
1	0.37	10	1:2.2	1:3.1
2	2	10	1:2.6	1:7.8
3	0.43	10	1:1.9	1:3.0
4	0.5	10	1:1.3	1:2.6
5	30	30	n.d.	1:12.1
6	1	0.5	n.d.	1:2.6
7	2	0.5	n.d.	1:7.4
8	2	0.4	n.d.	1:3.2

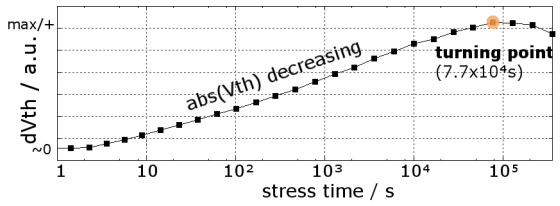

Fig. 6. Long term stress data show that even for low $V_{\mathrm{gs}} = -0.75\mathrm{V}$ the drift type $D_{\mathrm{Isub,max}}$ will be compensated by $D_{\Psi,\mathrm{max}}$. The turning point is located at $7.7 \times 10^4\mathrm{s}$.

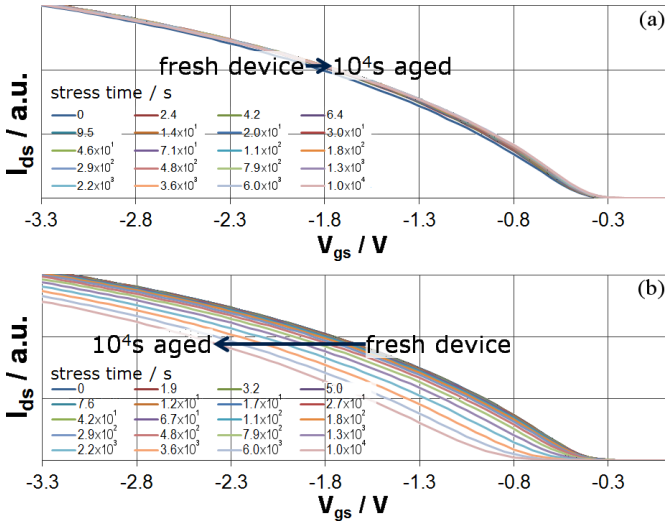

Fig. 7. Change of $I_{\mathrm{ds}}\,(V_{\mathrm{gs}})|_{V_{\mathrm{ds}}=-0.1V}$ during aging for a) $D_{\mathrm{Isub,max}}$, b) $D_{\Psi,\mathrm{max}}$ at room temperature. For drift type $D_{\mathrm{Isub,max}}$ the values of $I_{\mathrm{ds,lin}}$ are not changing significantly while $D_{\Psi,\mathrm{max}}$ shifts the whole characteristic to higher absolute potentials.

voltages ($-0.75\,\mathrm{V}$) a compensation of the degradation around $7.7 \times 10^4\mathrm{s}$ is observable (fig. 6).

The change of the linear characteristics ($I_{\mathrm{ds}}\,(V_{\mathrm{gs}})|_{V_{\mathrm{ds}}=-0.1V}$) during aging for the drift type $D_{\mathrm{Isub,max}}$ is much less significant than for $D_{\Psi,\mathrm{max}}$ (fig. 7). The former shifts the characteristics to slightly lower potentials while the latter shifts them to noticeable higher potentials resulting in a total shift of about $-0.9\mathrm{V}$.

VI. Discussion

In the literature several mechanisms for hot-carrier degradation have been reported. Single "hot" carriers which can gain high enough energies through field acceleration to break a Si-H bond [2], [3], [17], "hot" fractions of particle ensembles like for instance caused by impact ionization [18], Auger recombination [19], electron-phonon [20], [21] and electron-electron scattering [22], [23]. Further, the superposition of single and multiple carrier effects has been discussed [24], [25].

The first mechanism is assumed to be due to bond dissociation triggered by a solitary hot carrier. This process is typical for (relatively) high-voltage devices. In this case the indicator of hot-carrier degradation severity is the average (over the ensemble) carrier energy, and hence as a related

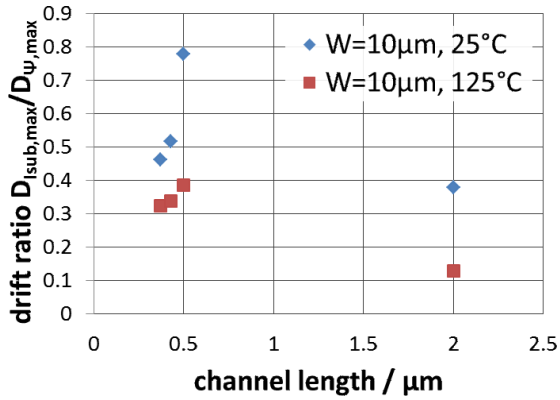

Fig. 8. The drift ratio is increasing with the channel length up to $0.5\,\mu\mathrm{m}$. Between $0.5\,\mu\mathrm{m}$ and $2\,\mu\mathrm{m}$ a strong decrease is observable. A maximum of the ratio $D_{\mathrm{Isub,max}} : D_{\Psi,\mathrm{max}}$ is expected in-between.

quantity, the substrate current, is widely used for hot-carrier degradation assessment. As a result, the worst-case conditions of hot-carrier degradation correspond to the substrate current maximum ($D_{\mathrm{Isub,max}}$). In scaled devices, on the other hand, a series of bond bombardment events by "colder" carriers can induce the multiple vibrational bond excitation. Thus, the multiple-carrier mechanism is dominating if device dimensions shrink. In this situation, the carrier flux rather than the particle energy is important and worst-case conditions correspond to the maximum flux ($D_{\Psi,\mathrm{max}}$). However, even in ultra-scaled devices the high-energy fraction of the carrier ensemble can be populated by scattering mechanisms such as impact ionization, Auger recombination, electron-phonon and electron-electron scattering.

In terms of hot-carrier degradation, the transition from long-channel to short-channel devices occurs at a channel length below $180\mathrm{nm}$ for single gate oxide NMOSFETs [6], [22]. In this work the investigated dual gate oxide PMOSFETs of a $130\mathrm{nm}$ technology for automotive and analog applications have a minimum gate length of $370\mathrm{nm}$ and provide a unique possibility to study the interplay of competing single- and multiple-carrier effects in more detail.

The observed drift compensation takes place after $10^4\mathrm{s}$ of stress at $V_{\mathrm{gs}} \approx -1.75\mathrm{V}$. At this, the corresponding gate voltage is independent of the transistor geometry.

It was ascertained that the main influence of the geometry is an increase of the drift ratio with increasing length between $0.37\,\mu\mathrm{m}$ and $0.5\,\mu\mathrm{m}$ as well as a decrease from $0.5\,\mu\mathrm{m}$ to $2\,\mu\mathrm{m}$ for wide devices (fig. 8). Therefore a maximum of the drift ratio is expected between $0.5\,\mu\mathrm{m}$ and $2\,\mu\mathrm{m}$ for the $10\,\mu\mathrm{m}$ wide channel stressed at room and elevated temperatures.

This means that the single "hot" carrier effect where the particles have sufficient high energies to degrade the device is only relevant for a specific channel length while degradation caused by multiple-carrier mechanisms can be found for shorter as well as for longer devices. The finding is valid for room and elevated temperatures and consistent with our hot-carrier degradation model [24], [25].

Long term stress data (3.6×10^5s) show that even for low gate voltages the drift type $D_{\mathrm{Isub,max}}$ will be compensated by $D_{\Psi,\mathrm{max}}$.

VII. Conclusion

Dual-gate oxide pFETs of a $130\mathrm{nm}$ technology clearly demonstrated two hot-carrier effects which compensate the drift of each other independently of the device geometry. The phenomenon is related to the interaction of single and multiple carrier mechanisms. An additional effect is noticeable after the first multiple carrier induced drift. Transistors stressed for longer than 10^5s show a drift compensation even for low gate voltages. The linear characteristics are mainly influenced by multiple-carrier (high flux) driven mechanisms resulting in a shift to higher absolute potentials. Devices of equal width are expected to have a maximum of the drift ratio $D_{\mathrm{Isub,max}} : D_{\Psi,\mathrm{max}}$ between a length of $0.5\,\mu$m and $2\,\mu$m and show an increase of the drift ratio from $0.37\,\mu$m to $0.5\,\mu$m. The presented findings evidently demonstrate the interplay of single- and multiple-carrier mechanisms of hot-carrier degradation. Most importantly, the results provide a benchmark for device degradation simulations due to the good separability of the observed effects.

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