STT-MRAM-Based Reprogrammable Logic Gates for Large-Scale Non-Volatile Logic Integration

Hiwa Mahmoudi, Thomas Windbacher, Viktor Sverdlov, and Siegfried Selberherr

Institute for Microelectronics, TU Wien, Gußhausstraße 27–29 / E360, A–1040 Wien, Austria
E-mail: {mahmoudi | windbacher | sverdlov | selberherr}@iue.tuwien.ac.at

A new spin-transfer torque magnetoresistive random-access memory (STT-MRAM)-based reprogrammable logic architecture is proposed in order to extend the functionality of the MRAM circuits to perform logic operations. The access transistors of the one-transistor/one-magnetic tunnel junction (1T/1MTJ) cells [1] are used to select simultaneously two or more input MTJs in a first MRAM array and an output MTJ in a second MRAM array - coupled to the first in series - to realize the MTJ-based reprogrammable logic circuits. Compared to the MTJ-based reprogrammable circuits from [2] (Fig. 1a), the 1T/1MTJ-based implementation (Fig. 1b) enables independent access to the input MTJs for STT writing (instead of magnetic-field-based switching) and thus brings significant advantages related to scalability and energy consumption [3], [4]. It will be shown that the non-zero ON resistance of the access transistors decreases the effective TMR of the 1T/1MTJ cells by about 10-20% which increases the error probability by about 20-40%. Therefore, MTJs with high TMR ratio are required for a reliable logic implementation.

The basic Boolean logic operations including AND, OR, NAND, NOR can be executed in two steps including a preset operation (TRUE or FALSE) in the output 1T/1MTJ and then applying a proper voltage level to the bit lines (BLs) of the MRAM arrays. Using the MRAM-based architecture, the output of one operation can be used as the input data for the next logic stage. Thus, arbitrary complex logic functions can be designed by executing a well defined set of subsequent basic operations. The parallelization of several MRAM arrays can be exploited to perform parallel operations on the same word lines (WLs), thus decreasing the number of required serial logic steps and improving the performance. Furthermore, a combination of implication-based IMP/NIMP operations [5] and reprogrammable operations in MRAM arrays can be utilized to realize MTJ-based logic circuits with an optimized number of logic steps, error probability, delay, and power consumption. The performance analysis of different possible designs for a MRAM-based full adder will be presented.

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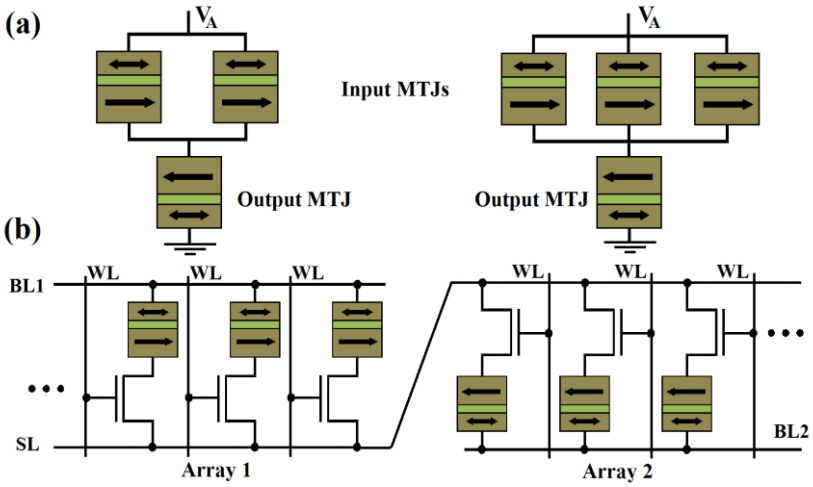

Fig. 1: (a) MTJ-based two- and three-input reprogrammable logic gates [2].
(b) proposed MRAM-based reprogrammable logic architecture.