Modeling of Spin-Based Silicon Technology

Viktor Sverdlov, Joydeep Ghosh, Hiwa Mahmoudi, Alex Makarov, Dmitri Osintsev, Thomas Windbacher, and Siegfried Selberherr
Institute for Microelectronics, TU Wien, Gußhausstraße 27–29/E360, 1040 Wien, Austria
{sverdlov|ghosh|mahmoudi|makarov|osintsev|windbacher|selberherr}@iue.tuwien.ac.at

Abstract—**Electron spin attracts much attention as an alternative degree of freedom for low-power reprogrammable logic and non-volatile memory applications. Silicon appears to be the perfect material for spin-driven applications. Recent progress and challenges in simulating spin-based devices are briefly reviewed. Strain-induced enhancement of the electron spin lifetime in silicon thin films is predicted and its impact on spin transport in SpinFETs is discussed. A new design of the spin-based non-volatile memory cell, MRAM, is presented. By means of micromagnetic simulations it is demonstrated that the new design leads to a reduction of the switching time of the cell. Any two memory cells from a MRAM array can form an implication logic gate. It is shown how by using these gates an intrinsic non-volatile logic-in-memory architecture is realized**.

***Index Terms*—silicon spintronics, spin transport, SpinFET, spin-based memory, spin-based logic**

I. Introduction

The outstanding increase in performance of integrated circuits is achieved by the continuous miniaturization of CMOS devices, however, growing technological challenges [1] and soaring costs are gradually bringing scaling to an end. Research on alternative technologies and computational principles is becoming essential for making devices smaller, faster, cheaper, and more ecologically friendly.

The MOSFET, the main building block of modern integrated circuits, fundamentally operates by employing the charge degree of freedom of an electron. The electron charge interacts with the electrostatic field induced by the gate. The transistor channel can be closed or opened by creating or removing a gate induced potential barrier. Another intrinsic electron property, the electron spin, attracts much attention as a possible candidate for complimenting or even replacing the charge in future electron devices. The electron spin state is characterized by the two possible spin projections on a given axis and thus has potential in digital information processing. In addition, the small amount of energy needed to invert the spin orientation is attractive for low power applications.

Until recently silicon, the main material of modern microelectronics, remained aside the main stream of spin-driven applications. Certainly, the use of silicon for spin devices would greatly facilitate their integration with MOSFETs on the same chip. In addition, silicon possesses several unique properties extremely attractive for spin-driven applications. Nuclei of the ^{28}Si isotope are characterized by zero spin, which favors long spin lifetime. Another source reducing spin lifetime, the spin-orbit interaction, is also weak in silicon. Because of these properties electron spin states of conduction electrons in silicon should live long, which makes silicon a perfect candidate for spin driven device applications.

An outstanding progress in demonstrating the basic elements necessary for spin-related applications, such as injection of spin-polarized currents in silicon, spin transport, spin manipulation, and detection, was achieved recently. A special technique based on the hot electron spin filtering allowed creating an imbalance between the electrons with spins up and down in silicon. Spin transport through an undoped 350µm thick silicon slab [2] has triggered a systematic study of spin transport properties in silicon [3].

II. Spin Transport

For proper functionality of spin-based devices the necessity to transfer the spin information through the channel is essential. While diffusing, the injected spin gradually relaxes to its equilibrium value which is zero in a non-magnetic semiconductor. The lower estimation for the spin lifetime at room temperature obtained within the three-terminal injection scheme was of the order 0.1-1ns [3]. This corresponds to a spin diffusion length - the length at which the spin relaxes - of 0.2-0.5µm.

The spin lifetime is determined by the spin-flip processes [4]. In silicon the spin relaxation due to the Elliot-Yafet mechanism is dominant. The Elliot-Yafet scattering mechanism is mediated by the intrinsic interaction between the orbital motion of an electron and its spin. The microscopic spin-orbit interaction does not commute with the spin and can therefore generate spin flips during scattering. Another contribution is due to a small add-on of an opposite spin projection into the eigenfunction. Thus, spin-independent scattering, for instance with phonons, generates a small but finite probability to flip the spin. A good agreement between the experimentally observed and calculated spin life time as a function of temperature confirms that the Elliot-Yafet mechanism is the dominant spin relaxation mechanism in bulk silicon [5]. The main contribution to the spin relaxation was identified to be due to optical

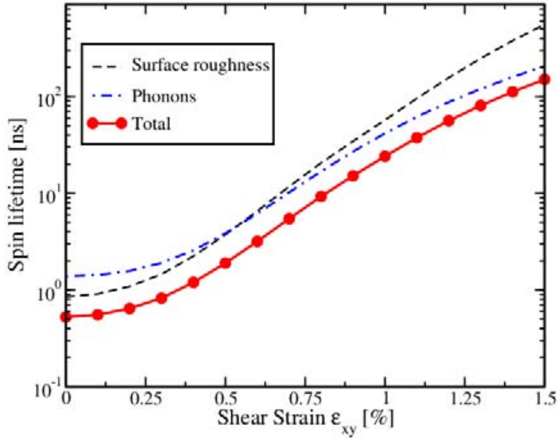

Figure 1. Dependence of total, phonon-, and surface roughness-limited spin lifetime on shear strain for the film thickness 2.1nm, T=300K and concentration 2.6 $10^{12}cm^{-2}$.

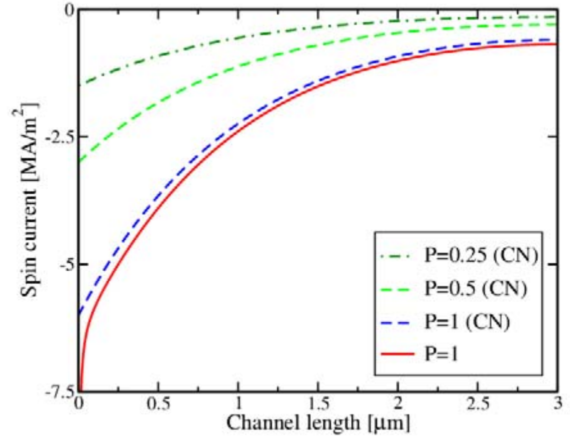

Figure 2. Spin current density at different spin polarizations P, under charge neutrality (CN) condition. One plot is shown considering high charge accumulation.

phonon scattering between the valleys residing at different crystallographic axes [6], [7].

In gated silicon systems and MOSFETs a relatively large spin relaxation [8], [9] may pose an obstacle in realizing spin-driven CMOS compatible devices, and a deeper understanding of fundamental spin relaxation mechanisms in silicon inversion layers, thin films and fins is needed.

The theory of spin relaxation must account for the most relevant scattering mechanisms which are due to the electron-phonon interaction and surface roughness scattering. In order to evaluate the corresponding scattering matrix elements the wave functions must be known. To find the wave functions, an approach based on a **k·p** Hamiltonian appears to be sufficiently rigorous to capture the most important physics. The effective **k·p** Hamiltonian must include the effective spin-orbit interaction which, apart from scattering, is the main ingredient of the Elliot-Yafet spin relaxation mechanism. In addition, a confinement potential must be included. It is also mandatory to have various other effects on the band structure, such as band non-parabolicity, and warping by external stress [10], [11].

For (001) oriented thin films the two relevant valleys along the [001] crystallographic axis are considered. The spin is injected along the Z-axis. The spin relaxation due to surface roughness scattering and electron-phonon interaction is included. The corresponding spin relaxation matrix elements are taken proportional to the square of the product of the subband function derivatives at the interface [12]. The spin relaxation due to the electron-phonon interaction is accounted for in the deformation potential approximation [13].

In unstrained films the two lowest subbands are degenerate [11]. This degeneracy, originating in the Z-valleys' degeneracy, produces a large mixing between the spin-up and spin-down states from the opposite valleys, resulting in hot spin relaxation spots. When shear strain is applied, the hot spots are moved away from the subbands' center and eventually end in the region with no states occupied. This results in a strong reduction of the hot spots' contribution to the spin relaxation. A strong increase of the spin lifetime with shear strain [13] is demonstrated in Figure 1. Therefore, tensile shear strain employed to enhance mobility and on-current in modern transistors can also be used to boost the spin life time in ultra-thin film/ultra-thin box silicon-on-insulator transistors.

III. Spin Injection

The fundamental reason preventing spin injection in silicon and other semiconductors by purely electrical means is an impedance mismatch problem [3]. A solution is to introduce a potential barrier between the metal ferromagnet and the semiconductor. Currently, reliable spin injection in n- and p-doped silicon at room temperature has been demonstrated for a number of ferromagnetic electrodes through several dielectric tunnel barriers [3]. However, there exists a discrepancy of several orders of magnitude between the signal measured and the theoretical value. The signal is larger in the three-terminal measurement setup and the reasons for the discrepancies are heavily debated [3].

Evidence that accounting for the space charge effects at the interface could boost the spin injection by an order of magnitude was recently presented [14]. We found, however, as shown in Figure 2, that in accumulation the spin current is increased only close to the interface. At a distance about the Debye screening length away from the interface the value of the spin current is very similar to that injected at the charge neutrality condition for the same spin polarization [15].

IV. Silicon SpinFET

The SpinFET is a future semiconductor spintronic device with a performance superior to that achieved in

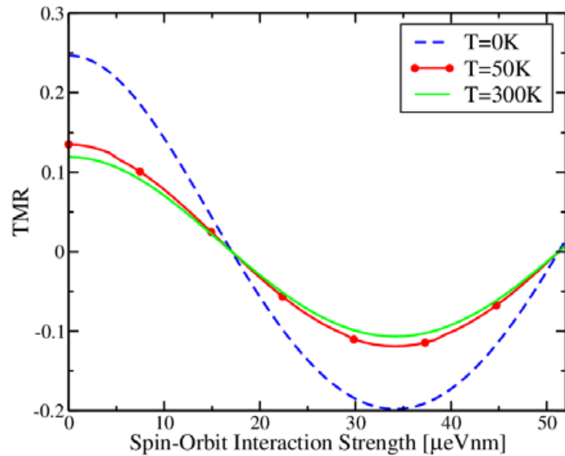

Figure 3. TMR dependence in a Si-based SpinFET on the value of the Dresselhaus spin-orbit interaction for $L = 8\mu m$

the present transistor technology. The SpinFET is composed of two ferromagnetic contacts (source and drain), linked by a non-magnetic semiconductor channel region. Ferromagnetic contacts inject and detect spin-polarized electrons, in analogy to polarizer and analyzer as envisioned by Datta and Das [16]. The current through the device depends on the relative angle between the magnetization direction of the drain contact playing the role of an analyzer and the electron spin polarization at the end of the semiconductor channel. Additional current modulation is achieved by tuning the strength of the effective spin-orbit interaction in the semiconductor region. The strength of the spin-orbit interaction in the channel depends on the effective electric field and can be controlled by purely electrical means applying voltage to the gate.

The strength of the spin–orbit interaction determines the minimum length of the semiconductor channel sufficient to change the orientation of spin to the opposite. Figure 3 shows the tunnel magnetoresistance (TMR) modulation as a function of the spin-orbit interaction strength at different temperatures for parameters typical to silicon. In order to guarantee the nonzero TMR at room temperature, Schottky barriers between the channel and the ferromagnetic source/drain electrodes must be introduced. Unfortunately, because the spin-orbit interaction in silicon is weak, the channel length needed to achieve the TMR modulation is close to a micron [17]. For shorter channels, the only option to realize a SpinFET is to exploit the relative magnetic orientation of the source and drain ferromagnetic contacts [18]. This adds a possibility to reprogram MOSFETs and to obtain a different current under the same drain and gate voltage by changing the drain magnetization orientation. It is important that, once modified, the magnetization remains the same infinitely long without any extra power applied. This property is used in emerging magnetic non-volatile memories discussed in the next section.

V. SPIN-BASED MEMORIES

One of the most promising candidates for future universal memory among emerging technologies is spin transfer torque magnetic RAM (STT-MRAM). The basic element of an STT-MRAM is a magnetic tunnel junction (MTJ), a sandwich of two magnetic layers separated by a thin non-magnetic spacer. While the magnetization of the pinned layer is fixed due to the fabrication process, the magnetization direction of the free layer can be switched between the two states parallel and anti-parallel to the fixed magnetization direction. Switching between these two states occurs due to the spin torque exerted on a free layer by spin-polarized current flowing through the MTJ. The spin-polarized current is only a fraction of the total charge current. A reduction of the current density required for switching and/or the increase of the switching speed without compromising the thermal stability are the most important challenges in this area [19]. The reduction of the switching current is observed in MTJs with perpendicular magnetization [20]. STT-MRAM based on CoFeB-MgO MTJs with interfacial anisotropy is already close to overcoming the scalability limit of charge based storage memories. However, such devices still require reducing damping and increasing thermal stability.

In the MTJ with the monolithic free layer the amplitude of the end domains precession increases when the current starts flowing. However, the central region experiences almost no spin torque and preserves its initial orientation, thus preventing the whole layer from switching its magnetization orientation. This is, however, not the case, when the central region is removed and these domains become virtually independent. Because of that fact a pronounced decrease of the switching time (Figure 4) and current density were recently predicted in a MTJ structure with a composite free layer [21]. The structure also displays a substantial switching time distribution narrowing and can be further optimized for fabrication [22].

VI. SPIN-BASED LOGIC CIRCUITS

Using spin-transfer torque to switch a magnetic tunnel junction is one of the most promising non-volatile storage technologies, which combines the advantages of CMOS compatibility, high speed, high density, unlimited endurance, and scalability. Distributing non-volatile memory elements over the CMOS logic circuit plane can provide extremely low standby power consumption. Recently, MTJ-based implication logic gates have been proposed [23], in which the MTJs are used as the main devices for logical computations and thus intrinsically enable logic-in-memory architectures. The implication logic gates realized in MRAM arrays represent the building blocks of the intrinsic logic-in-memory architecture, where the MTJs are simultaneously used to store and to process the information [24] thus providing the opportunity to proceed beyond the conventional von Neumann computational paradigm.

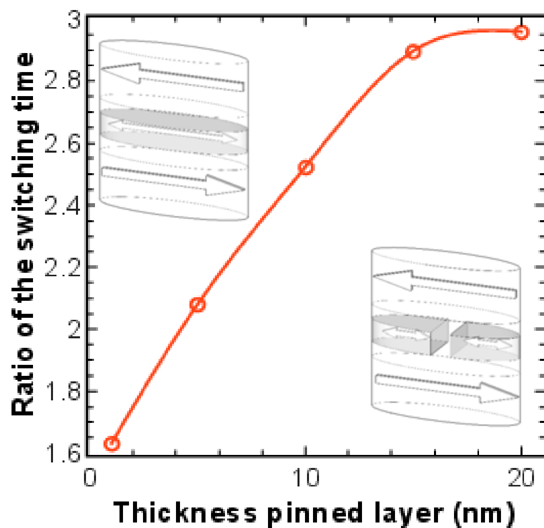

Figure 4. Ratio of the switching time in the monolithic structure (upper inset) to that in the composite structure (lower inset) as function of the thickness of the pinned layer.

VII. CONCLUSION

Because of the recent ground-breaking experimental findings silicon is now gaining momentum to be used in electronic applications involving spin. Mechanical stress routinely used to enhance the electron mobility can also be used to boost the spin lifetime. An efficient coupling between the electrical and the magnetic degrees of freedom makes STT-MRAM a viable candidate for future universal memory which is fast, non-volatile, and CMOS compatible. Building implication logic gates from STT-MRAM cells opens the way towards intrinsic logic-in-memory architecture where the same elements are employed to store and to process the information.

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