Magnetic Tunnel Junctions for Future Memory and Logic-in-Memory Applications

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Extended Abstract

Memories based on charge storage are gradually approaching the physical limits of scalability, and the search for new memory technologies using alternative storage principles has accelerated. Apart from good scalability, a new type of memory must exhibit low operating voltages, low power consumption, high operation speed, long retention time, high endurance, and a simple structure. Magnetoresistive random access memory (MRAM) switched with spin-transfer torque (STT) is a promising candidate for future universal memory. Currently, 64Mb STT-MRAM memory arrays are commercially available. The basic memory element is a magnetic tunnel junction (MTJ), a sandwich of two ferromagnetic layers separated by an oxide, typically MgO. The magnetization direction of the free layer can be switched between the two stable orientations parallel or anti-parallel to the magnetization direction of the second, pinned layer. The MTJ resistance depends on the magnetization configuration of the layers and facilitates the reading of the stored binary data. STT-MRAM combines the speed of SRAM, the density of DRAM, and the non-volatility of flash memory, and has thus all the characteristics of a universal memory. However, the reduction of the switching current density and/or the switching time while maintaining a high thermal stability is currently the main challenge for the memory cell.

We demonstrate that a substantial decrease of the switching time in in-plane magnetic tunnel junctions can be achieved by a special design of the free magnetic layer. The idea is to remove the portion of the central region of the free layer along the short cross-section axis. The end domains become virtually decoupled, which results in a substantial switching time and current reduction. The switching becomes more homogeneous with a very narrow distribution of switching times as compared to the standard MRAM structure. Most importantly, the magnetizations of both ends and, therefore, the total magnetization remains in-plane during switching. Thus, the switching proceeds through the state with the minimum energy barrier separating the two equilibrium magnetization states. We conclude that the proposed in-plane STT-MRAM cell with the composite free layer ensures the switching and thermal barriers to be the same guaranteeing fast switching in the MTJ with the composite free layer. Several new geometries with improved characteristics suitable for fabrications are also introduced and optimized.

The designed non-volatile memory element is promising for applications in STT-MRAM arrays. STT-MRAM is one of the most promising non-volatile storage technologies, which combines the advantages of CMOS compatibility, high speed, high density, unlimited endurance, and scalability. Distributing non-volatile memory elements over the CMOS logic circuit plane (logic-in-memory architecture) can provide extremely low standby power and instant start-up by holding the information in the MTJs and eliminating the need for refreshing CMOS-based memory elements. Introducing non-volatility into logic circuits is critical to reduce the standby power and enables instant-on applications. However, in hybrid CMOS/MTJ circuits the MTJs are used only as ancillary devices which store the computation results. Therefore, sensing amplifiers are required for reading the data at each logic stage and to provide the next stage an appropriate voltage or current signal as input. This limitation increases the device count, delay, and power consumption. Furthermore, the generalization to large-scale logic systems is problematic.

Recently, circuits for logic applications based entirely on MRAM cells were demonstrated. The logic operations are implemented by using reprogrammable- and material implication-based logic gates providing a new intrinsic logic-in-memory computational platform. Performing logics on the memory elements enables a stateful logic framework which by definition extends the use of memory elements to information processing. Therefore, in stateful logic the same magnetic tunnel junction serves simultaneously as a logic gate and a latch. The key idea to implement stateful logic gates in standard MRAM arrays is to exploit the access transistor of a memory cell as a voltage-controlled resistor. The proposed implication memory-based logic framework is more efficient and reliable as compared to conventional reprogrammable logic. The stateful logic provides non-volatile logic fan-out and enables highly delocalized computation executions. The MRAM-based logic is well suited to perform parallel non-volatile large scale computations on a platform going beyond the Von Neumann architecture.

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