Modeling Spin-Based Electronic Devices

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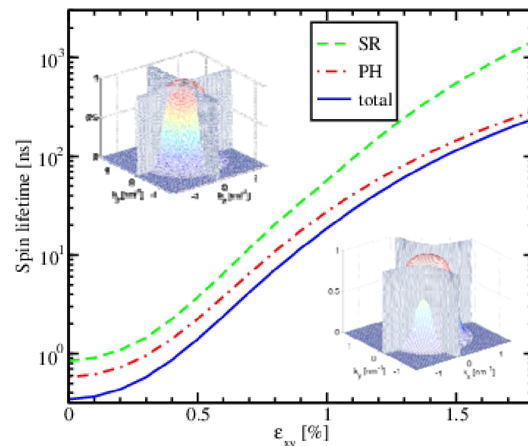
The electron spin possesses several exciting properties suitable for emerging devices: It is characterized by only two projections on an axis and can change its orientation rapidly by utilizing an amazingly small amount of energy. Employing spin opens new exciting opportunities for developing conceptually novel non-volatile nanoelectronic devices for future low power applications [1]. The spin field-effect transistor (SpinFET) proposed by Datta and Das [2] employs the gate voltage-dependent spin-orbit interaction to modulate the current in the channel. For a practical realization of a SpinFET it is mandatory to guarantee spin injection, propagation, manipulation, and detection [3]. Electrons in bulk silicon, the main material of microelectronics, are subject to a very weak spin-orbit interaction which results in a long spin lifetime [4]. Close to the interface the spin diffusion length and relaxation time at room temperature appear to be shorter with much weaker temperature dependence compared to the bulk [5]. Thus, methods to boost the spin lifetime in MOSFETs are needed. We utilize a spin-dependent **k·p** Hamiltonian [6] for investigation of potential methods. Without strain the unprimed subbands are degenerate. By lifting this degeneracy spin-orbit interaction produces a large mixing between the spin-up and spin-down states from the opposite valleys, resulting in hot spots characterized by strong spin relaxation [7] shown in the upper-left inset of the figure. In strained samples these hot spots are pushed to higher energies outside of the occupied states (lower-right inset), thus reducing spin relaxation at higher shear strain. Therefore, shear strain used to enhance the on-current in n-channel MOSETs can also be used as an efficient spin lifetime booster [7].

Although many interesting ideas to build spin-based devices have been introduced [8-13], much more efforts are required to bring them to practical applications. To make new devices commercially successful, one has to fulfill several important requirements. Room temperature operation, compatibility with CMOS, and non-volatility are the properties desired most. Although significant progress in understanding spin injection, transport, and detection in silicon has been achieved, more research is urgently needed to enhance the spin injection efficiency at room temperature and to resolve the issue of spin manipulation by pure electrical means. Albeit many exciting inventions are lying ahead on this trilling path, the viable practical option for the near future is to benefit from using magnetic tunnel junctions (MTJs). MTJ-based spin transfer torque (STT) magnetic RAM is CMOS compatible, non-volatile, and nearing production. Arrays made of 1MTJ/1Transistor cells open new opportunities to develop intrinsic non-volatile logic-in-memory systems [14]. One of the most important issues in modern STT-MRAM is the reduction of the switching current and/or switching time while at least preserving or, as is highly desired, increasing the thermal stability factor [15]. Careful structural optimization of MTJ architecture and materials is paramount for an ultimate STT-MRAM success. Magnetic tunnel junctions with a composite free layer demonstrate a three-fold switching time reduction at the same current as compared to the monolithic structures, without compromising on the thermal stability factor [16]. Composite MTJ structures are promising for building efficient STT oscillators [17].



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