Effects of Sidewall Scallops on Open Tungsten TSVs

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***Abstract*—In order to examine the effects of sidewall scallops on through-silicon via (TSV) performance, the etch processes required to generate several TSV geometries are simulated and the resulting structures are imported into a finite element tool for electrical parameter extraction and reliability analysis. The electrical models, which were confirmed using experimental measurements with non-scalloped structures, are applied to the simulated TSV devices. The effects of the scalloped features are investigated by comparing the performance of a TSV with scalloped sidewalls to one with flat walls. In addition, the variation in TSV performance, when the sidewall scallop height is varied, is analyzed. A link between increased scallop height and increased resistance and signal loss is observed. The maximum thermo-mechanical stress in the structure is also noted to increase with the presence of large scallops, but the overall average stress does not vary significantly.**

I. Introduction

In order to advance processing technology along the desired Moore's Law [1] path, the microelectronics manufacturing industry has aggressively scaled devices with "more Moore" integration over the last decades. However, the increased process equipment and factory costs for scaling are expected to limit scaling at the 6nm node [2]. Due to these scaling limitations, a great amount of effort has recently been directed towards adding more functionality to applications beyond memory and logic, deemed "more than Moore" integration. A major development in this direction is the through-silicon via (TSV), a three-dimensional integration technology which allows for the fabrication of systems connecting various technologies, dense device packing, lower power consumption, and reduced RC delay [3].

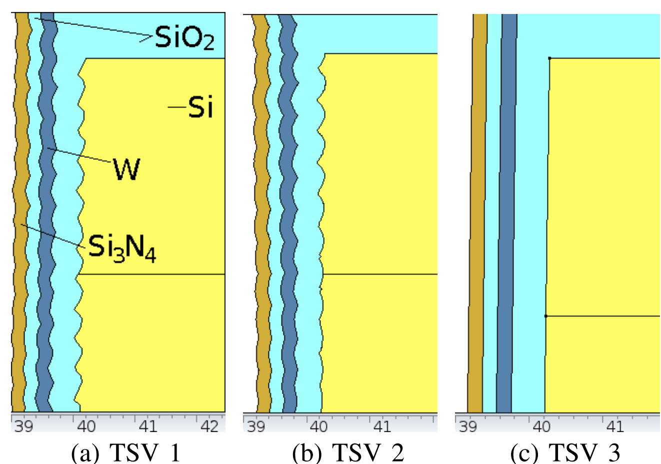
A sequence of several sensitive processing steps are required in order to generate a TSV with a desired size and aspect ratio. In addition to the deposition of insulation and conducting materials, a method to etch vertical wells through a silicon wafer is required. Modern efforts to etch highly vertical TSVs result in scalloped TSV sidewalls, which could affect the TSV performance and reliability [4]. This work compares, through simulations, the electrical and reliability properties of open tungsten TSVs with a diameter of approximately 80μm and a geometric aspect ratio of 1:3. An analysis of the effects of scalloped sidewalls on TSV performance is also performed. The TSV performance is evaluated by measuring the thermo-mechanical stress after a 300K temperature drop and by observing the electromigration (EM) induced stress when a 1A current is applied through the structure. In addition, the electrical parameters and signal loss of the TSV are calculated, allowing for further small signal analysis. A non-scalloped structure with the same size and aspect ratio has previously been used in order to extract model parameters which successfully replicate experimental measurements in [5]. A similar study has been performed for filled TSV where the etched hole is filled using electromechanical deposition of copper [6]. This work deals with TSVs which are manufactured by depositing a layer of tungsten on the etched sidewalls using CVD processes.

II. Effects of the Presence of Sidewall Scallops on TSV Performance

In order to generate the TSV profiles, an in-house process simulator is used. The simulator is implemented using the level set framework and it is capable of simulating a sequence of processing steps, including etching and deposition. The initial step of generating the TSV profile is the etching of the silicon wafer. In order to perform high aspect ratio etching simulations, alternating passivation and etching cycles are required.

A. Process Simulations for TSV Generation

In order to generate the required TSV structures, two simulation methods are implemented, resulting in two different etch profiles, named as TSV 1 and TSV 2 in Fig. 1(a) and Fig. 1(b), respectively. The presented etch rates and etch rate ratios are a slightly modified version of those published in [6] and are given as a guideline to simulating highly vertical walls during an etch process.



(a) TSV 1 (b) TSV 2 (c) TSV 3

Fig. 1. Two-dimensional view of the top of TSV structures, used to analyze the effects of scallop presence on TSV performance.

1) TSV 1 - Ideal Etch and Deposition Models: The simulation models implemented in order to generate TSV 1 from Fig. 1(a) include a polymer deposition at the beginning of each cycle using an isotropic rate of 10nm/second for 4 seconds.

The combination of isotropic and anisotropic/directional rates required for the polymer and silicon etching is the second step in each cycle and the simulation parameters for this step are shown in Table I. A total number of 110 intermittent deposition/etch cycles are required in order to etch the desired depth of 250μm, resulting in a total etch time of 28 minutes and an etch rate of approximately 9.0μm/minute.

2) TSV 2 - Coupled Monte Carlo Method: An additional transport model, suggested in [7], which uses the ray tracing technique in order to compute the ion and neutral fluxes at the silicon, mask, and polymer surfaces during the intermittent deposition and etching steps is implemented. This model is implemented in order to generate TSV 2 from Fig. 1(b) and the initial deposition step is performed for a duration of 4 seconds in a CF_x environment with ion and neutral fluxes of $3.125 \cdot 10^{15}$atoms/(cm^2·s) and $2 \cdot 10^{18}$atoms/(cm^2·s), respectively. The etch step of the cycle is performed in a SF_6/O_2 environment using a model described in [8]. The neutral and ion fluxes used for this step are given in Table I. This simulation results in the appearance of scallops only at the top of the etched hole and after approximately 10-15 cycles. After the scallops flatten, the profile is assumed to be straight down to the TSV bottom.

3) Deposition of Additional Layers: The deposition of the isolation oxide (SiO_2), the thin tungsten (W), the liner oxide (SiO_2), and the silicon nitride (Si_3N_4) layers is performed using a ray tracing technique which results in material thicknesses of 500nm, 200nm, 200nm, and 200nm, respectively. The profile for TSV 3 from Fig. 1(c) has been generated by drawing a geometry which contains no scallops on the sidewalls, but has the same geometric aspect ratio and overall sidewall tapering noted in TSV 1 and TSV 2.

B. *TSV Performance in the Presence of Scallops*

The electrical performance, the signal loss calculated through S-parameter extraction, the thermo-mechanical stress, and the electromigration reliability of the structures are analyzed after importing the finalized geometries into a finite element environment. The models used to extract the electrical behavior have been proven against experimental results given in [5]. Fig. 2 shows the TSV resistance (R_{TSV}), inductance (L_{TSV}), and capacitance (C_{TSV}) of the three TSVs. The resistance is highest for the TSV which has defined scallops along the entire length of the device, while the other two TSVs have a relatively equal resistance, with a slightly higher value for TSV 2.

The frequency-dependent capacitance is plotted in Fig. 3, where it is evident that the slight difference in capacitance observed at low frequency operation does not carry through when the device is operating at high frequencies.

The signal loss through the TSVs has also been analyzed using S-Parameter extraction, where the TSV is viewed as a 2-port system with the input signal between the W top and bulk Si and the output signal between the Al bottom and bulk Si. The signal loss is found by calculating S21 as plotted in Fig. 4 (top). Little to no variation can be noted due to the presence of scallops along the TSV sidewalls.

Additionally, the structure with sidewall scallops appears to have the highest thermo-mechanical stress at material interfaces after a temperature drop of 300K is imposed on

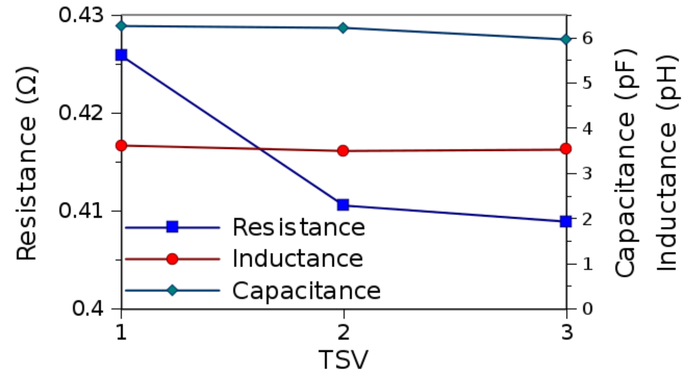


Fig. 2. Electrical parameters (R_{TSV}, L_{TSV}, and C_{TSV}) dependence on sidewall scallops for the tested TSVs.

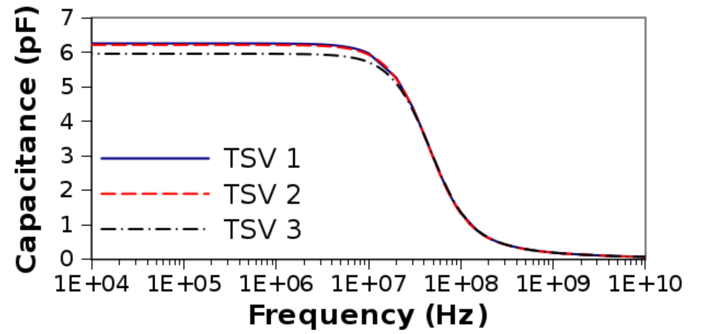


Fig. 3. Frequency dependence on the TSV capacitance for the TSVs from Fig. 1.

the structures, shown in Table III and Table IV. The strain reference temperature is set to 593K with a drop to 293K and no residual stress is included in the simulation. The stress is generated due to the materials having different coefficients of thermal expansion (CTE). However, when the stress through the silicon is observed in Fig. 5, the three TSVs show very minor variation. This result suggests that for this type of TSV, the presence of scallops neither helps nor hinders the generation of stress due to ambient thermal variation and that the keep-out zone (KOZ) of the TSVs remains unchanged.

The EM-induced stress (σ_{max}^{EM}) in the bottom aluminum layer after 1 year of operation at a current of 1A is shown in Fig. 6(b), where a two-dimensional cut through the TSV bottom is depicted. In Fig. 6(a), the current density ($J_{Al/W}$) during operation is shown. The difference between the EM-induced stress with and without the scalloped sidewalls is insignificant, as can be observed in Fig. 7. This is an expected result, as aluminum is much more sensitive to electromigration failure than tungsten, while the aluminum layer is unaffected by the presence of scallops.

III. Effects of Scallop Height on the Performance of TSVs

In order to evaluate the effects of scallop height on TSV performance, several TSVs have been generated using a level set simulator. An etch model is implemented, which performs several cycles of polymer deposition followed by polymer and silicon etching in order to generate a highly vertical well in the silicon wafer. Four TSVs are generated, each with

TABLE I. ETCH PARAMETERS - TSV 1 AND TSV 2 SIMULATION.

TSV 1 - Constant Rates		TSV 2 - Monte Carlo & Ray Tracing	
Isotropic rate	39 nm/second	F flux	$1.0 \cdot 10^{19}$atoms/(cm^{2}s)
Directional rate	20 nm/second	Ion flux	$6.0 \cdot 10^{15}$atoms/(cm^{2}s)
	Etch time per cycle	11.2 seconds (110 total cycles)	
	Si:mask etch ratio	80:1 isotropic and directional	
	Si:polymer etch ratio	13:1 isotropic / 2:1 directional	

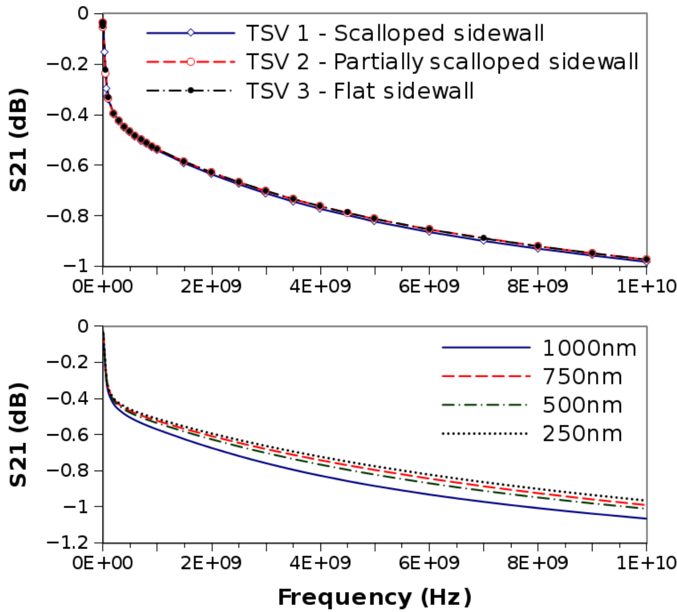


Fig. 4. Signal loss S21 (db) through the TSVs depicted in Fig. 1 (top) and Fig. 8 (bottom). The results suggest that only large scallops cause a deviation from the flat sidewall behavior.

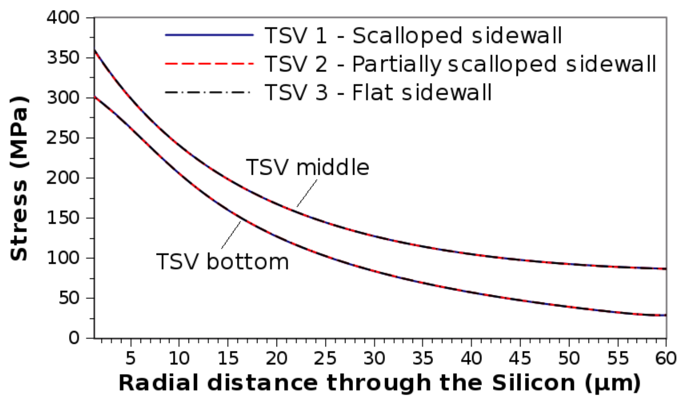
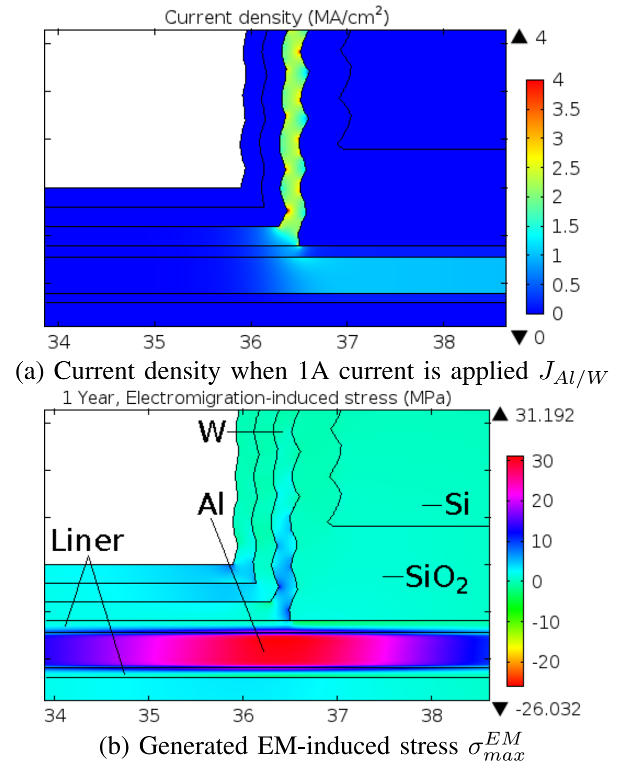


Fig. 5. Von Mises stress through the silicon, radially moving away from the TSV through the middle (125μm) and the bottom (240μm) of the devices from Fig 1.



(a) Current density when 1A current is applied $J_{Al/W}$

(b) Generated EM-induced stress σ_{max}^{EM}

Fig. 6. Two-dimensional view of TSV 1 bottom.

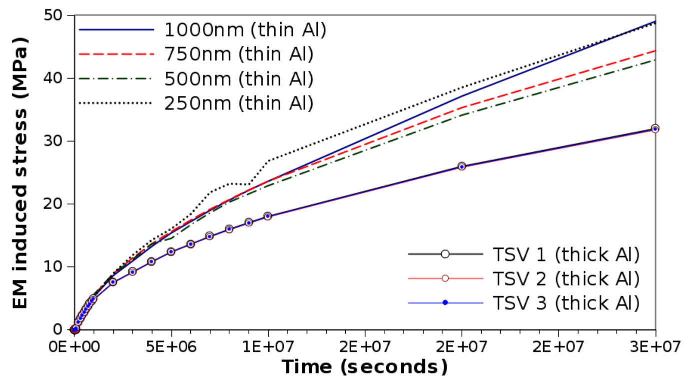


Fig. 7. EM-induced stress build-up with time through the aluminum layer for devices with varying scallop heights and aluminum layer thicknesses. The thick Al layer is approximately 25% thicker than the thin Al layer.

different heights of sidewall scallops. The generated structures are then imported into a finite element simulator, where their electrical performance, signal loss, thermo-mechanical stress, and electromigration-induced stress are analyzed.

A. *Process Simulation for TSV Generation*

In order to analyze the effects of the height of the sidewall scallops on the TSV performance, four different simulations are performed using the same deposition and etch rates, while varying the duration of the deposition and etch cycles. The polymer deposition and silicon etch durations for each cycle have been varied in order to generate a variation in scallop heights, as shown in Fig. 8. Similar to the previous section, the etch rates and ratios presented here are a slightly modified

version of those published in [6] and are given as a guideline to simulating highly vertical walls during an etch process.

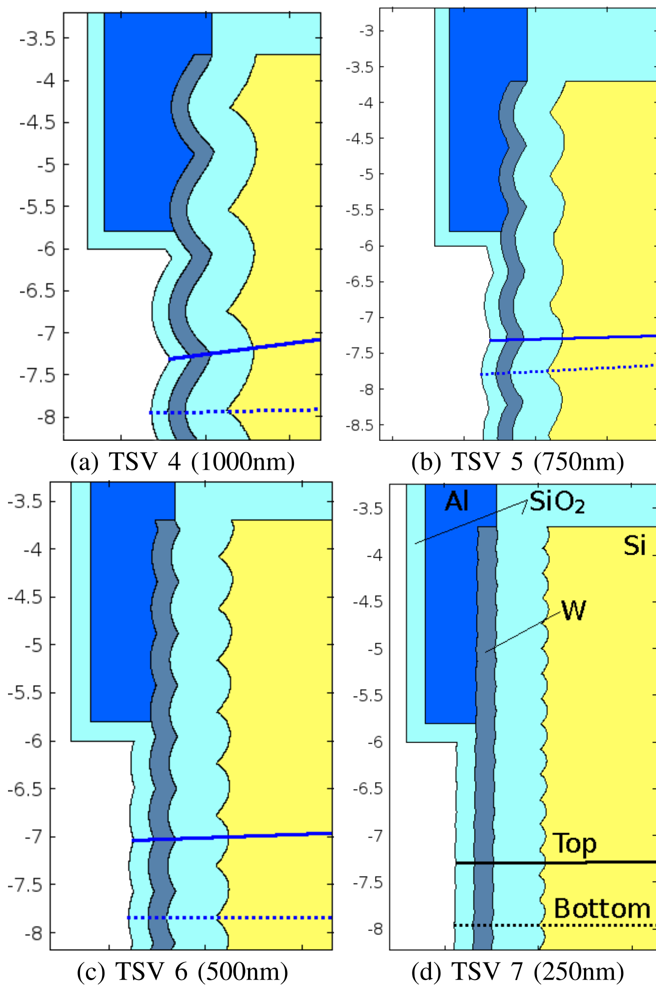


Fig. 8. Two-dimensional view of the top of TSV structures, used to examine the effects of varying scallop height on TSV performance.

Table II summarizes the simulation parameters implemented in order to generate the required TSV geometries. The TSVs have a diameter of approximately 80μm and an aspect ratio of 1:3. Following the etch simulation, layers of isolation oxide (SiO_2), tungsten (W), and liner oxide (SiO_2) are deposited using constant rates in order to generate material thicknesses of 500nm, 200nm, and 200nm, respectively. A layer of aluminum metal is used for top and bottom contacts of the TSV. The tops of the generated structures TSV 4, TSV 5, TSV 6, and TSV 7 are shown in Fig. 8(a), (b), (c), and (d), respectively, where the variation in scallop heights is evident. The total time to etch the full depth of the TSVs (250μm) is approximately one hour, with an overall etch rate of about 4.2μm/min.

B. Dependence of Scallop Height on TSV Performance

The variation of the resistance through the TSV (R_{TSV}) for varying scallop heightss is shown in Fig. 9. It is evident that the TSV with the largest scallops also has a significantly larger R_{TSV} due to the extended length of the W layer because of the large bending introduced by the scallops.

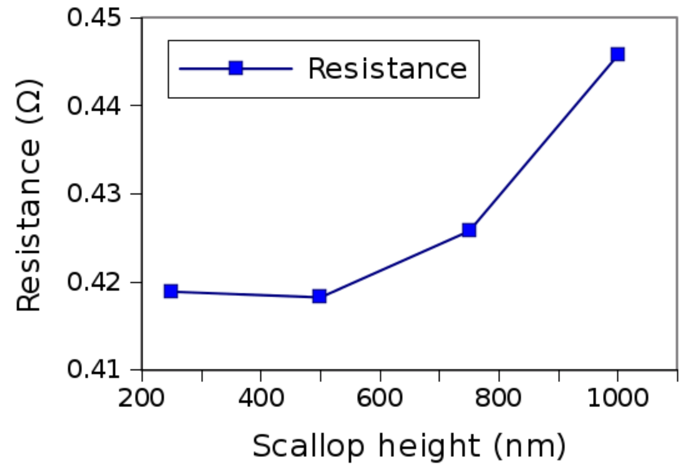


Fig. 9. Resistance through the TSV (R_{TSV}) dependence on sidewall scallop height for the tested TSVs

The variation of the TSV parasitic inductance (L_{TSV}) and capacitance (C_{TSV}) as the scallop height is varied, is plotted in Fig. 10. It is evident that the effect is not as noticeable as for the TSV resistance. However, there is a slight trend of increasing L_{TSV} and C_{TSV} with increasing scallop height. The capacitance is mainly governed by the deposition of the isolation oxide layer, while the inductance is thought to have a relationship with the amount of tungsten metal present in the TSV. The increased amount of tungsten, due to the curved nature of the sidewalls with large scallops, explains the increased inductance noted in Fig. 10.

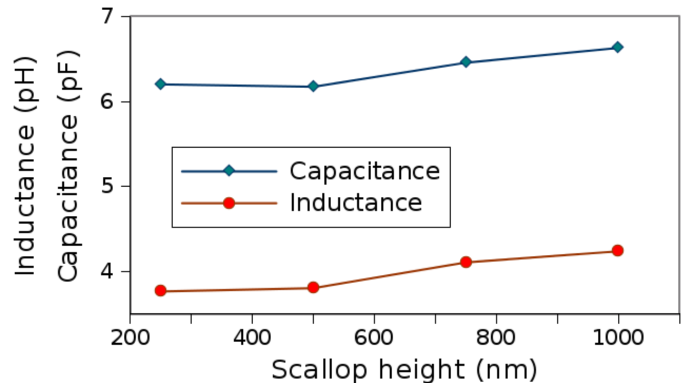


Fig. 10. Parasitic inductance (L_{TSV}) and capacitance (C_{TSV}) dependence on sidewall scallop height for the tested TSVs.

The signal loss through the TSVs, analyzed using S-parameter simulations is shown in Fig. 4 (bottom), where it is clear that the high-frequency loss is increased for the TSV with the largest scallop height (TSV height of 1000nm). Fig. 11 shows the frequency-dependent capacitance behavior of the generated TSVs. It is once again evident that scallop height plays no role in the high-frequency capacitance, while the low-frequency and DC performance varies according to scallop height.

Similar to the previous test of thermo-mechanical stress, a thermal drop of 300K was applied to the structures with varying sidewall scallop heights and the effects on the stress

TABLE II. ETCH PARAMETERS - TSV 4, TSV 5, TSV 6, AND TSV 7 SIMULATIONS, RESULTING IN TSVS WITH SCALLOP HEIGHTS OF 1000NM, 750NM, 500NM, AND 250NM, RESPECTIVELY.

	Rate	Etch Ratio		Cycle Time (sec) TSV 4	TSV 5	TSV 6	TSV 7
Polymer deposition	10nm/s	-	-	4.8	3.6	2.4	1.2
Silicon etch (isotropic)	120nm/s	Si:mask	27:1	12	9	6	3
		Si:polymer	40:1				
Silicon etch (directional)	50nm/s	Si:mask	85:1				
		Si:polymer	9:1				
Total number of cycles:				209	338	466	931
Resulting scallop height:				1000nm	750nm	500nm	250nm
Resulting scallop width:				300nm	230nm	150nm	75nm

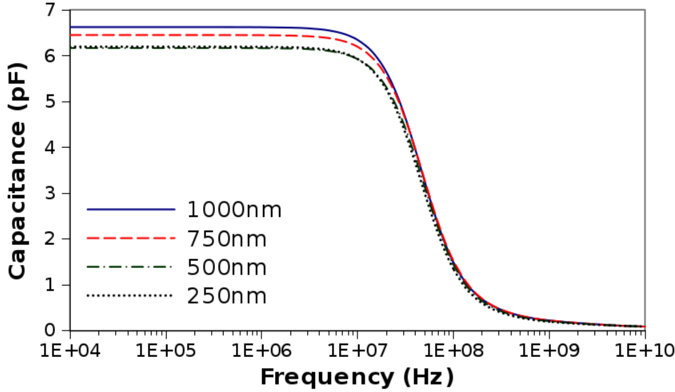


Fig. 11. Frequency dependence on the TSV capacitance for the TSVs from Fig. 8.

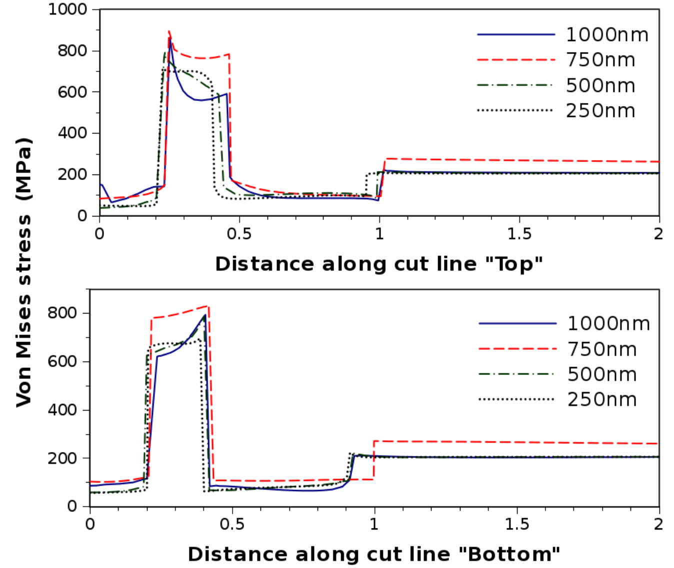


Fig. 12. Von Mises stress through the top and bottom one-dimensional cut lines from Fig 8. The highest stress build-up is noted in the tungsten layer.

build-up at material interfaces was noted in Table III and Table IV. From the results, it can be concluded that the thermo-mechanical stress at the SiO_2/W interface is increased by the introduction of the scallops. There is additionally a significant increase of stress at the outer interface between the SiO_2 liner and ambient. Additional analysis of the stress is performed by plotting one-dimensional radial cut lines through the device at the locations where scallops meet, which is shown to have the highest stress levels. The locations of the cuts are depicted in Fig. 8 and the resulting stresses through those lines are shown in Fig. 12. The highest stress is noted in the tungsten layer, while the height of the sidewall scallops does not seem to play a significant role in determining the stress levels. It is noted that the overall stress through the device does not change significantly, but the stress has a higher peak at the location where two large scallops meet as compared to the contact point between two smaller scallops. Therefore, these meeting points are at a higher risk for potential stress-induced failure and the region must be treated carefully to avoid metal cracking, while ensuring proper metal sticking to the SiO_2 layer is essential.

The electromigration-induced stress (σ_{max}^{EM}) in the bottom aluminum layer after 1 year of operation at a current of 1A is shown in Fig. 13(b), where a two-dimensional cut through the TSV bottom is shown. In Fig. 13(a), the current density ($J_{Al/W}$) during operation is shown. The variations observed in Fig. 7 do not appear consistent with variations in scallop heights. The noted differences are more likely to be due to variations in mesh refinement for the different TSVs. However, the difference in the EM-induced stress when a thinner aluminum layer is used on the TSV bottom is noticeable. The thick aluminum is approximately 25% thicker than the thin alternative and it results in approximately 50% more EM-induced stress, shown in Fig. 7. This once again reinforces the previous observation that the aluminum layer, which is unaffected by scallops, is the one which is prone to electromigration failure.

IV. CONCLUSION

The effects of sidewall scallops and their height on the electrical performance and stress generation for an open tungsten TSV have been analyzed. The geometries for the tested TSVs have been generated using an in-house level set-based process simulator by performing alternating passivation and etching cycles. The resulting TSV geometries have been imported into a finite element simulator, where the TSVs' performances have been analyzed and compared.

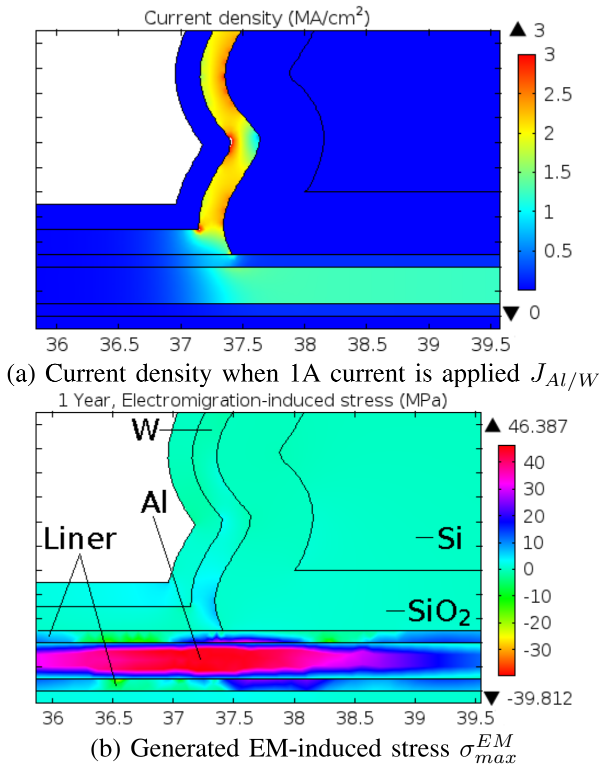
The electrical performance of the TSVs is in agreement with experimental measurements performed on a non-scalloped structure. The presence of scallops introduces an increased TSV resistance, while increasing the scallop height results in a further resistance increase. The parasitic inductance and

TABLE III. MAXIMUM THERMAL STRESS AT MATERIAL INTERFACES.

	Maximum von Mises Stress (MPa)						
Interface	**TSV 1**	**TSV 2**	**TSV 3**	**TSV 4**	**TSV 5**	**TSV 6**	**TSV 7**
Si/SiO_2	377	329	329	509	436	451	571
SiO_2/W	1517	856	856	914	1121	1208	1132
W/SiO_2	1620	720	720	1173	1288	1186	1308
SiO_2/Ambient	-	-	-	733	300	183	206
SiO_2/Si_3N_4	661	447	447	-	-	-	-
Si_3N_4/Ambient	832	547	548	-	-	-	-

TABLE IV. AVERAGE THERMAL STRESS AT MATERIAL INTERFACES.

	Average von Mises Stress (MPa)						
Interface	**TSV 1**	**TSV 2**	**TSV 3**	**TSV 4**	**TSV 5**	**TSV 6**	**TSV 7**
Si/SiO_2	228	221	221	229	236	230	230
SiO_2/W	557	534	533	559	591	554	544
W/SiO_2	559	540	539	554	586	556	548
SiO_2/Ambient	-	-	-	131	120	109	108
SiO_2/Si_3N_4	298	295	295	-	-	-	-
Si_3N_4/Ambient	490	488	487	-	-	-	-



(b) Generated EM-induced stress σ_{max}^{EM}

Fig. 13. Two-dimensional view of TSV 7 (750nm) bottom.

capacitance of the devices display a similar pattern, but the effects are much smaller. The signal loss, measured using S-parameter extractions, is noticeably higher for the TSVs with the largest scallops, but is otherwise relatively unchanged when small scallops are introduced.

The thermo-mechanical stress at the TSV's interface with the ambient is highest for the TSV with the largest scallops. Additionally, the locations where two scallops meet is prone to very high stresses due to the pinch-off caused by the scallops' attempts to expand during a drastic change in temperature.

The electromigration-induced stress, however, affects the bottom aluminum layer and not the sidewall tungsten itself. Therefore, it is the thickness of this layer which determines the EM reliability of the TSV. Changing the shape, thickness, and scallop pattern of the tungsten itself is not expected to influence the electromigration response. It was noted that a thinner aluminum layer resulted in an increased current density which directly increased the electromigration-induced stress.

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