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ユーザーフレンドリーなGUIを有する3次元配線容量／電流密度シミュレーションシステムの開発

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あらまし:　今日のLSIの微細化に伴い、高密度配線を実現するためにはLSI設計時に配線容量を正確に見積もったり、また配線のコンタクトやビアホールにおける信頼性確保のために電流密度を正確に見積もることが不可欠である。これを可能とするために非常に使い安いGUIを有する3次元配線容量／電流密度シミュレーションシステムを開発した。これにより、ユーザーはスクリーン上でインタラクティブに3次元データを表示させながら配線データを簡単に入力作成できる。このユーザーフレンドリーなシステムにより入力工数が従来に比べて数パーセントに短縮できた。さらにこのシステムは入力の複雑さの為に取扱いが従来不可能であった複雑な構造の入力及びシミュレーションを可能とした。

キーワード:　3次元、容量、電流密度、信頼性、シミュレーション、GUI

The Simulation System for Three-Dimensional Capacitance and Current Density Calculation with a User Friendly GUI

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Abstract:　For the realization of today's wiring miniaturization, it is necessary to take into account the interconnect wiring capacitance for LSI designing and the current density distribution in a line or contact/via holes to achieve reliability. This system enables users to construct wiring data, displaying 3-dimensional graphics on the screen, interactively. Due to this interface with easy and flexible operation capability, TAT has been reduced to a few percent compared to the original. Furthermore, this system can also be applied to the wirings of complex structures, for which until now it was almost impossible to simulate due to the huge amount of tedious data input work required.

key words:　three-dimensional, capacitance, current density, reliability, simulation, GUI

1. Introduction

According to today's wiring miniaturization, it is required to accurately estimate the interconnect wiring capacitance and the current density, which has not been so far adequately accomplished. Firstly, correct prediction of wiring capacitance is necessary to evaluate switching speed, delay of signal and cross-talks. Wiring capacitance can be classified into wire-to-ground capacitance and wire-to-wire capacitance. For conventional processes, wire-to-wire capacitance could be ignored because the distance between wires was large and its magnitude was relatively small compared with wire-to-ground capacitance. However, as the process advances, the distance between wires becomes very small, and wire-to-wire capacitance cannot be neglected. Secondly, from the aspect of wiring reliability the concentration of the current density distribution generates heat and might cause electromigration resulting in failure there. Therefore the precise prediction of current density is also necessary to maintain reliability.

We developed SENECA, a three-dimensional simulation system capable of very easily simulating wiring capacitance and current density for practical complex structures[1].

2. Simulation System SENECA

SENECA consists of three modules: the input interface SCIN, the numerical calculation part SCAP [2][3] which utilizes a three-dimensional finite element approach for the computation of wiring capacitances and current densities, and the output processor and viewer SCOUT.

The input data for SCAP consists of coordinate points and permittivity information of every hexahedron which is obtained by sectioning the object into small pieces, and the location information of electrodes. In case of practical applications, sectioning objects into hexahedrons by hand is almost impossible because the number of hexahedrons for practical objects soon reaches the order of a thousand or more. In order to resolve this problem, we developed a graphical input interface called SCIN, which enables to construct complex input structures accurately and very efficiently with very easy interactive operation

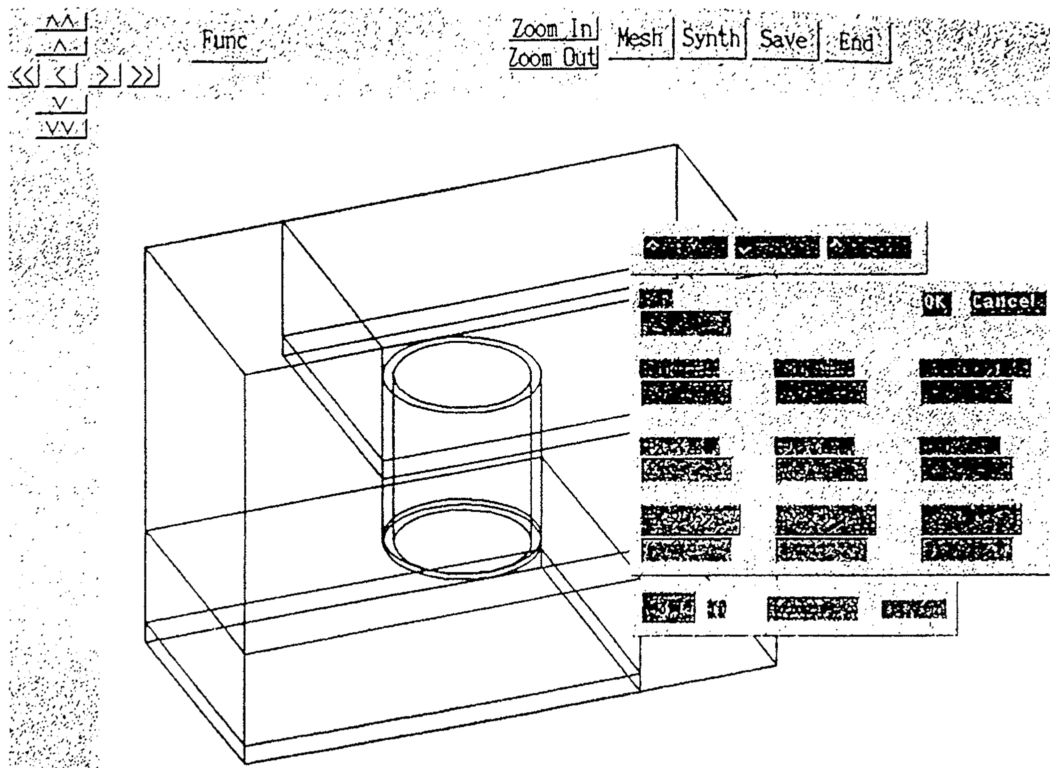

Fig.1 Input example for contact hole using SCIN

as shown in Fig.1. As one important feature of SCIN, rectangular parallelepiped, cylinder and spoon-cut, which are the structures used in wirings, are prepared as built-in models of input data, and the desired structure can be created by combining those built-in models and specifying parameters. Thus a defined input structure can be subsectioned into hexahedron meshes automatically and it generates thereby the input data for three-dimensional finite element numerical analysis. The realization of this graphical input interface made it possible to reduce the man power from more than three days work to less than 30 minutes for a practical structure.

SCAP can calculate three-dimensional wiring capacitances and current densities using finite element analysis. The three-dimensional Laplace equation is solved for the input configuration specified with SCIN. Tetrahedrons are used for discretization with quadratic shape functions leading to 10 parameters per element. Hexahedrons are decomposed automatically to tetrahedrons.

SCOUT, the output processor, calculates electric field, current density, generated heat from the current flow, and plots colored mapping and also vector representations. It can show any cross sections on the three-dimensional object, partial enlargement on any specified part, and print out with very simple button operation.

3. Evaluation and Practical Applications of SENECA

In order to investigate the interconnect capacitances between lines and between line and ground, SENECA was applied to the three kinds of processes A(0.7μm rule generation), B(0.5μm rule generation), C(0.35μm rule generation). Firstly, the detailed comparison is made on process B between experiments and simulations for the configurations as shown in Fig.2. Table 1 gives some of the results showing quite good agreement of 10% difference or less. Shown in Fig.3 are the structures and dimensions of process A, B, C, respectively. In Table 2, the ratio is shown of the capacitance between wires and between wire and ground. As the process shrinks from A to C, the role of

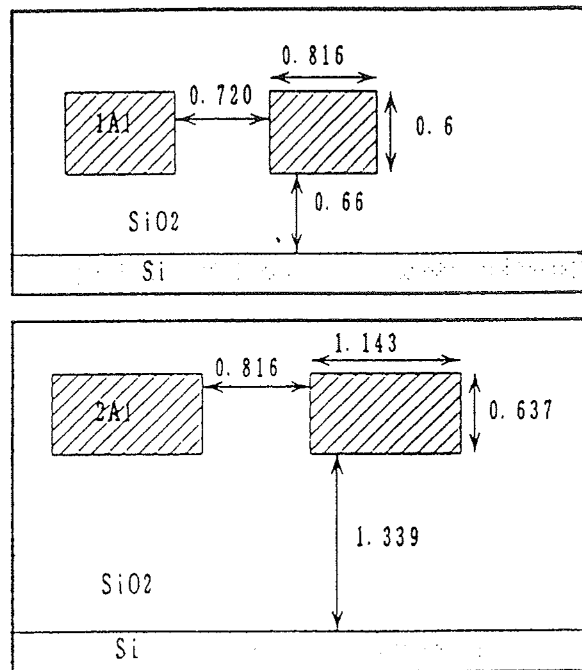

Fig. 2 Wiring size (um) of measured device

Table 1 Comparison between measured and simulated data (fF/um)

	1Al (First Aluminum)		2Al (Second Aluminum)	
	wire-gnd	wire-wire	wire-gnd	wire-wire
SENECA	0. 0742	0. 0510	0. 0485	0. 0564
measured	0. 0762	0. 0561	0. 0517	0. 0607
diff	3%	10%	7%	8%

Table 2 Capacitance of A, B and C (fF/um)

	wire-gnd	wire-wire	ratio
A	0. 1044	0. 0145	13. 8%
B	0. 0871	0. 0399	45. 8%
C	0. 0586	0. 0385	65. 7%

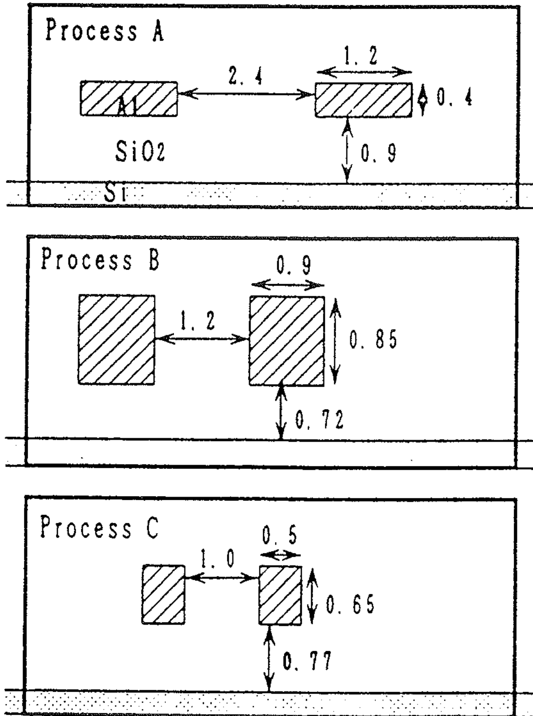

Fig.3 Wiring size(um) of process A, B and C

wire to wire capacitance increases from 13.8% for process A to 65.7% for process C, resulting in the very important contribution. Figure 4 shows the twisted wiring structure. We also calculated capacitance for this structure as shown in Table 3. Usually for this kind of complex structures, actual measurement is quite difficult. Only simulation makes it possible to obtain accurate capacitance values.

Table 3 Capacitance of crossed wires (fF/um)

wire1-ground	0.5234
wire2-ground	0.1508
wire1-wire2	0.3419

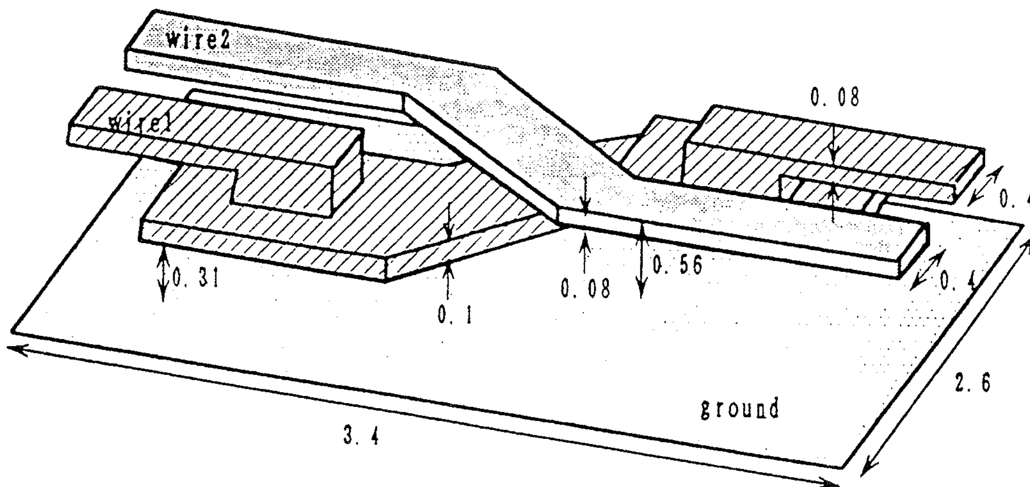

Fig.4 Crossed wires of 256K DRAM (um)

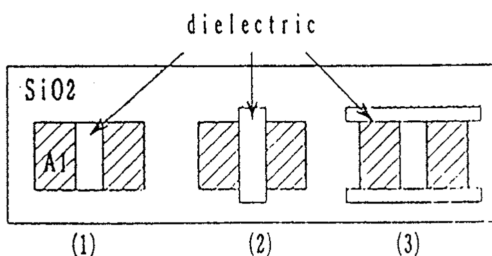

Fig.5 Wire and dielectric structures

In order to see the effect of permittivity change on the capacitance between interconnections for the purpose of decreasing it , we simulated interconnect capacitances between lines with dielectric whose permittivity is lower than SiO_2 (specific permittivity is about 3.9) [4]. We assumed the dielectric with its specific permittivity 2.5 and simulated three struc-

tures as shown in Fig.5; (1) holds dielectric with same height as wires between interconnect wirings; (2) holds dielectric with its height 1.2 times as wires; (3) also puts dielectric above and below wires with 20 % of the height of wires. Table 4 shows the capacitance on each wiring assuming that the capacitance between wires with SiO_2 is 100 . The capacitance of case (2) does not decrease so much, compared with case (3). This is due to the fact that expansion of electric field to upward and downward can be suppressed more in case (3) than in case (2).

Table 4 Capacitance ratio

All SiO2	100
case (1)	78
case (2)	71.8
case (3)	68.7
All ε=2.5	62.5

SENECA was applied to estimate the current density distribution in order to investigate the reliability[5] due to current localization for the layered wire with the aluminum layer crack caused by stress-induced migration. The wire is connected through barrier metal such as Ti/TiN/Ti. Figure 6 shows the enlargement of the cracked part. High current densities are shown darker than low densities. The magnitude of the highest current density parts specified with arrows and the lowest current density part are shown in the figure. The current density ratio is around 13.6 compared with the lowest part. From this current localization we can see the importance of barrier metal structures.

Shown in Figure 7 are simulation results for the cases with four contact holes of cylindrical structures connecting first and second interconnect layers. Although it is difficult experimentally to obtain the current density at each contact, it is quite easy to obtain it if SENECA

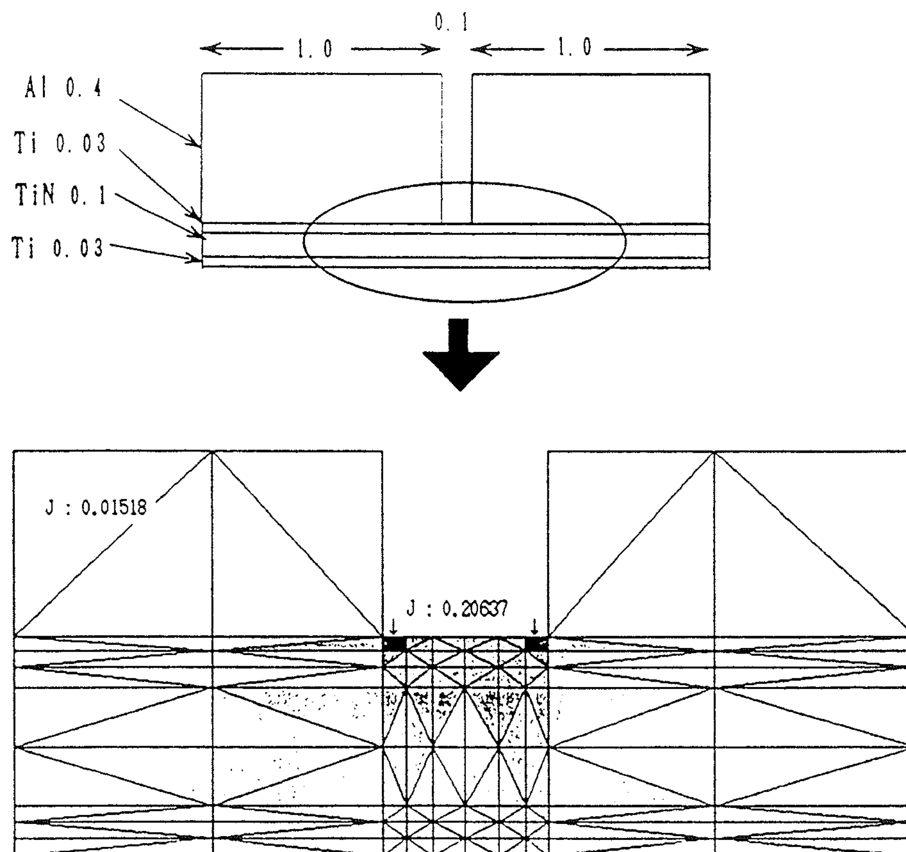

Fig.6 Current density distribution

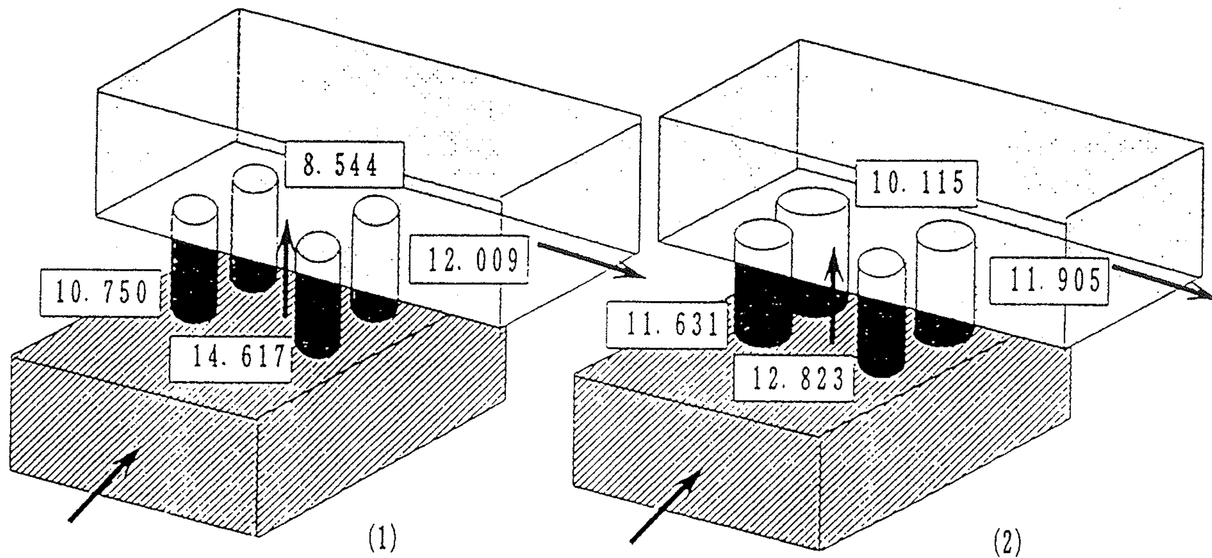

Fig. 7 Current of four contacts in arbitrary unit. (1) with same radius. (2) with different radius to level each current. Arrows indicate the direction of current.

is used. Figure 7(1) shows the simulation result for four contact holes of the same size. The ratio of magnitude of the current between minimum and maximum passing these contact holes reaches 1.7. That means the contact hole with largest current could cause a problem on reliability. This could be resolved as shown in Figure 7(2) by optimizing the size of each contact hole so that the current flows through contact holes are equal, resulting much better reliability.

4. Conclusion

We have developed SENECA, the three-dimensional wiring capacitance and current density simulation system with graphical user interface for easy and flexible operation. SENECA is now in practical use for simulating wiring capacitances of LSIs and current density estimation for achieving better reliability. The comparison between simulation and experiment proves quite good agreement. Five important applications are given to show how SENECA is utilized for practical cases.

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