ECS Transactions, 66 (5) 223-231 (2015)
10.1149/06605.0223ecst ©The Electrochemical Society

Spin-Based Silicon and CMOS-Compatible Devices

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Silicon, the main material of microelectronics, is attractive for extending the functionality of MOSFETs by using the electron spin. However, spin lifetime decay in the silicon-on-insulator transistor channel is a potential threat to spin-driven devices using silicon. We predict a giant enhancement of the electron spin lifetime in silicon thin films by applying uniaxial mechanical stress. The advantage of this proposal is that stress techniques are already routinely used in semiconductor industry to enhance the electron and hole mobility, respectively. The spin manipulation in silicon by purely electrical means is a challenge because of a relatively weak coupling of the electron spin to the electric field through an effective gate voltage dependent spin-orbit interaction. In contrast, the coupling between the spin orientation and charge current is much stronger in magnetic tunnel junctions. Magnetic random access memory (MRAM) built on magnetic tunnel junctions is CMOS-compatible and possesses all properties required for universal memory. We demonstrate a significant improvement of one of the critical MRAM characteristics, the switching time, by specially designing the recording layer. Finally, by using MRAM arrays we discuss a realization of an intrinsic non-volatile logic-in-memory architecture suitable for future low-power electronics.

Introduction

The tremendous increase in performance, speed, and density of modern integrated circuits has been supported by the continuous miniaturization of CMOS devices. Among the most crucial technological changes, lately adopted by the semiconductor industry, was the introduction of a new type of multi-gate three-dimensional (3D) transistors (1). Multi-gate 3D device architecture potentially allows device scaling beyond 10nm. However, the obvious saturation of MOSFET miniaturization puts clear foreseeable limitations to the continuation of the increase in the performance of integrated circuits. Thus, research for finding alternative technologies and computational principles is paramount.

The electron spin is attractive for complimenting or even replacing the charge-based MOSFET functionality. Spin is characterized by two possible projections on a given axis and can be potentially used in digital information processing. In addition, only a small amount of energy is needed to alter the spin orientation. Silicon is well suited for spin-driven applications. Silicon predominantly consists of ^{28}Si nuclei with zero magnetic spin. The spin-orbit interaction is also weak in the silicon conduction band. Even though these

features are promising, the demonstration of basic elements necessary for spin related applications, such as injection of spin-polarized currents into silicon, spin transport, and detection, was performed only recently.

A special technique (2) based on the attenuation of hot electrons with spins anti-parallel to the magnetization of the ferromagnetic film allowed creating an imbalance between the electrons with spin-up and spin-down in silicon thus injecting spin-polarized current. The spin-coherent transport through the device was studied by applying an external magnetic field causing precession of spins during their propagation from source to drain. The detection is performed with a similar hot electron spin filter. Although the drain current is fairly small due to the carriers' attenuation in the source and drain filters, as compared to the current of injected spins, the experimental set-up represents a first spin-driven device which can be envisaged working at room temperature. Contrary to the MOSFET, however, the described structure is a two-terminal device. Nevertheless, the first demonstration of coherent spin transport through an undoped 350µm thick silicon wafer (3) has triggered a systematic investigation of spin transport properties in silicon (4).

Silicon Spin Field Effect Transistor

The spin field-effect transistor (SpinFET) is a future semiconductor spintronic device with supposedly a superior performance relative to the present transistor technology. Complementing or replacing the charge degree of freedom used for computation in modern CMOS circuits with the electron spin promises to reduce the energy dissipation (5). SpinFETs are composed of two ferromagnetic contacts (source and drain), linked by a non-magnetic semiconductor channel region. The ferromagnetic contacts inject and detect spin-polarized electrons, in analogy to polarizer and analyzer as indicated already long ago by Datta and Das (6). Because of the effective spin-orbit interaction in the channel, which depends on the perpendicular effective electric field, the spin of an electron injected from the source starts to precess. Only the electrons with spin aligned to the drain magnetization direction can leave the channel thus contributing to the current. Therefore, the total current through the device depends on the relative angle between the magnetization direction of the drain and the electron spin polarization at the end of the semiconductor channel. A current modulation is achieved by tuning the strength of the spin-orbit interaction in the semiconductor region by the gate voltage.

In order to realize the SpinFET, the following requirements must be fulfilled (7), namely an efficient spin injection and detection, spin propagation, and spin manipulation by purely electrical means. We briefly overview recent achievements and challenges for the practical realization of a SpinFET.

Spin injection and propagation

Spin injection in silicon from a ferromagnetic metal is overshadowed by an impedance mismatch problem (8). A solution to this impedance mismatch problem is the introduction of a potential barrier between the ferromagnetic metal and the semiconductor (9). A successful experimental demonstration of a signal, which should

correspond to spin injection in doped silicon at room temperature, was first performed in 2009 (10) using a $Ni_{80}Fe_{20}/Al_2O_3$ tunnel contact. Electrical spin injection through silicon dioxide at temperatures as high as 500K has been reported in (11). Regardless of the success in demonstrating spin injection at room temperature, there are unsolved challenges which may compromise the results obtained. One of them is a several orders of magnitude discrepancy between the signal measured and the theoretical value.

It turns out that the signal is stronger than predicted in three-terminal measurements (4). The reasons for the discrepancy are heavily debated (12), (13) and it is apparent that more research is needed to resolve this controversy. For a spin-based device the possibility to transfer the excess spin injected from the source to the drain electrode is essential.

The excess spin is not a conserved quantity, in contrast to charge. While diffusing, it gradually relaxes to its equilibrium value which is zero in a non-magnetic semiconductor. An estimation for the spin lifetime at room temperature obtained within the three-terminal injection scheme was of the order 0.1-1ns (4). This corresponds to an intrinsic spin diffusion length l = 0.2-0.5µm. The spin lifetime is determined by the spin-flip processes. Several important spin relaxation mechanisms are identified (14), (15). In silicon the spin relaxation due to the hyperfine interaction of spins with the magnetic moments of the ^{29}Si nuclei is important at low temperature. Because of the inversion symmetry in the silicon lattice the Dyakonov-Perel spin relaxation mechanism is absent in bulk systems (14), (15). At elevated temperatures, however, the spin relaxation due to the Elliot-Yafet mechanism (14), (15) becomes important.

The Elliot-Yafet mechanism is mediated by the intrinsic interaction between the orbital motion of an electron and its spin, and electron scattering. When the microscopic spin-orbit interaction is taken into account, the Bloch function with a fixed spin projection is not an eigenfunction of the total Hamiltonian. Because the eigenfunction contains a contribution with an opposite spin projection, even spin-independent scattering with phonons generates a small probability of spin flips (16). The spin lifetime in undoped silicon at room temperature is about 10ns, which corresponds to a spin diffusion length of 2µm, in agreement with experiments (4).

The main contribution to spin relaxation is due to optical phonon scattering between the valleys residing along different crystallographic axis, or *f*-phonon scattering (17), (18). The relatively large spin relaxation reported in electrically-gated lateral-channel silicon structures (19), (20) indicates that the extrinsic interface induced spin relaxation mechanism is important. This may pose an obstacle in realizing spin-driven CMOS-compatible devices, and a deeper understanding of the fundamental spin relaxation mechanisms in silicon inversion layers, thin films, and fins is needed. The theory of spin relaxation must account for the most relevant scattering mechanisms which are caused by electron-phonon interaction and surface roughness. In order to evaluate the corresponding scattering matrix elements, the wave functions must be found, for the purpose of which we employ the Hamiltonian describing the valley pairs along the [001]-axis (21). The Hamiltonian includes confinement and an effective spin-orbit interaction. It also describes the unprimed subband structure, when uniaxial stress is applied (22). The lifetime enhancement is shown in Fig.1. Therefore, shear strain now routinely used to enhance the performance of modern MOSFETs can also be used to influence the spin

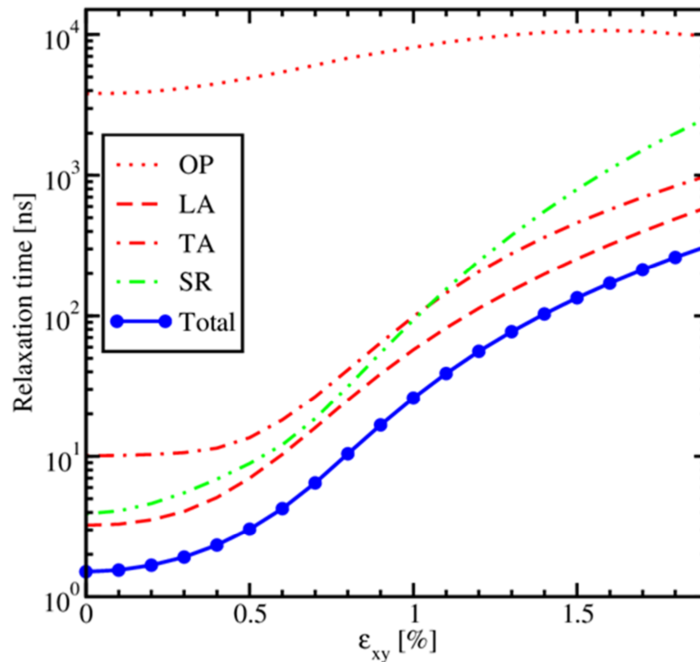

Figure 1. Dependence of spin lifetime on shear strain for T=300K and a film of 3.5nm thickness. Optical (OP), longitudinal (LA) and transversal (TA) acoustic phonon, and surface roughness spin relaxation contributions are also shown.

propagation in the channel by enhancing the spin lifetime and the spin diffusion length significantly.

Electric spin manipulation in silicon

Because of the weak spin-orbit interaction, silicon was not considered as a candidate for a SpinFET channel material. Recently it was shown (23) that thin silicon films inside SiGe/Si/SiGe structures can exhibit relatively large values of spin-orbit coupling. In actual samples with rough interfaces the inversion symmetry is broken, and atomistic simulations predict a relatively large value for the spin-orbit coupling 2μeVnm (24), which is in agreement with the only value reported experimentally (25), sufficient for realizing a silicon SpinFET. However, the channel length needed to achieve the substantial TMR modulation is longer than one μm (26). For shorter channels, the only option to realize a SpinFET is to exploit the relative magnetic orientation of the source and drain ferromagnetic contacts (7). This adds a functionality to reprogram MOSFETs to obtain a different current under the same conditions by changing the drain magnetization orientation relative to the source. Once modified, the magnetization remains the same infinitely long without any external power. This property is used in emerging magnetic non-volatile memories.

Spin Transfer Torque Magnetic Random Access Memory

The basic element of magnetic random access memory (MRAM) is a magnetic tunnel junction (MTJ). The three-layer MTJ represents a sandwich of two magnetic layers separated by a thin spacer which forms a tunnel barrier. While the magnetization of the

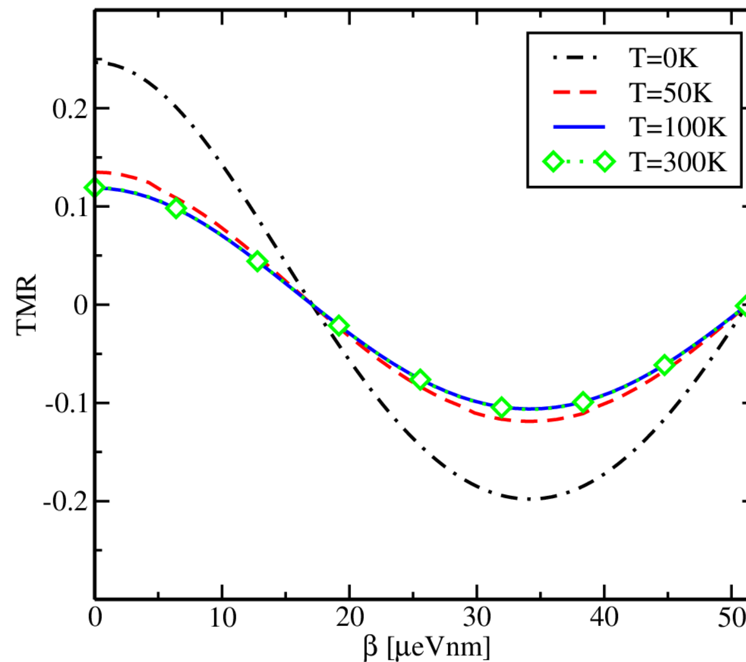

Figure 2. TMR ratio dependence on the strength of the electric-field dependent strength of the effective spin-orbit interaction for a square silicon fin oriented along [001] direction, for several temperatures (cf. (26)). The fin length is 8μm.

pinned layer is fixed, the magnetization orientation of the recording layer can be switched between the two stable states parallel and anti-parallel to the fixed magnetization direction. A memory cell based on MTJs is scalable, exhibits relatively low operating voltages, low power consumption, high operation speed, high endurance, and a simple structure.

Switching between the two states is induced by spin-polarized current flowing through the MTJ. The recoding layer's magnetization switching, by means of the spin transfer torque (STT) (27), (28), makes STT-MRAM a promising candidate for future universal memory. Indeed, STT-MRAM is characterized by small cell size (4F2) and high density inherent to DRAM, fast access time (few ns) intrinsic to SRAM, non-volatility and long retention time subject to NAND. Other exciting characteristics are unlimited endurance (more than 10^{14}) and radiation hardness. High reliability makes STT-MRAM a perfect candidate for space applications and avionics.

Because the spin-polarized current is only a fraction of the total charge current passing through the cell, high currents are required to switch the magnetization direction of the recording layer. The reduction of the current density required for switching and the increase of the switching speed are the most important challenges in STT-MRAM developments (29). If the recording layer is composed of two parts, one obtains a nearly three time faster switching at the same current density in a system with a composite in-plane ferromagnetic layer (30). The composite layer is obtained by removing a central stripe of a certain width from the monolithic recording layer of elliptic form (Fig.3). Due to the removal of the central region the switching processes of the left and right parts of the composite layer occur in opposite senses to each other. In contrast to the switching

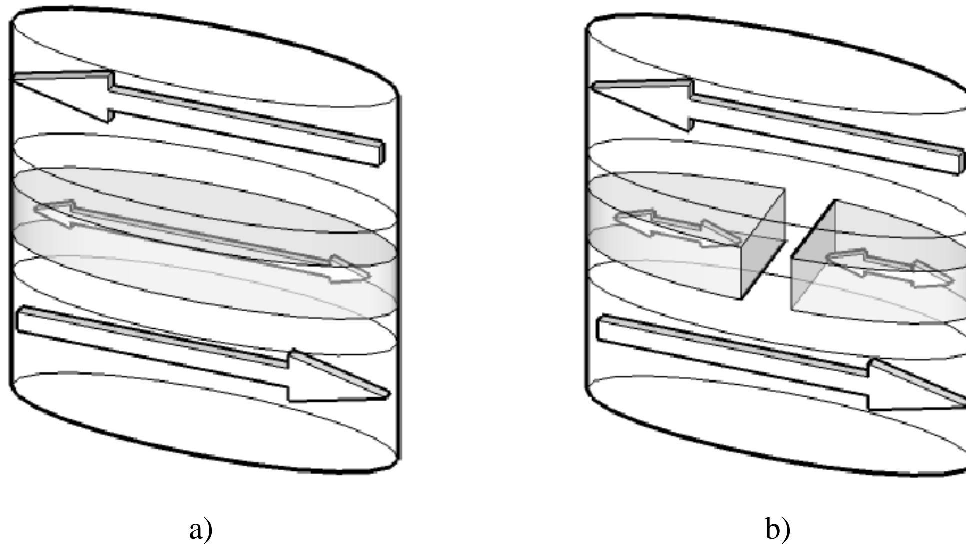

Figure 3 . a) The in-plane penta-layer MTJ structure with a monolithic recording layer and b) The proposed structure with a recording layer composed of two parts separated by a narrow gap.

of the monolithic layer, the magnetization of each half stays in-plane (Fig.4). This switching behavior leads to a decrease of the switching energy barrier, while preserving the thermal stability. The reduction of the switching time depending on geometry parameters is investigated in (31), (32). It is shown that a structure with a recording layer composed of ellipses with the axes $a/2$ and b inscribed into a rectangle $a > b$ is characterized by a switching time similar to the one in a previously considered structure with a composite recording layer, without sacrificing thermal stability. Importantly, since this architecture does not require a narrow gap between the two parts of the composite recording layer, it can be easily fabricated.

STT-MRAM-based Logic-in-Memory Architectures

The introduction of non-volatile logic could help significantly reducing the heat generation, especially at stand-by, booting, and resuming stages. It is extremely attractive to use the same elements as memory and latches to reduce the time delay and energy waste while transferring data between CPU and memory blocks. STT-MTJ-based memory has all the characteristics of a universal memory (36). Furthermore, the MTJ technology is attractive for building logic configurations which combine non-volatile memory cells and logic circuits (so-called logic-in-memory architecture) to overcome the leakage power issue (37)–(39). Recently, the realization of MTJ-based non-volatile logic gates was successfully demonstrated, for which the MTJ devices are used simultaneously as non-volatile memory cells and main computing elements (33)–(35). In (33), (34) reprogrammable logic gates realize the basic Boolean logic operations AND, OR, NAND, NOR, and the Majority operation.

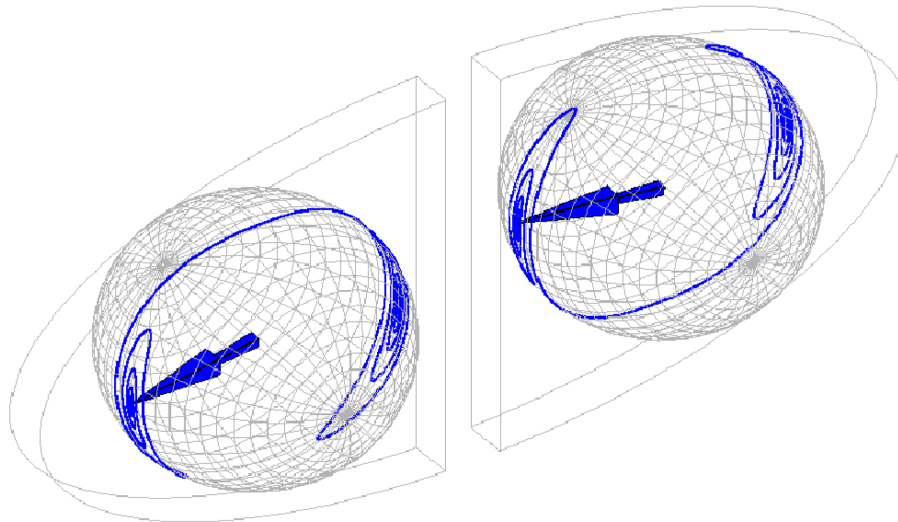

Figure 4. Magnetization components versus time for an elliptical MTJ with a composite recording layer. The magnetizations of the left and right halves, shown separately, stay in-plane explaining the acceleration of switching (cf. (32)).

All basic Boolean logic operations are executed in two sequential steps including an appropriate preset operation in the output MTJ and then applying a voltage pulse with a proper amplitude to the gate. Depending on the logic states of the input MTJs, the preset in the output MTJ, and the voltage level applied to the gate, a conditional switching behavior in the output MTJ is provided, which corresponds to a particular logic operation (34). A different set of the MTJ-based logic gates (35) is designed by using any two MRAM memory cells (Fig.5) from an array (Fig.6) to realize the Boolean implication (IMP) operation. Compared to the TiO_2 memristive switches (40), MTJs provide a higher endurance. Furthermore, the bistable resistance state of the MTJs eliminates the need for refreshing circuits (Fig.6). The logic implementation using MTJ-based gates relies on a conditional switching provided by the state-dependent current modulation on the output (target) MTJ.

The resistance modulation between the high and low resistance states in the MTJ is proportional to the TMR ratio. The error probability of MTJ-based operations decrease with increasing TMR ratio which is thus the most important device parameter for the reliability (41).

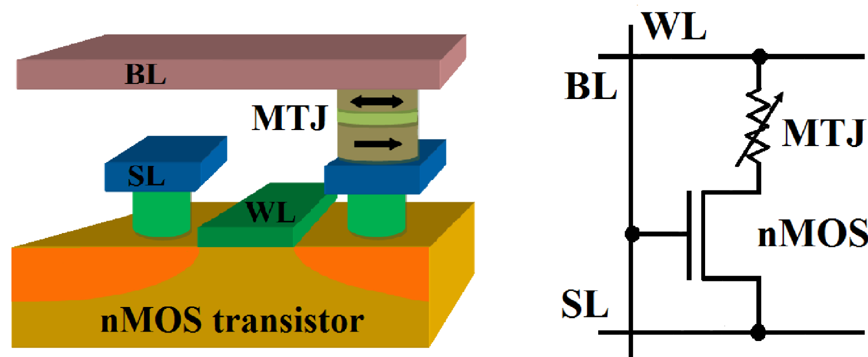

Figure 4. The 1T/1MTJ STT-MRAM cell includes an MTJ and a transistor (cf. (35)).

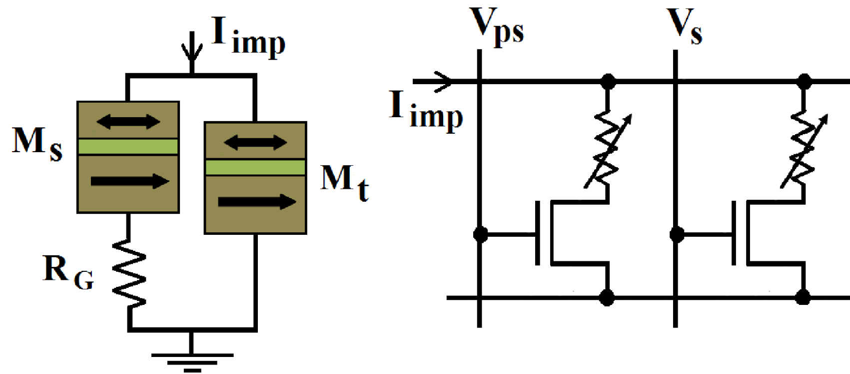

Figure 5. The implication (IMP) logic gate employs two MTJs from an STT-MRAM array (cf. (41)).

Conclusion

Recent ground-breaking experimental and theoretical findings regarding spin injection and transport in silicon make spin an attractive option to supplement or to replace the charge degree of freedom for computations. Stress routinely used to enhance the electron mobility can also be used to boost the spin lifetime. CMOS-compatible STT-MRAM cells built on magnetic tunnel junctions with a composite recording layer demonstrate a three-fold improvement of the switching time as compared to similar cells with a monolithic layer. The realization of an intrinsic non-volatile logic-in-memory architecture by using MRAM arrays is outlined.

Acknowledgments

This research is supported by the European Research Council through the Grant #247056 MOSILSPIN.

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