Tue-Expo-17:30-P16

High resolution imaging of dopant and depletion layer distributions in SiC power MOSFET using super-higher-order nonlinear dielectric microscopy

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Evaluation techniques for semiconductor devices are keys for device development with low cost and short period. Especially, dopant and depletion layer distribution in device is critical for electrical property of the device and is needed to be evaluated. Super-higher-order nonlinear dielectric microscopy (SHO-SNDM) is one of the promising techniques for semiconductor device evaluation. We developed method for imaging detailed dopant distribution and depletion layer in semiconductor device using SHO-SNDM. As a demonstration, cross-section of a SiC power semiconductor device was measured by this method and detailed dopant distribution and depletion layer distribution were imaged.

Tue-Expo-17:30-P17

Quantifying the Limits of Scanning Electron Microscopy for the Metrology of Critical Dimensions of Photoresist Structures in the Nanometer Range

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Statistical fluctuations of the critical dimensions in the Front-End-of-Line represent a challenge for the yield and reliability of CMOS technologies in the sub-22nm nodes. This implies the use of advanced characterization techniques with resolution capabilities in the sub-nanometer range. In this paper, the ability of scanning electron microscopy to achieve the required level of uncertainty is investigated by Monte Carlo simulation. Examples based on the model library approach are shown, which deal with the extraction of the critical dimensions in photoresist lines and contact holes with line edge roughness.

Tue-Expo-17:30-P18

Scanning Spreading Resistance Microscopy for failure analysis of nLDMOS devices with decreased breakdown voltage

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Scanning Spreading Resistance Microscopy (SSRM) is applied to investigate failing nLDMOS devices. The fail devices exhibit a lowered break down voltage (BVDSS) in the electrical tests. For the purpose of comparison, additionally two pass devices are visualized using SSRM. It is shown that the pass devices exhibit similar characteristics regarding the different doping areas, proving the comparability of the measurement results. In contrast, the fail device shows a degradation of the drift zone and significantly different spreading resistance values for the deep body. As simulation shows, the hypothesis of a missing drift zone implant alone explains the electrically observed lowered breakdown voltage. Based on the SSRM results a second hypothesis is proposed, based on an increased net doping of the deep body. This second hypothesis fits both, the electrical data and the observed SSRM results. SSRM enables the proving/disproving of different hypotheses causing the same electrical fail behaviour. In this work SSRM proves its applicability for implant related failure analysis cases.

Tue-Expo-17:30-P19

Electromigration in Open TSVs

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Through silicon vias (TSVs) are the components in three-dimensional integrated circuits, which are responsible for the vertical connection inside the dies. In this work we present studies about the reliability of open TSVs against electromigration (EM). A two-step approach is followed. In the first step the stress development of a void free structure is analyzed by means of simulation to find the locations where voids due to stress are most probably nucleated. In the second step, voids are placed in the TSV and their evolution is traced including the increase of resistance. The resistance raises more than linear in time and shows an abrupt open circuit failure. These results are in good agreement with results of time accelerated electromigration tests.

Tue-Expo-17:30-P20

Copper dendrites growth in LLT (Lead Lock Tape) embedded in QFP package: physical identification and characterization

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A non-destructive method to identify copper dendrites in packaged devices has been developed using X rays 3D tomography. The method shows the dendrites grows in the lead locking tape glue layer A recipe has been developed to validate the 3D results, saving the defect evidence. It requires laser ablation to define the area under inspection, chemical etching and treatment by water and LLT plastic film removal to uncover the glue layer. Dendrites are better visible by dark field optical microscopy.

Power Devices Reliability

Tue-Expo-17:30-P21

Joining and package technology for 175°C Tj increasing reliability in automotive applications

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For the task of improving the reliability and robustness of power electronic semiconductor devices, the main focus is on packaging and joining technology. The improvement is made necessary by various applications which require higher active and passive temperature cycles capability. For example: Automotive applications require a minimum life time of 15 years, wind power 25 and traction applications, 30 to 40 years and longer. Furthermore, higher reliability is demanded of new semiconductor technology, because maximum junction temperatures will, sooner or later, exceed currently recognised limits. In the near future, silicon devices will reach a maximum junction temperature of up to 200°C. And the new wideband-gap devices have the potential to exceed even this limit. That's why a new package and joining technology is mandatory. There are new developments in the pipeline: For the die contact, planar wire technology and copper based bond wires can be expected in the long term. This new technology is based on new material science and PCB process techniques. As a robust joining method, sinter or diffusion solder will be in use soon. But on the semiconductor module level, further action can be taken now, or in the near future, to increase reliability significantly. This paper presents improvements, based on material science, which are already available and can be used now, or in the near future.