Void Evolution in Open TSVs

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Through silicon vias (TSVs) are components in three-dimensional integrated circuits responsible for the vertical connections inside the dies. Beside the traditionally used filled copper TSVs, a new approach is based on so-called open TSVs. In this technology the TSV is a hollow tungsten-plated cylinder rather than an entirely filled interconnect and it is connected by an aluminium ring on the top and at the bottom to the adjacent interconnect structures. Thereby an aluminium/tungsten interface is formed, which introduces an electromigration problem. To fully understand the electromigration degradation of this structure these interfaces have to be especially addressed.
In this work we present studies about the electromigration reliability of open TSVs by means of Finite Element Method based simulation. The calculation of the material flux and the stress build up in the TSV is based on the Kirchheim model and the evolution of voids is described by the Phase Field Model (PFM).
The electromigration failure calculations are based on a two-step approach. In the first step the stress development of a void free structure is analyzed using only the Kirchheim model. This analysis indicates the locations, where voids due to stress are most probably nucleated. In the second step voids are placed in the TSV and their evolution is traced by the PFM. The result of this simulation shows the development of the TSV's resistance in time. After a void is placed and allowed to grow with time, it is found that the resistance rises more than linearly because the growing void reduces the conducting cross section. Finally an abrupt resistance jump is observed leading to an open circuit failure. Our findings are in good agreement with results of accelerated electromigration tests.