Characterization and Modeling of Reliability Issues in Nanoscale Devices

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***Abstract*—Detailed investigations of charge trapping mechanisms have revealed a very specific picture of defects in the oxide of MOSFETs. Important features of these defects, such as the existence of metastable states, were indicated by time-dependent defect spectroscopy. These insights, together with the theoretical foundation provided by the non-radiative multi-phonon (NMP) theory, led to the development of the four-state NMP model. This model describes charging processes of oxide defects microscopically, and it is able to unify reliability phenomena such as bias temperature instability, random telegraph noise and stress-induced leakage currents. Furthermore, it correctly describes the continuous degradation measured on large-area devices and the discrete trapping events observed on nanoscale devices, using the same parameters. We finally also demonstrate how this comprehensive validity can be exploited to efficiently extract the physical model parameters in order to simulate the variability and reliability of nanoscale devices.**

Introduction

Charge trapping events in nanoscale devices can be identified and quantified based on the height of the step they cause in the threshold voltage. By applying time-dependent defect spectroscopy (TDDS) [1], the time constants of defects corresponding to these steps can be extracted. Based on nonradiative multiphonon (NMP) theory [2, 3], the four-state NMP model has been developed which can explain these bias- and temperature dependent time constants for various stress conditions. In accordance with measurements, this model also explains the wide distribution of time constants [4, 5] and the link between random telegraph noise (RTN) [6–10] and bias temperature instabilities (BTI) [11–18]. As a wide distribution of time constants implies a pronounced variability of nanoscale devices, a lot of defects have to be characterized with TDDS in order to obtain the distribution of the defect parameters. However, as TDDS measurements are very time consuming it is difficult to obtain these distribution this way [19]. In order to obtain these technology dependent defect parameters efficiently, the distributions can be extracted from large-area devices (or many nanoscale devices in parallel). This approach is based on the assumption that the distributions of defects properties are the same for nanoscale and large-area devices of the same technology (see Fig. 1).

Microscopic Oxide Defects

Important details about the nature of oxide defects can be obtained by measuring and analyzing the discrete steps of the threshold voltage during the recovery of previously stressed nanoscale devices [13, 20–22]. The TDDS uses a "spectral map" where these steps enter according to their step height and emission time. This is done for many subsequent stress and recovery cycles on the same device which give rise to clusters of similar step height and emission times in the spectral map.

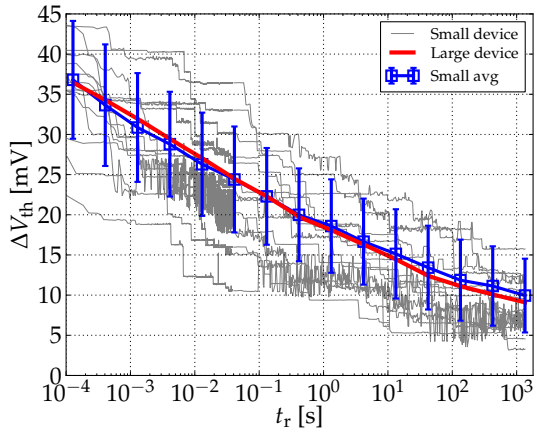

Fig. 1: The recovery of the threshold voltage of previously stressed nanoscale devices (grey) shows discrete steps which correspond to single charge trapping events. The average of these recovery traces (blue) was reduced by 30% to obtain perfect agreement with the recovery data measured on a large-area device of the same technology (red).

As the step height of a defect is mainly determined by its position along the channel, these clusters can be assigned to particular defects, and thereby reveal the statistics of their *annealing process*. By evaluating these clusters for varying stress times, the statistics of *defect activation* can be obtained as well. Doing so for various stress voltages, the effective capture (τ_c) and emission time constants (τ_e) of single defects as a function of the gate voltage and the temperature are accessible. Such TDDS studies have revealed defects with a distinct sensitivity to the readout voltage as shown in Fig. 2. Furthermore, the measured capture and emission time constants were found to be only weakly correlated, which implies metastable states in addition to the two stable charge states. Based on these considerations the microscopic four-state NMP model has been developed where the charge state transitions are modeled according to the NMP theory and the others follow simple transition state theory. This model approximates the energy potential surface along the transition path between the states by quantum harmonic oscillators. The system energy can be plotted in configuration coordinate (CC) diagrams which determine the transition dynamics of the defect. Therein, the voltage dependence enters via the position and bias dependent electrostatic potential. The parameters which define the CC diagrams, and thereby the transitions dynamics, can be obtained from density functional theory calculations on suitable defect structures [23]. Such studies on likely defect candidates have provided reference values of these parameters. Based on this data, the four-state NMP model can explain all phenomena observed in TDDS measurements. Fig. 3 shows TDDS data and the corresponding simulation results for an exemplary defect.

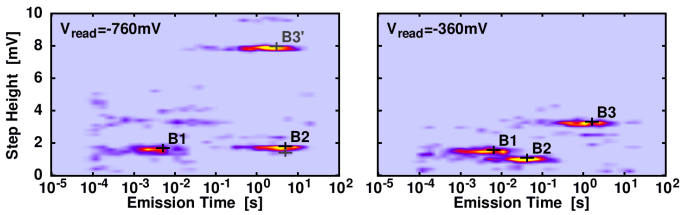

Fig. 2: Typical spectral maps obtained by the TDDS at two different readout (recovery) voltages. Three defects are clearly visible. Defect B1, is a fixed charge trap with an emission time independent of the readout voltage. Defects B2 and B3, however, are switching oxide traps with a bias-dependent emission time, with B2 being much more sensitive than B3. Also, for these defects, the step-heights are very sensitive to the readout voltage [24].

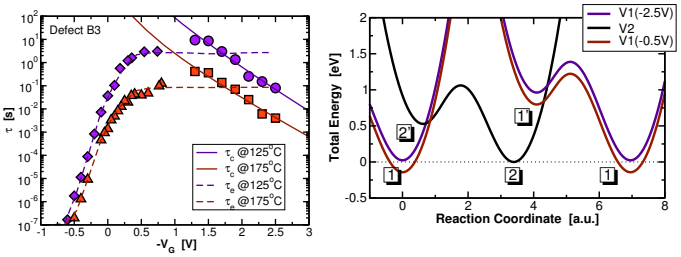

Fig. 3: The capture and emission times of switching trap B3 at two temperatures (symbols: data, lines: four-state NMP model). Excellent agreement is obtained over 8 orders of magnitude.

Distribution of Defects

With its physical model parameters, the four-state NMP model can explain various aspects of charge trapping related reliability issues. The wide distributions of the parameters can be efficiently extracted by applying information obtained on the single defect level to large-area devices.

In order to cover the whole degradation picture as measured on large-area devices, the four-state NMP model, accounting for oxide defects, has to be complemented by a model which describes the creation of interface states [25]. We model the creation and annealing of these interface states using a simple phenomenological double well model and evaluate their charge with an amphoteric SRH model. The transitions of the double well model can be depicted in a CC diagram as well and we assume all parameters which define the CC diagrams of both, the four-state NMP and the double well model, to be independent and normally distributed, while the *spatial* distribution of all defects and precursors is assumed to be uniform. In Fig. 4 the distribution of CC diagrams is shown for both defects types, together with the resulting distributions of the emission time constant during low gate voltage $\left(\tau_{\mathrm{e}}^{\mathrm{L}} = \tau_{\mathrm{e}}\left(V_{\mathrm{G}}^{\mathrm{L}}\right)\right)$ and capture time constants during high gate voltage $\left(\tau_{\mathrm{c}}^{\mathrm{H}} = \tau_{\mathrm{c}}\left(V_{\mathrm{G}}^{\mathrm{H}}\right)\right)$.

An exemplary parameter extraction has been demonstrated recently for a 2.2 nm SiON pMOSFET technology using different stress voltages ($-V_{\mathrm{G}} = 1.2, 1.7, 2.2, 2.7, 3.2\,\mathrm{V}$), temperatures ($T = 125$ and $170°\mathrm{C}$), and stress and recovery times in the range $1\,\mu\mathrm{s}$–$100\,\mathrm{ks}$ [26]. The threshold voltage shift during recovery was measured using the stress-measure-stress technique, where repetitive stress-recovery cycles were performed on the same device with stress times increasing for each subsequent cycle. With this technique the threshold voltage is not measured during stress. Therefore, this information has to be obtained indirectly by making the measurement delay t_{D} between switching to recovery voltage

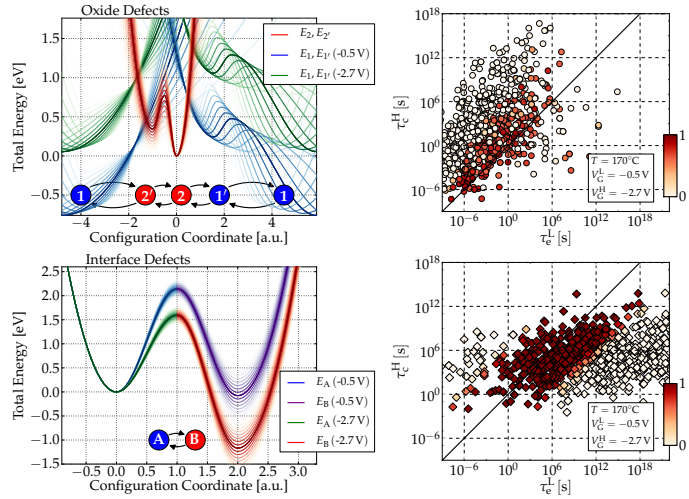

Fig. 4: **Top left**: Exemplary distribution of the CC diagrams which describe four-state NMP defects. The opaque lines represent the mean values and the fade-out illustrates up to one σ of the distributions. For simplicity this CC diagram only illustrates the situation for carrier exchange with the valence band of the substrate. An increase of the gate voltage shifts the energies according to the difference of the electrostatic potential at the defect site compared to the surface potential. **Top right**: The defects corresponding to the distributed CC diagrams plotted according to their time constants $\tau_{\mathrm{c}}^{\mathrm{H}}$ and $\tau_{\mathrm{e}}^{\mathrm{L}}$. Their color indicates their contribution to the threshold voltage shift. **Bottom**: Same as in the upper row but for the double well model.

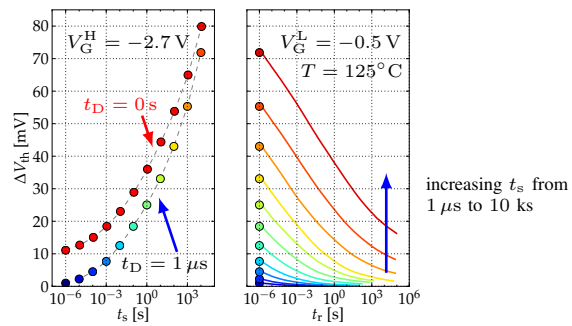

Fig. 5: Measurement results obtained with the stress-measure-stress technique. Repeated stress-recovery cycles are performed in order to indirectly measure degradation during stress. It is important to keep the delay after switching to recovery and performing the first measurement small, as even for a very short measurement delay with t_{D} of $1\,\mu\mathrm{s}$ some defects are already discharged and this information about degradation is lost.

and measuring the threshold voltage as short as possible. Still, it is important to note that some defects will already be discharged even for the shortest possible measurement delays (see Fig. 5). In order to obtain comparable data for various combinations of stress voltages and temperatures, the measured device should behave the same for each measurement, but the typically observed "permanent" threshold voltage shift of previously stressed devices requires to measure each combination of stress voltage and temperature on another "fresh" device. Therefore, device to device variability has to be taken into account. For the applied large-area pMOSFETs with an gate area of $1\ \mu\mathrm{m}^2$ this variability was found to be in the range of $\pm 15\%$, apparently mainly due to the permanent component. Given the correct distribution of the physical defect parameters and large enough devices, the simulations results for all possible BTI stress conditions have to be in agreement with the corresponding measurements. Fig. 6 shows the comparison of measured and simulated degradation, based

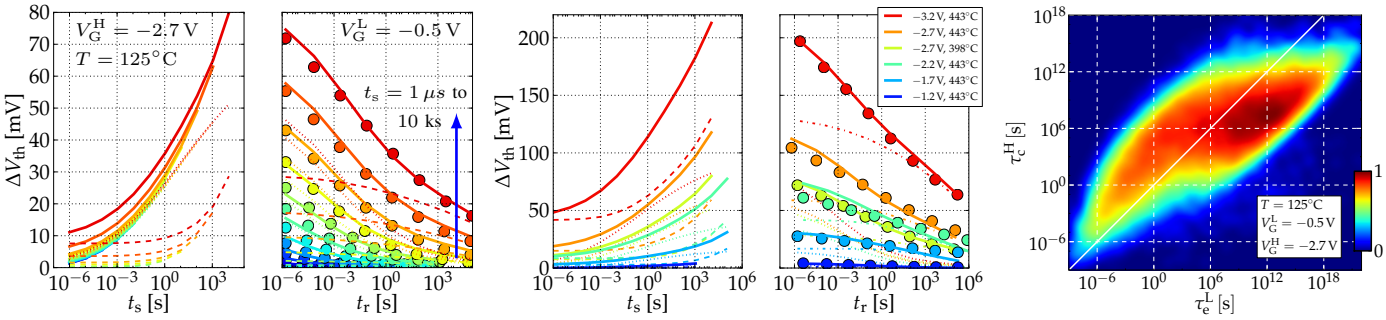

Fig. 6: **Left**: Comparison of simulated threshold voltage shifts (solid lines) to the experimental data (dots) during stress (t_s) and recovery (t_r). The contribution of the four-state NMP defects (dotted lines) and of the defects described by the double-well model (dashed lines) are also shown separately. The stress-recovery measurements and simulations were performed on the same device subsequently with increasing stress durations. However, for the sake of convenience they are plotted on top of each other in the stress and recovery part of the figure. **Middle**: Same as left for various stress voltages and temperatures, but only the last stress-recovery cycle is shown. **Right**: The CET map computed from the simulated oxide and interface defects.

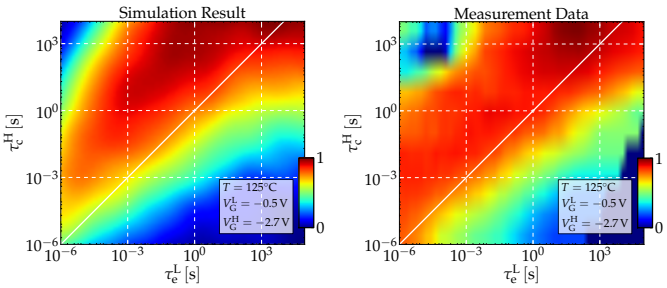

Fig. 7: Comparison of the simulated (**left**) and measured (**right**) CET maps within the measurement window. The important characteristics are reproduced: the center of the distribution is above the $\tau_c^H = \tau_e^L$ axis for short emission times and starts to cross the axis towards larger emission times.

on the distribution of defect parameters for this technology, together with the capture/emission time (CET) map [27–29] which was computed from the simulated microscopic defects. The density plotted in CET maps represents the contribution to the threshold voltage shift depending on the capture and emission time constants. It is important to recall that the emission time constant is given for low gate voltage while the capture time is given for high gate voltage. This implies that CET maps represent certain stress scenarios also including the temperature. The contribution of a particular defect to this density at $\left(\tau_c\left(V_G^H\right), \tau_e\left(V_G^L\right)\right)$ is given by its step height times the probability that the defect changes its charge state for the given stress setup. Using the equilibrium occupancy $f\left(V_G\right)$, the later can be described by its equilibrium occupancy difference which evaluates to [30]

$$a = f(V_G^H) - f(V_G^L) = \frac{\tau_e^H}{\tau_e^H + \tau_c^H} - \frac{\tau_e^L}{\tau_e^L + \tau_c^L}.$$

In contrast to this computation from *simulation results* of single defects, CET maps can also be calculated directly from *measurement data*. As the integral of CET maps gives the threshold voltage shift, this can be done by taking the mixed partial derivative of the measured recovery traces [27, 30]. This allows for a comparison of measurement data and simulation results within the measurement window (see Fig. 7).

Implications of Oxide Defects

When the defect parameter distribution is applied to obtain the microscopic defects of nanoscale devices, various reliability aspects become apparent. First, nanoscale devices with typical defect densities possess only a few tens of defects in typical TDDS measurement windows, and as their number

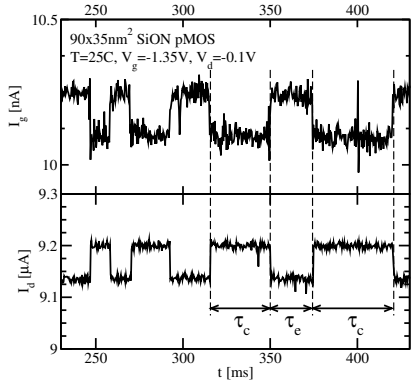

Fig. 8: A hole capture event in the oxide reduces the drain current I_d while a subsequent emission of the hole restores the original electrostatics and, thereby, I_d. On nanoscale devices these events are visible as discrete steps in the drain current (lower panel). At the same time discrete steps of the gate current I_g can be observed (upper panel) which indicates the opening and closing of a tunneling path that correlates with the capture and emission events [31].

is subject to random fluctuations, significant variability is inherent. More importantly, the parameters of the defects are drawn from broad distributions which explains the large variability observed on nanoscale devices. Another important insight which is perfectly described by the four-state NMP model is that RTN and BTI are just different realizations of the same mechanism: BTI is related to charging of defects in the oxide, but for certain stress conditions the capture and emission time constants can be roughly equal, leading to a stochastically repeating charging and discharging as it is usually observed in RTN measurements. The metasable states of the model can also explain the more involved anomalous RTN. Reliability issues related to trap assisted tunneling through gate oxides come naturally with microscopic defects. For example, the effect of stress induced leakage current (SILC) is inherent to the four-state NMP model and can be explained by the CC diagram where for certain stress voltages capture processes take place via the channel while emission processes are governed by gate interaction. The correlation between tunneling through the gate oxide and BTI has been verified experimentally (see Fig. 8).

Conclusions

The four-state NMP model can successfully describe various charge trapping related reliability issues which can be observed on nanoscale up to large-area devices. For the understanding of these defects it is important to know the *distributions* of the physical model parameters. We have demonstrated

how large-area devices can be employed to efficiently extract these widely distributed parameters. Simulations based on these parameter distribution show good agreement for various stress conditions on large-area devices and they allow for a detailed insight into the relation of large and small devices with respect to reliability issues. Finally, the extracted distribution of defect parameters enables accurate simulation and investigation of charge trapping processes in nanoscale devices.

ACKNOWLEDGEMENTS

This work has received funding from the the European Community's FP7 Project n°619234 (MoRV) and the Intel Sponsored Research Project n°2013111914.

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