Predictive Hot-Carrier Modeling of n-Channel MOSFETs

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***Abstract*— We present a physics-based hot-carrier degradation (HCD) model and validate it against measurement data on SiON n-channel MOSFETs of various channel lengths, from ultra-scaled to long-channel transistors. The HCD model is capable of representing HCD in all these transistors stressed under different conditions using a unique set of model parameters. The degradation is modeled as a dissociation of Si–H bonds induced by two competing processes. It can be triggered by solitary highly energetical charge carriers or by excitation of multiple vibrational modes of the bond. In addition, we show that the influence of electron–electron scattering (EES), the dipole-field interaction, and the dispersion of the Si–H bond energy are crucial for understanding and modeling HCD. All model ingredients are considered on the basis of a deterministic Boltzmann transport equation solver, which serves as the transport kernel of a physics-based HCD model. Using this model, we analyze the role of each ingredient and show that EES may only be neglected in long-channel transistors, but is essential in ultrascaled devices.**

***Index Terms*— Degradation, hot-carrier, interface trap, MOSFET, reliability, spherical harmonics, spherical harmonics expansion (SHE), ViennaSHE.**

I. Introduction

HOT-CARRIER degradation (HCD) has been known as a detrimental phenomenon for more than four decades as it impacts the performance of the fundamental building block of modern microelectronics, the MOS transistor. During the last four decades, HCD models have evolved from empirical or phenomenological approaches [1]–[3] to more complex models in an attempt to reveal the rich physics behind this effect [4]–[6]. The early attempts aimed at linking the device life time to macroscopic quantities, such as the electric field, which was commonly considered to be the driving force behind HCD. Many HCD models, such as the lucky electron model [1], are based on this idea. However, further investigations have demonstrated that HCD is energy rather than electric field driven [7]–[10]. This concept has resulted in the so-called energy driven paradigm proposed in [9] and [10]. However, in [11] and [12], we have shown that the maximum of the interface state density N_{it} coincides neither with the electric field nor with the average carrier energy. Instead, another quantity that is called the carrier acceleration integral (AI) was identified to properly describe HCD [13], [14]. First introduced in [15] and [16] (Hess model), the AI defines an Si–H bond dissociation rate using the carrier energy distribution function (EDF). Another idea that has been put forward in [15] and [16] is that the dominant mechanism of the bond-breakage changes when MOSFETs are scaled down. For example, in high-voltage and/or long-channel devices, individual carriers are rather hot and the high energetical fraction of the carrier ensemble is substantially populated. As a result, Si–H bond dissociation can be triggered by a solitary hot carrier in a single collision. This mechanism is referred to as the single-carrier process [15]. Contrary to that, in ultra-scaled MOSFETs, operating voltages are rather low and hence the probability to find carriers with kinetic energies higher than a typical bond dissociation energy (1.5 eV) [17] is low. Nevertheless, significant HCD is observed. This is because an ensemble of colder carriers can excite the vibrational modes of the bond followed by hydrogen release from the last bonded level to the transport state [15], [18], [19]. This process is referred to as the multiple-carrier mechanism.

The main disadvantage of the Hess model is that the degradation is formulated in terms of interface trap densities, which are not linked to the device level, and therefore, the degradation of the device characteristics is not captured. This is important, since for instance a trap in the drain junction will have a different effect on the device characteristics than a trap within the channel. To bridge this gap, a model that inherits the main features of the Rauch and La Rosa paradigm as well as the Hess model has been developed in [20]–[23]. The main advancement of this model is due to a simplified carrier transport treatment. In particular, the AI is represented by some empirical factors that depend on the operation condition linked to the drain current. This simplified treatment of carrier transport is in the spirit of the energy driven paradigm, where the bond dissociation rates are modeled using the knee energy concept [9], [10], [24], [25]. The combination

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of the Hess model and the energy driven paradigm allows to distinguish three main modes of HCD, namely:

1) driven by single-carrier process of the bond dissociation;
2) governed the multiple-carrier process;
3) dominated by electron–electron scattering (EES).

In the Bravaix model, these regimes are considered to be independent. This appears to be a serious simplification since all these mechanisms affect the carrier distribution function, and hence their own rates. For instance, if a trap is generated and subsequently becomes charged, it disturbs the electrostatics of the MOSFET and acts as an additional scattering center, thereby distorting also the mobility. This means that the rates of all three mentioned processes are affected. Furthermore, although the importance of EES in the context of HCD has been discussed, there is still no consensus on the role of EES. It has long been shown that EES can play a crucial role in ultrascaled MOSFETs. In [26] and [27], it was demonstrated that EES populates the high-energy tail of the EDF, thereby significantly enhancing HCD. At the same time, Randriamihaja *et al*. [23] suggest that the impact of EES on HCD is negligible. Instead in [23], the dominant mechanism responsible for HCD in short-channel devices is modeled as a two particle process, which is the combination of the multiple-carrier and single-carrier mechanisms of bond dissociation.

In previous versions of our physics-based model of HCD, these mechanisms were coupled in a manner that their contributions into the total interface state density $N_{\rm it}$ are weighted with some probabilities [28], [29]. These probabilities are empirical factors and were used as fitting parameters. Physically this is not meaningful, since these processes are competing pathways of the same reaction. In both cases, this reaction converts same neutral precursors (passivated Si–H bonds) into same interface traps. Therefore, single- and multiple-carrier processes have to be considered consistently within the same system of rate equations. This idea was first expressed within the Hess model [15] but never properly followed up.

Another important model ingredient is the bond dissociation energy dispersion [30], [31]. The statistical distribution of this energy was suggested to determine two different slopes of HCD [32]–[34]. However, this information has not been incorporated into any HCD model connecting the microscopic level of defect generation and the device simulation level. Another factor intimately related to the energy dispersion is the activation energy reduction due to the interaction of the bond dipole moment and the electric field [21], [35].

To summarize, a physics-based model for HCD includes three main subtasks: 1) proper description of the defect generation mechanisms; 2) with rates being determined by the carrier distribution function obtained from carrier transport treatment; and 3) modeling of the degraded devices. The main goal of this paper is to present a physics-based model for HCD covering the aforementioned aspects. The model has to properly consider the interaction of hot and colder carriers, leading to competing pathways of the Si–H bond-breakage reaction. As essential ingredients, EES, dispersion of the bond dissociation energy, and its reduction via a dipole-field interaction are incorporated into the model. The role of each of these ingredients is then carefully analyzed. Finally, the model will be validated against experimental data obtained on ultrascaled MOSFETs as well as in their longer-channel counterparts. One of the main demands to the model is a proper description of HCD in these different devices using the same set of the model parameters.

TABLE I
PAIRS OF GATE V_g AND DRAIN VOLTAGES V_d USED TO HOT-CARRIER STRESS THE n-MOSFETs

$L_{\rm G}$	$V_{\rm g}$,$V_{\rm d}$	$V_{\rm g}$, $V_{\rm d}$
65 nm	1.8 V, 1.8 V	2.2 V, 2.2 V
100 nm	1.2 V, 1.8 V	1.46 V, 2.2 V
150 nm	0.9 V, 1.8 V	1.1 V, 2.2 V

II. EXPERIMENT

To validate the model, we employed n-MOSFETs of identical architecture differing only in the gate length: $L_G = 65$, 100, and 150 nm, where the corresponding channel lengths are approximately 45, 80, and 130 nm. For all devices, an SiON gate oxide with an effective oxide thickness of 2.5 nm has been fabricated using a decoupled plasma nitridation followed by a postnitridation anneal. For simulations, we employed device structures generated by the Sentaurus process simulator and subsequent calibration using MinimosNT [36] and ViennaSHE [37]. The calibration procedure has been performed using coupled process and device simulators to reproduce the I_d–V_d, I_d–V_g, and capacitance–voltage characteristics of the fresh device.

All transistors have been subjected to hot-carriers stress at two different drain voltages $V_d = 1.8$ and 2.2 V. The gate voltage was adjusted depending on the gate length. Devices with $L_G = 65$ nm can be treated as ultrascaled MOSFETs with the HCD worst-case conditions at $V_g = V_d$ [4], [5]. At the same time, for $L_G = 150$ nm, these conditions are realized when the substrate current $I_{\rm sub}$ is at its maximum, which was experimentally observed at $V_g = V_d/2$. Initially, it was not clear whether the $L_G = 100$ nm device behaves like a short- or long-channel MOSFET. Thus, the experimental $I_{\rm sub}(V_d, V_g)$ dependencies were recorded and the maximum substrate current was obtained at $V_g = 2/3\,V_d$. The various stress conditions for all three devices are summarized in Table I. Note that we intentionally stressed the devices at relatively high voltages to enforce all bond-breakage mechanisms. This is needed for proper understanding of the physical picture behind HCD.

Measurements have been carried out on a single device per channel length and stress condition (Table I). Thus, effects of variability are not investigated in this paper. Since the devices under test differ only in the channel length, we did not strive to investigate the impact of other scaling effects on HCD. Throughout all experiments, the ambient temperature was kept at 25 °C. To asses HCD, the linear drain current $I_{d,\,\rm lin}$ was measured at $V_d = 5$ mV and $V_g = 1.5$ V, since the degradation for these devices is best seen in $I_{d,\,\rm lin}$.

To clarify whether the devices have been really subjected to HCD and not to a mixture with positive bias temperature instability (PBTI), we also recorded relaxation curves immediately

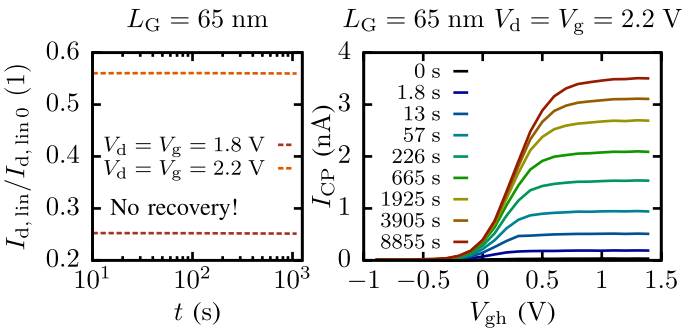

Fig. 1. Left: two exemplary relaxation curves recorded after stress for two stress conditions of the 65-nm device. The absence of recovery is a strong indicator of a negligible PBTI contribution. This behavior has been observed for all devices and stress conditions used. Right: the charge pumping currents I_{CP} measured right after each stress phase. The plateau is not followed by an increase of I_{CP} and corresponds to the saturation of the interface trap contribution to I_{CP}. We thus conclude that there is a negligible contribution of bulk oxide states. This trend is typical for all devices and all stress conditions.

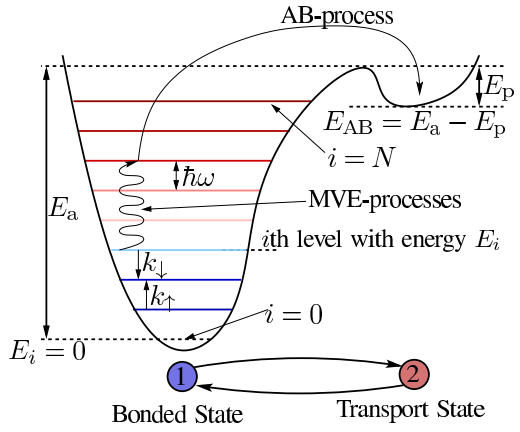

Fig. 2. Truncated harmonic oscillator model of the Si–H bond used in the derivation of the HCD model. In this concept, the Si–H bond is intact in state 1 (blue circle) and in the AB state 2 (red circle), it is broken. Impinging carriers can induce a series of bond vibrational modes, thereby exciting the bond. Once excited to a higher level, the bond can be more easily dissociated, i.e., the hydrogen can overcome the potential barrier separating the bonded and transport configurations, either thermally or due to a carrier bombarding the interface. This is because the more the bond is vibrating, the higher the oscillator level is occupied, and hence lower energy is needed to rupture the Si–H bond.

after stress. Fig. 1 (left panel) shows the normalized linear drain current changes plotted as a function of relaxation time for the 65-nm device and for both stress conditions. One can see that the $I_{d,\,lin}$ does not recover within the time slot of ~1 ks. Note that this trend is typical not only for the 65-nm transistor but also for 100- and 150-nm counterpart (not shown). At the same time, PBTI is known to have a strong recoverable component [38], [39] and the absence of this component suggests that the PBTI effect is negligible.

A major contribution to PBTI is known to be related to bulk oxide traps [40]. In the presence of both interface and bulk oxide states the charge-pumping current I_{CP} plotted versus the varying high-level voltage V_{gh} of the pulse should have a plateau followed by a further increase in the signal [41]. Such plateaus represent the saturated effect of interface traps while the signal increase is due to field sensitive oxide traps. Fig. 1 (right panel) shows a series of $I_{CP}(V_{gh})$ curves measured at each stress time step in the 65-nm device under $V_g = V_d = 2.2$ V. Since all the curves exhibit plateaus, which are not followed by an I_{CP} current growth, we conclude that only a negligible number of oxide traps have been created during HCD stress, and thus the PBTI contribution is weak.

III. Simulation Framework and Modeling

In our model, hot-carrier-induced degradation is associated with the build-up of defects at or near the semiconductor–insulator interface in MOSFETs. Since the gate dielectrics employed in modern MOSFETs are amorphous in nature, semiconductor–insulator interfaces are imperfect and characterized by disorder. Among other things, a lattice mismatch leads to electrically active dangling silicon bonds at the interface, thereby affecting the device performance. Thus, these dangling bonds are intentionally saturated by annealing the devices in a hydrogen ambient to create electrically passive Si–H bonds. The reaction rates of Si–H passivation and depassivation are determined by the kinetic energy distribution of the carriers and the configuration of the Si–H bonds. To obtain the energy distribution of the carriers for a physics-based HCD model, we solve the Boltzmann transport equation (BTE). First, a process simulation using Sentaurus process is carried out. Afterward the BTE solver is used to obtain the carrier EDFs for a particular device geometry and given stress or operating conditions. Then, this information is employed to calculate interface state density N_{it} profiles as a function of the coordinate x along the semiconductor–insulator interface. Finally, these N_{it} profiles are used to compute the characteristics of the degraded device for each stress condition over time.

A. Charge Carrier Transport

As stated, HCD is highly sensitive to the high-energy tail of the carrier EDF. Thus, an accurate solution of the BTE is required [14], [42]. In early versions of our HCD model, the stochastic BTE solver MONJU [43] based on the Monte-Carlo method was employed [28], [29]. Due to the enormous computational burden of the Monte-Carlo method to resolve the high-energy tail, a spherical harmonics expansion (SHE) of the BTE to assess HCD is attractive [44], [45]. In this paper, we use the arbitrary-order SHE simulator ViennaSHE [37], [46] to solve the bipolar BTE coupled to the Poisson equation, which also incorporates EES [47].

B. Bond Breakage Mechanisms

The carrier transport model provides the energy distribution of the charge carriers interacting with the Si–H bonds. However, the bond dissociation rates also depend on the Si–H configuration. In our model, the Si–H bond is treated as a truncated harmonic oscillator [19], [20], [48] (Fig. 2).

Due to the large disparity between the electron and proton masses, the bond-breakage energy typically cannot be delivered directly in a single collision. Instead, the bond

dissociation occurs via an excitation of one of the bonding electrons to an antibonding (AB) state [17]. As a result, a repulsive force is induced, which pushes the hydrogen atom away and the Si–H bond is considered to be broken. The AB mechanism corresponds to bond rupture by a single highly energetic carrier and corresponds to the classical HCD mode [4]. If a charge carrier, however, does not provide enough energy to trigger the AB mechanism, it contributes to the multivibrational excitation (MVE) process. This situation corresponds to bond dissociation by a series of cold carriers [49]. The MVE is especially important for scaled devices, where only few charge carriers reach kinetic energies beyond the typical dissociation energy of the Si–H bond (∼1.5 eV). In the current model, all combinations of the AB and MVE mechanisms are considered, as opposed to [29] and [50] where only bond dissociation from the ground and last bonded states was involved (termed single- and multiple-carrier processes). The consistent consideration of AB and MVE mechanisms is based on the idea that the bond can first be excited to an intermediate level by a series of subsequent scattering events followed by hydrogen release into the transport mode triggered by a solitary hot carrier.

The truncated harmonic oscillator can be described by a set of rate equations, which read

$$\partial_t n_i = \begin{cases} k_\downarrow(n_{i+1}-n_i) - k_\uparrow(n_i - n_{i-1}) & \\ \quad -r_i n_0 + p_i N_{\rm it}^2 & \text{if } 0 < i < N-1 \\ k_\downarrow n_1 - k_\uparrow n_0 - r_0 n_0 + p_0 N_{\rm it}^2 & \text{if } i = 0 \\ \quad -k_\downarrow n_{N-1} + k_\uparrow n_{N-2} & \\ \quad -r_{N-1} n_{N-1} + p_{N-1} N_{\rm it}^2 & \text{if } i = N-1 \end{cases}$$

where n_i is the occupation number of the ith level, N is the number of levels, $k_\downarrow$ and $k_\uparrow$ are the bond deexcitation and excitation rates, p_i is the Si–H passivation rate, and r_i the Si–H rupture rate for the ith level. To solve this rate equation, it is assumed that there is a large disparity in the timescales of the harmonic oscillator transitions and the passivation/depassivation processes. Thus, the rate equation above can be reduced to

$$\partial_t N_{\rm it} = (N_{\rm it,\,max} - N_{\rm it})R - N_{\rm it}^2 P \tag{1}$$

$$\text{where} \quad R = C\sum_m^{N-1} r_m \left(\frac{k_\uparrow}{k_\downarrow}\right)^m, \quad P = \sum_m^{N-1} p_m \tag{2}$$

$$\text{with } C = \sum_m^{N-1} \left(\frac{k_\downarrow}{k_\uparrow}\right)^m \tag{3}$$

which is solved analytically with the initial condition $N_{\rm it}(0) = 0$. The solution reads

$$N_{\rm it}(t) = \frac{1}{\tau P}\frac{1-f(t)}{1+f(t)} - \frac{R}{2P} \tag{4}$$

$$f(t) = \frac{2\tau^{-1} - R}{2\tau^{-1} + R} \times \exp(-2t/\tau)$$

$$\tau^{-1} = \sqrt{R^2/4 + N_{\rm it,\,max} R P}.$$

Here, R represents the cumulative bond dissociation rate that is just the sum of rates from each particular level weighted with the corresponding occupation numbers. The cumulative rate P describing the passivation process is modeled by an Arrhenius law with a single potential barrier E_p, i.e., $P = \nu_p \exp(-E_p/k_B T_L)$ with the prefactor ν_p being the attempt frequency. Due to the quadratic dependence of the passivation process rate on $N_{\rm it}$ used in the model, P is usually small due to the large potential barrier E_p. Thus, the annealing rate of broken Si–H bonds is kept reasonably small. The dissociation rate for the ith level with energy E_i is

$$r_i = I_{{\rm AB},\,i}^{n/p} + \nu_r \exp\left(-\frac{E_a - \boldsymbol{d}\cdot\boldsymbol{E}_{\rm ox} - E_i}{k_B T_L}\right) \tag{5}$$

where ν_r is an attempt frequency, while $\boldsymbol{d}$ is the bond dipole moment. The rate r_i contains an Arrhenius term that models the thermal activation of hydrogen over the potential barrier and the AI $I_{{\rm AB},\,i}^{n/p}$ [15], [16] that represents the cumulative ability of the carrier ensemble to break the Si–H bonds. It is worth mentioning that the potential barrier E_a, which enters (5) can vary depending on the energetical position of the level i and the interaction of the dipole moment $\boldsymbol{d}$ with the electric field $\boldsymbol{E}_{\rm ox}$, leading to an energy reduction $\boldsymbol{d}\cdot\boldsymbol{E}_{\rm ox}$ [21]. Such an energy lowering affects both Arrhenius and hot-carrier terms in (5) for each oscillator vibrational level i.

In a similar fashion, the bond excitation and deexcitation rates are defined as

$$k_\uparrow = I_{\rm MVE}^{n/p} + \omega' \exp\left(-\frac{\hbar\omega}{k_B T_L}\right) \text{ and } \quad k_\downarrow = I_{\rm MVE}^{n/p} + \omega' \tag{6}$$

where ω' is the oscillator frequency. The AI for the AB process is defined as

$$I_{{\rm AB},\,i}^{n/p} = \sigma_0 \int_{E_{\rm th}}^{\infty} f^{n/p}(\boldsymbol{x}_{\rm it}, E, t) g^{n/p}(E) v_g^{n/p}(E) \left[(E \underbrace{-E_a + \boldsymbol{d}\cdot\boldsymbol{E}_{\rm ox} + E_i}_{=-E_{\rm th}})/E_{\rm ref}\right]^p dE \tag{7}$$

where $E_{\rm th}$ is a threshold energy for electrons and holes, $E_{\rm ref} = 1$ eV, and $p = 11$ is an empirical exponent. For MVE, the AI is defined as

$$I_{\rm MVE}^{n/p} = \sigma_0 \int_{E_{\rm th}}^{\infty} f^{n/p}(\boldsymbol{x}_{\rm it}, E, t) g^{n/p}(E) v_g^{n/p}(E) \left[(E - \underbrace{\hbar\omega}_{=E_{\rm th}})/E_{\rm ref}\right] dE \tag{8}$$

and does not depend on the current state the oscillator is in.

C. Activation Energy Dispersion and Bond Dipole Moment

Due to the amorphous nature of the dielectrics employed in modern MOSFETs, the energy needed to break Si–H bonds is naturally dispersed [30], [31], [51]. To consider the effect of the activation energy E_a fluctuations, we use a Gaussian distribution with a mean and standard deviation of 1.5 and 0.15 eV, respectively. These values are in good agreement with those obtained experimentally [30], [31], [51]. To account for the dispersion of the activation energy E_a during simulation, we discretize the Gaussian distribution using a sufficient

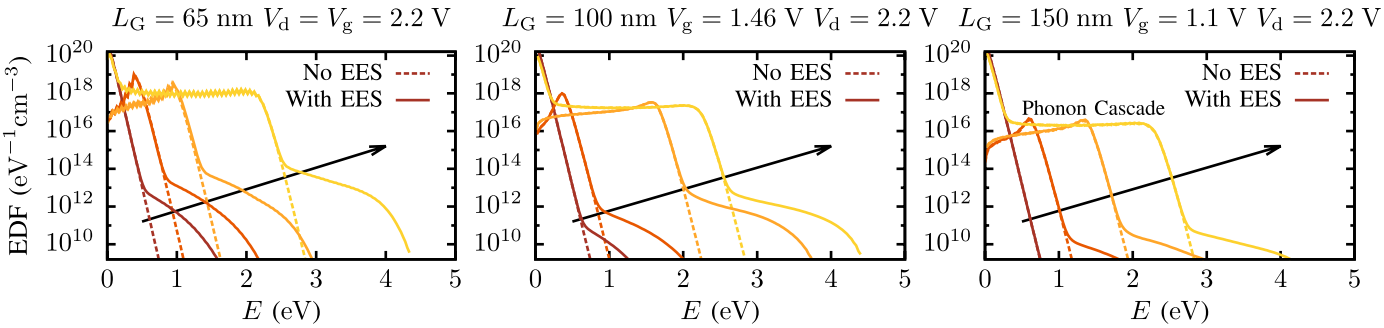

Fig. 3. EDFs along the channel with and without considering EES for the 65 (left), 100 (middle), and 150nm (right) n-channel MOSFETs. The arrow indicates the evolution of the distribution function from source to drain. The plots show that EES is most important for assessing HCD in short-channel devices.

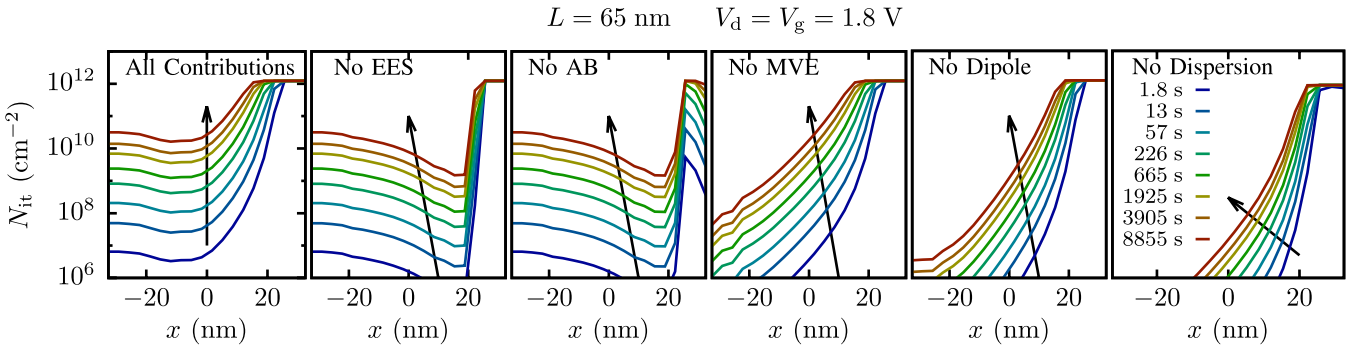

Fig. 4. N_{it} profiles predicted by the model for the 65-nm n-channel MOSFET stressed at $V_g = V_g = 1.8$ V. Most astounding is the strong influence of the dipole moment and the activation energy dispersion, which massively influence N_{it} close to the source side, but show less impact on the drain current degradation as compared with EES. The arrow indicates the growth of N_{it} with increasing stress time.

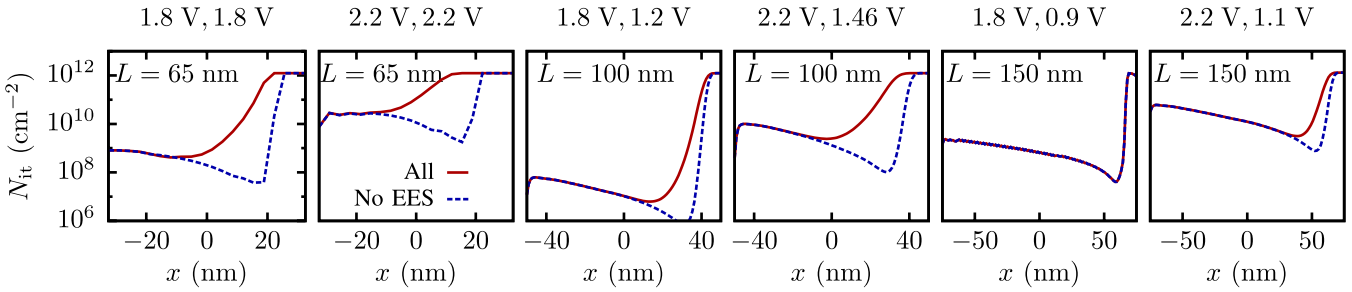

Fig. 5. N_{it} profiles predicted by the model with and without EES for the all n-channel MOSFETs for all stress conditions at $t_s = 226$ s. It can clearly be seen that EES becomes more important for smaller channel lengths and can be ignored for long-channel MOSFETs only.

number of points and subsequently calculate weight factors using the Gaussian function. Then, for each sample point, the model equations are solved, where each particular N_{it} value is multiplied by the corresponding weight factor (normalization).

IV. Results

The model has been calibrated to represent the relative change of the linear drain current versus stress time $\Delta I_{d,\,\mathrm{lin}}(t)$ (hereafter, $\Delta I_{d,\,\mathrm{lin}}(t) = (I_{d,\,\mathrm{lin}\,0} - I_{d,\,\mathrm{lin}}(t))/I_{d,\,\mathrm{lin}\,0}$). It is important to emphasize that we strive to capture HCD in these different MOSFETs using a unique set of model parameters. The examples of carrier EDFs calculated with and without EES for all three channel lengths and the stress conditions listed in the last column of Table I are shown in Fig. 3. These EDFs are obtained at different locations along the interface. One can see that EES drastically changes the shape of the EDFs and results in pronounced humps at

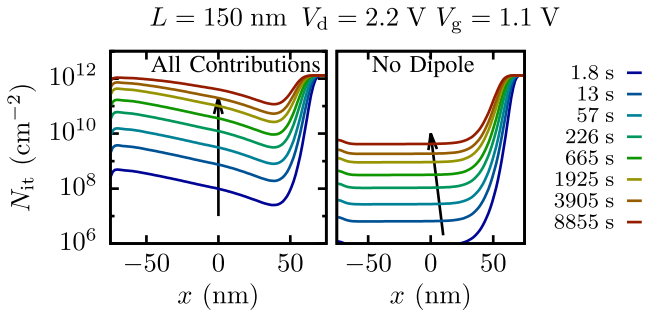

Fig. 6. N_{it} distribution for the 150-nm MOSFET stressed at $V_g = 1.1$ V and $V_d = 2.2$ V calculated with all the model ingredients (left) and ignoring field-dipole interactions (right). It can be seen that without the field-dipole interactions the N_{it} profiles feature a ledge near the source side of the gate.

higher energies. Physically, this high energetical fraction of the carrier ensemble is more populated by EES, thereby massively enhancing HCD. Note that the onset of these humps starts later

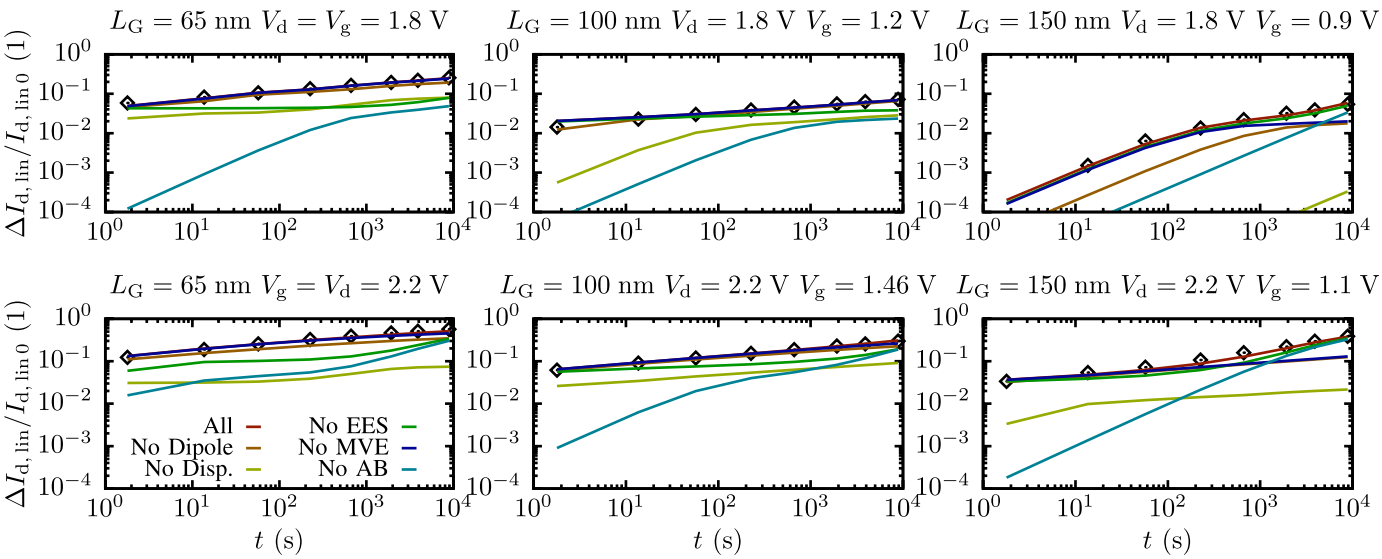

Fig. 7. Relative drain current degradation as predicted by our model (lines) for all three n-channel MOSFETs and all stress conditions (V_d, V_g) compared with measurement data (diamonds). Both short- and long-channel devices show a significant dependence of the results on activation energy dispersion and the AB process. For the long-channel MOSFET, EES plays a negligible role.

in longer devices. This is consistent with previous findings of [27] where the authors claimed that EES appears to be crucial starting at a channel length of 100 nm and beyond.

The interface state density profiles calculated with our physics-based HCD model for the case of the MOSFET with $L_G = 65$ nm stressed at $V_g = V_d = 2.2$ V for several stress time steps shown in Fig. 4. The first plot summarizes N_{it} profiles calculated using all the model ingredients, namely the superposition of the AB and MVE mechanisms, EES, the $\boldsymbol{d} \cdot \boldsymbol{E}_{ox}$ effect, and the activation energy dispersion. Further plots are obtained by ignoring one of these components. The N_{it} profiles evaluated with the full version of the model show a massive peak near the drain end of the gate, where all the virgin bonds are predominately broken and N_{it} reaches the saturation level $N_{it,\,max}$. In this area, HCD is dominated by highly energetic charge carriers. As a result, if the AB-process rate is artificially turned OFF, the drain-side N_{it} peak becomes substantially weaker and narrower, while the interface trap density near the source is only slightly affected. In the vicinity of the source carriers is rather cold and the AB process is characterized by a low rate. Here, HCD is controlled by colder carriers, and thus by the MVE mechanism. Therefore, deactivation of the MVE-process results in substantial suppression of the HCD damage near the source. Ignoring EES leads to the same tendency as suppression of the AB-process rate: the N_{it} drain maximum becomes less pronounced. This can be easily explained considering that EES populates the hot fraction of the carrier ensemble, and thus accelerates the AB mechanism. The effect of EES on the N_{it} profiles is shown in Fig. 5 for all three devices and corresponding stress conditions.

The N_{it} profiles calculated with the full model exhibit a peak near the source that becomes more pronounced at longer stress times. This peak is related to the interaction of the bond dipole moment and the oxide electric field. If this interaction is switched OFF the secondary maximum disappears, and instead a plateau is observed near the drain (Fig. 4). To resolve this plateau in more detail, we also plot the N_{it} profiles for the 150-nm device calculated for $V_g = 1.1$ V, $V_d = 2.2$ V, considering all the model ingredients and neglecting the role of the field-dipole interaction (Fig. 6). In the latter case, a plateau near the source end of the gate is clearly visible in the N_{it} profile. Such a plateau is related to a saturated MVE mechanism and is consistent with our previous findings [13], [28], [29] as well as with the results presented in [52]. In addition, the activation energy distribution affects the N_{it} profiles predominately near the source. This effect is similar to the impact of the MVE process on HCD. Near the drain, the carriers are hot enough and available virgin Si–H bonds are already broken, thereby leading to the saturation of N_{it}. As a result, a further reduction of the activation energy does not impact the N_{it} value in this MOSFET section.

Fig. 7 reveals good agreement between experiment and simulations using a single set of model parameters. Similar to Fig. 4, to analyze the importance of different model ingredients together with $\Delta I_{d,\,lin}(t)$ obtained by incorporating all mechanisms into the model the $\Delta I_{d,\,lin}(t)$ curves calculated disregarding one of the model features are shown. From this comparison, one can conclude that EES plays a key role in 65-nm devices being less pronounced if the device gate length increases (Fig. 5). For instance, in the case of the 150-nm MOSFET EES can be neglected for both stress conditions, while ignoring EES in the 65-nm counterpart leads to a severe underestimation of HCD (Fig. 5).

Since we use short as well as long-channel MOSFETs at high drain voltages, we obtained a unique possibility to study the intermediate case when both AB and MVE mechanisms are efficient. If we suppress the rate of the AB process in all three transistors, HCD is dramatically underestimated, especially at short stress times. At longer stress times, the discrepancy between experiment and simulation with suppressed

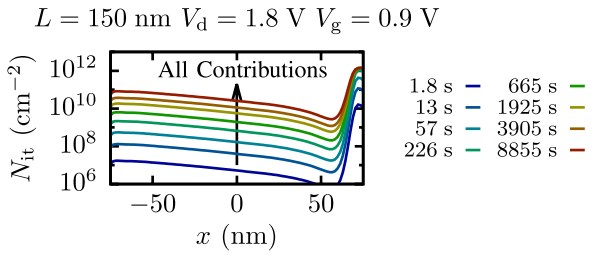

Fig. 8. N_{it} profiles simulated at each stress time step for the 150-nm MOSFET and for $V_d = 1.8$ V and $V_g = 0.9$ V. The N_{it} peak value saturates only after the fourth time steps, as opposed to the case of the 65-nm devices (Fig. 4).

AB-process $\Delta I_{d,\,\mathrm{lin}}(t)$ curves diminishes. Instead, after 10^3 s, the dipole-field interaction starts to play the crucial role. This is especially pronounced at higher $V_d = 2.2$ V in all three MOSFETs. It was shown that in the context of the N_{it} profiles, the influences of the dipole-induced energy lowering and the MVE process are qualitatively similar (Fig. 4). This tendency is shown in Fig. 7. For instance, in the case of $L_G = 150$ nm and $V_d = 2.2$ V, one can clearly see the disagreement between experiment and the model without the MVE mechanism, with the discrepancy being more pronounced at longer stress times. In all cases, neglecting the activation energy dispersion massively shifts all $\Delta I_{d,\,\mathrm{lin}}$ curves toward lower values.

Finally, the time slopes of $\Delta I_{d,\,\mathrm{lin}}(t)$ curves presented in this paper have been found to be steeper than reported in [22] and [53]. Fig. 8 shows that the peak N_{it} value for the 150-nm device stressed at $V_d = 1.8$ V and $V_g = 0.9$ V saturates only after ∼220 s. This is in contrast to the trend for the 65 nm shown in Fig. 4, where the peak value is saturated already after the first time step. As a result, the time slope of the corresponding $\Delta I_{d,\,\mathrm{lin}}(t)$ curve becomes steeper after ∼220 s, i.e., closer to values typical for the 65-nm device (Fig. 7). In the former case, the degradation is determined by a monotonous N_{it} increase throughout the whole device, while in the latter case, the time slope is determined by a slower process of propagation of a saturated N_{it} front toward the source.

V. Conclusion

We have presented a physics-based HCD model that is based on the solution of the BTE using the deterministic solver ViennaSHE. All modules of the HCD model were incorporated within the same framework, namely on the platform of ViennaSHE. The model has been validated using a wide class of n-MOSFETs, namely with gate lengths of 65, 100, and 150 nm. It is important to emphasize that the model uses a unique set of the parameters for all devices and stress conditions. Within our approach, the consistent treatment of Si–H bond breakage induced by a solitary hot carrier and bond rupture via excitation of the multiple vibrational modes has been performed. For this, we had to consider all superpositions of the competing AB and MVE processes. This means that the Si–H bond can be excited by a series of colder carriers to an intermediate level and then dissociated via excitation of one of the bonding electrons to an AB state by a single energetical carrier. Within this scenario, the potential barrier separating this intermediate state and the transport mode is lowered due to the energetical position of the level.

We have thoroughly analyzed the roles of the AB and MVE processes and realized that even in the case of ultrascaled devices the former one plays the crucial role if the stress voltages are high. The role of EES has also been studied in detail and we have shown that EES plays an important role in transistors with $L_G = 65$ and 100nm. Neglecting EES in these devices leads to a dramatic underestimation of HCD. At the same time, EES appears to be less important or even negligible in the 150-nm MOSFET. These results contradict the findings of Randriamihaja *et al*. [23], who have suggested that the role of EES in the context of HCD is overestimated. However, our findings are consistent with [27]. It is important to emphasize that rather than the channel length exclusively, the device architecture and applied voltages dictate whether the AB process is crucial or not and define the relative contribution of EES.

Another important conclusion is that the MVE process and the activation energy reduction due to dipole interaction determine HCD at long stress times. The latter mechanism results in a secondary maximum observed in the N_{it} profile near the source. This peak was earlier attributed to the contribution of majority carriers [50], which is not necessary the case. In addition, neglecting the dispersion of the bond-breakage activation energy leads to underestimation of hot-carrier damage within the entire stress time slot. Finally, the presented model is able to properly represent the linear current change observed in three different n-MOSFETs (including ultrascaled and long-channel devices) subjected to stress at different voltages.

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