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The effects of etching and deposition on the performance and stress evolution of open through silicon vias

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ABSTRACT

The effects of silicon etching using the Bosch process and LPCVD oxide deposition on the performance of open TSVs are analyzed through simulation. Using an in-house process simulator, a structure is generated which contains scalloped sidewalls as a result of the Bosch etch process. During the LPCVD deposition step, oxide is expected to be thinner at the trench bottom when compared to the top; however, additional localized thinning is observed around each scallop. The scalloped structure is compared to a structure where the etching step is not performed, but rather a flat trench profile is assumed. Both structures are imported into a finite element tool in order to analyze the effects of processing on device performance. The scalloped structure is shown to have an increased resistance and capacitance when compared to the flat TSV. Additionally, the scalloped TSV does not perform as well at high frequencies, where the signal loss is shown to increase. However, the scallops allow the TSV to respond better to an applied stress. This is due to the scallops' enhanced range of motion and displacement, meaning they can compensate for the stress along the entire sidewall and not only on the TSV top, as in the flat structure.

1. Introduction

Due to the anticipated limitations of device scaling with "more Moore" at the 6 nm node and the increasing process and factory costs of scaling, a significant amount of effort has been directed towards "more than Moore" integration [1]. This type of integration deals with the introduction of more functionality to applications beyond memory and logic. Three-dimensional (3D) integration, using a through silicon via (TSV) process is a promising technology which allows for the fabrication of systems connecting various technologies, dense device packing, lower power consumption, and reduced RC delay [2]. TSVs allow for the vertical stacking of various technologies using either a 3D stack or a silicon interposer in cases where heat dissipation is a concern [3].

There are several studies which investigate the reliability and performance of filled copper TSVs [4] as well as open tungsten TSVs. Open TSVs are desired when stress build-up due to material thermal expansion is a concern. The presence of a hole through the TSV gives the metal layer space to expand, avoiding the reliability concerns related to copper pumping [5]. However, the improved reliability performance comes at a cost of increased required area. Open TSVs are usually much wider than their filled alternatives and have lower aspect ratios [1]. One such example for a TSV intended for use in high voltage applications with a 100 μm diameter and 250 μm depth is presented in [6]. A 200 nm thick tungsten layer is deposited along the TSV sidewalls as the main conducting metal. The study given in [6] concerns itself with extracting electrical parameters from the TSV, while the scalloped sidewalls are ignored. The simulated structure is extracted from the TEM image of a manufactured TSV, making the inclusion of scallops along the sidewalls very complex. In this work a TSV with the same diameter and a 200 μm depth is studied with sidewall scallops resulting from the etching step and oxide narrowing resulting from the deposition step included in the discussion.

Due to the complexity of the processing steps required to manufacture TSVs, several concerns and potential sources of failure have appeared. These include sidewall scallops due to the nature of the etching process, void formation in the TSV hole, sidewall curvature due to etch tapering, etc. [7]. Some studies already attempt to describe the impact of the scalloped sidewalls [8], but an understanding of the effects of the oxide deposition step on the scallops and TSV performance is still lacking. The presented work simultaneously examines the effects of the Bosch etch and deposition steps on TSV performance and the applicability of well-known LPCVD models on a scalloped trench geometry. A TSV with 100 μm diameter and 200 μm depth is used as a test structure for this study.

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2. TSV processing and structure generation

The two main methods to etch the silicon layer for TSV implementation are the Bosch process and plasma etching [1]. Each process has its own flaws and reliability concerns. Problems specific to the Bosch process are a rough, scalloped TSV sidewall, notch formation at the TSV bottom, and potential step coverage issues related to the deposition of thin layers on a scalloped sidewall [7]. The plasma etching of silicon results in angled sidewalls and an added wall curvature due to the via taper edge, but the rough scallops are avoided. When dealing with open TSVs, which usually have a larger diameter and depth than filled TSVs, a Bosch process is preferred.

In order to simulate the etching and deposition steps, an in-house level set simulator is employed. The silicon etching step is performed using several deposition/etch cycles, known as the Bosch process. An oxide deposition step is then performed on the etched trench using a low pressure chemical vapor deposition (LPCVD) model. Finally, the tungsten layer, oxide liner, and nitride liner are deposited using isotropic deposition steps. In addition, the structure is connected to a 300 nm thick layer of aluminum to the tungsten at the TSV bottom.

2.1. Silicon etching using the Bosch process

The silicon etching simulations were performed using an in-house topography simulator, implemented in a level set environment [9]. The simulator is capable of generating structures after a sequence of processing steps, including etching and deposition. The first step in one cycle of the full Bosch sequence is the deposition of a polymer layer. This is performed using an isotropic deposition step at a rate of 12 nm/s for 3.5 s. The subsequent etching step is a combination of isotropic and directional/anisotropic models with differing etch rates for each material (silicon dioxide mask, silicon, and deposited polymer). The etch parameters used to generate the scalloped structure are given in Table 1.

The resulting trench is highly vertical (0.286° tapering) and contains scallops with a height and width of approximately 2.2 μm and 0.5 μm along the sidewall, respectively. The total simulation time required to generate the etched structure is approximately 10 h. This time includes the generation of the meshed interfaces after each simulation cycle. Once the etching steps are completed an isolation oxide deposition step is performed on the structure. In order to compare the effects of the scalloped sidewalls on the deposition and final shape of the isolation oxide, an alternative structure with flat sidewalls and an identical sidewall tapering is generated. The deposition steps are performed on both structures and the performance of the two TSV geometries are then compared.

2.2. LPCVD model implementation

The line-of-sight model which was implemented into a level set framework in order to simulate oxide deposition is described in [10] and is very frequently used to perform such simulations. The simulation predicts a thicker oxide layer near the top of the trench, as shown in the sample simulations in Fig. 1. The geometries shown in Fig. 1 are the results of a simulation for a 20 s etch step at an etch rate of 10 nm/s, a reaction order of 2, and a sticking probability of 0.15. Deposition profiles are shown at 5 s intervals. The structure with an aspect ratio of 1:1 appears to have the deposited material thickness reduced along the depth of the trench to approximately 75% of its highest thickness location, at the trench top. The deeper structure, with an aspect ratio of 1:2, shows a further decrease in the deposited thickness along the trench bottom, where approximately 50% of the maximum thickness is present.

This deposition model is applied to the generated trenches with flat and scalloped sidewalls. Additionally, thin layers (200 nm) of tungsten, oxide, and silicon nitride coating are deposited using isotropic rates, resulting in the structures shown in Figs. 2 and 3, respectively.

Fig. 2 shows the resulting structure after a deposition step is performed on a trench with flat sidewalls. The reduction in the deposited isolation oxide thickness is evident, as it drops from 1.2 μm at the top to 0.6 μm at the bottom of the structure. This follows the expected 50% reduction in the deposited thickness, noted in the sample trench from Fig. 1. Fig. 3 shows the final TSV structure after the required etching and deposition steps are completed on the Bosch-etched trench. The scallops along the sidewall are immediately clear. It can also be noted that the average thickness of the deposited oxide is higher at the TSV top when compared to the thickness at the TSV bottom. The oxide thickness observed at the top scallop is approximately 1 μm, while the bottom scallop thickness is about 0.5 μm. Therefore, the same effect of oxide narrowing is noted in the scalloped structure in Fig. 3 as was observed in the flat structure in Fig. 2. However, there is an oxide thickness variation around the scallops themselves, which is more accurately represented in Fig. 4. The thickness around a single scallop at approximately half of the TSV depth is noted to vary from 350 nm to 500 nm, while the oxide thickness of the TSV with flat sidewalls, at the same depth, is approximately 700 nm. The simulation time required to deposit the oxide for the flat structure of Fig. 2 is 1.5 h, while the scalloped structure requires significantly more time, approximately 10 h, in order to generate the structure in Fig. 3.

The two-dimensional profiles of the two structures, shown in Figs. 2 and 3, are imported into a finite element simulator, where they are meshed and their electrical properties, susceptibility to high-frequency signal loss, and stress responses under several conditions, are compared. The mesh used for the scalloped structure is shown in the insets of Fig. 3 for the TSV top and bottom. The total

Table 1
Etch parameters required for the Bosch model in order to generate the scalloped TSV structure with a 100 μm diameter and 200 μm depth.

	Rate	Etch ratio	Cycle time
Deposition	12 nm/s	–	3.5 s
Silicon etch (isotropic)	500 nm/s	Silicon:oxide mask 80:1	5.5 s
Silicon etch (directional)	534 nm/s	Silicon:polymer 100:1	
Resulting scallop height: 2.2 μm			
Resulting scallop width: 0.5 μm			
Total number of deposition/etch cycles: 91			
Total simulation time for the etch simulation: 10 h			

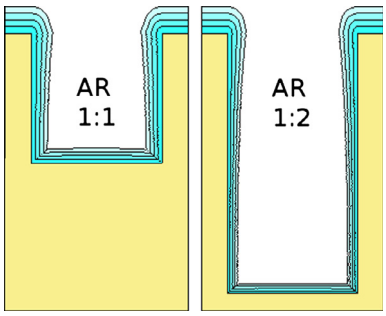

Fig. 1. Sample deposition profiles with varying hole aspect ratios. The hole diameter is 10 μm, trench aspect ratios are 1:1 and 1:2, and the simulation time is 20 s with a deposition rate of 10 nm/s, a reaction order of 2, and a sticking probability of 0.15.

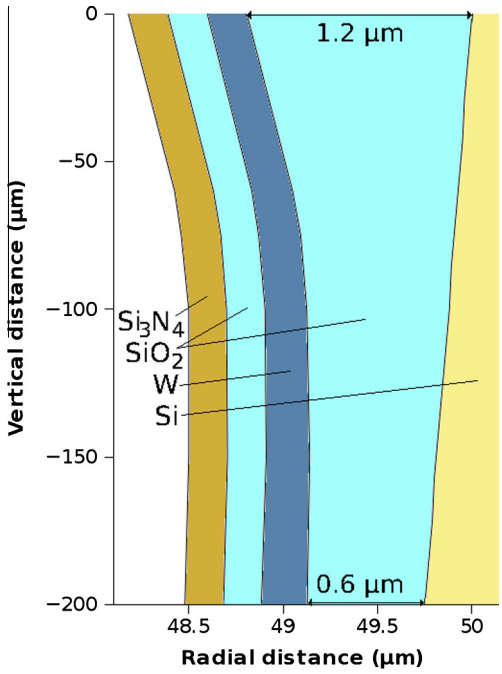

Fig. 2. Sidewall profile of a TSV without scallops. The variation in oxide thickness is evident. This structure is used for all further simulations which refer to a TSV with flat sidewalls.

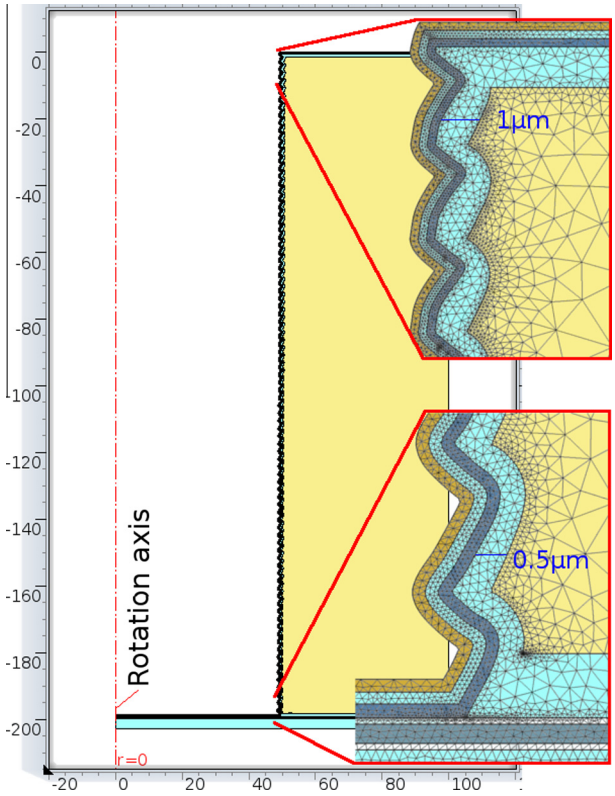

Fig. 3. TSV profile showing the scalloped nature of the structure sidewalls. The oxide is thicker at the top of the structure, but there are regions of thinning oxide around every scallop. The tungsten is connected to aluminum at the TSV bottom, which is surrounded by a thin layer of TiN. This structure is used for further simulations which refer to a TSV with scalloped sidewalls. The generated mesh, used in finite element simulations, is also shown.

mesh consists of 771,697 triangular elements, with an average element quality of 0.92. In comparison, the flat-sidewalled TSV is meshed with 96,809 triangular elements with an average element

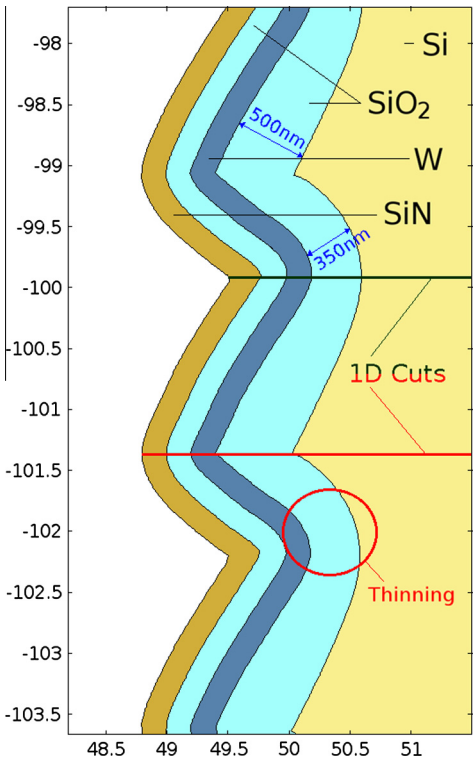

Fig. 4. TSV profile showing the scalloped nature of the structure sidewalls, showing thinning oxide regions around each scallop. The oxide thickness around each scallop can vary by up to 30%. The 1D cuts depicted represent the one-dimensional cut lines used to show the resulting stress through the structure after the thermo-mechanical stress simulation.

quality of 0.95. It is not surprising that the flat TSV requires less mesh elements, since the very fine mesh of the curvature noted in the scalloped structure is not necessary. The resulting thinning around the scallops, shown in Fig. 4, is also observed in a fabricated structure in [11], suggesting that the implemented LPCVD model can be used to accurately simulate deposition along scalloped trenches.

3. Simulations of TSV performance and reliability

The performance and several reliability aspects of the generated TSVs are examined and compared. The simulations are performed by importing the two-dimensional TSV profiles from Figs. 2 and 3 into a finite element tool for meshing and parameter extraction and stress simulation. Two-dimensional models with assumed rotational symmetry around the axis, as shown in Fig. 3, are implemented for the simulations. The comparisons are used to identify those parameters which are affected by the scalloped sidewalls. It is clear that oxide deposition is affected by the scallops, and that the oxide coverage is a leading factor in determining the TSV parasitic capacitance. The electrical parameters of the TSV, along with the high-frequency signal loss are analyzed. In addition, the stress generation due to thermo-mechanical effects and electromigration (EM) is analyzed and compared through finite element simulations. For the stress simulations, fixed constraints are placed on the bottom of the TSV and in the silicon substrate at a location 100 µm away from the TSV center. The middle and top of the TSV are left without constraints.

3.1. Electrical parameters

The main electrical parameters of the TSVs are the resistance, parasitic capacitance, and inductance, as given in Table 2. The

inductance does not seem to vary significantly, but both the resistance (+25%) and the capacitance (+40%) increase significantly in the presence of scallops. Resistance increases because of an increased length (+15%) of the tungsten layer due to its curvature around the scallops. This increased path for electrons to travel results in a higher overall TSV resistance. The capacitance is increased due to the thinning which occurs around the scallops, as shown in Fig. 4.

3.2. High-frequency signal loss

The frequency-dependent capacitance is plotted in Fig. 5, where it can be seen that, although the low-frequency capacitance varies significantly, at higher frequencies, when the device switches to the resistive region, no significant variation is observed. The simulation is performed by placing a contact on the tungsten metal at the top of the TSV, while the interface between the silicon and silicon dioxide at the TSV bottom serves as the ground node. The simulation generates the resulting electric field and from this information, a capacitance is extracted.

The frequency-dependent signal loss (S21) is analyzed by viewing the TSV as a two-port system; the signal loss is shown in Fig. 6. The simulated is performed by applying a small signal voltage at the TSV top with the output, or load, applied at the TSV bottom. The silicon/silicon dioxide interface at the TSV bottom serves as the ground node. The loss is generally caused by substrate leakage and coupling. The scalloped TSV is shown to experience a larger loss, which is once again because of the thinning of the deposited oxide around the scallops. The thin oxide results in a higher electric field between the tungsten and the bulk silicon, leading to a higher probability of leakage current and potential failure.

3.3. Thermo-mechanical stress response

The thermal stress in the TSVs is observed, when the structures are cooled from a stress-free temperature of 320 °C to 20 °C, simulating the cooling which occurs after a thermal processing step. The resulting von Mises stress in the TSV sidewall layers is shown in Fig. 7. The stress is generated due to the different coefficients of thermal expansion (CTEs) between the adjoining materials. The CTEs for the materials relevant for the presented TSVs and used in the thermo-mechanical simulations are given in Table 3. The difference in the CTEs between tungsten (4.5×10^{-6}/K) and the adjoining silicon dioxide (0.5×10^{-6}/K) is largest, which results in tungsten experiencing the highest stress.

It is clear that the flat structure experiences a higher stress through a larger portion of the tungsten layer, although the scalloped structure does show points of high stress where scallops meet and at scallop peaks. The flat structure experiences an average stress of about 1 GPa, while the scalloped structure experiences approximately 800 MPa. For a more accurate estimate of the total stress through the tungsten, the build-in stress in the order of 400 MPa [8] should also be included in the calculation. In Fig. 8, the stress is plotted using one-dimensional cut lines along the radial distance of the TSV. The scalloped TSV cuts are taken at the locations given in Fig. 4. Although Fig. 7 suggests a clear reduction in stress through the tungsten layer for the scalloped

Table 2
Electrical parameters of the TSVs.

Parameter	Flat TSV	Scalloped TSV	Difference (%)
Resistance (Ω)	0.299	0.374	25
Capacitance (pF)	4.672	6.527	40
Inductance (pH)	5.469	5.307	−3

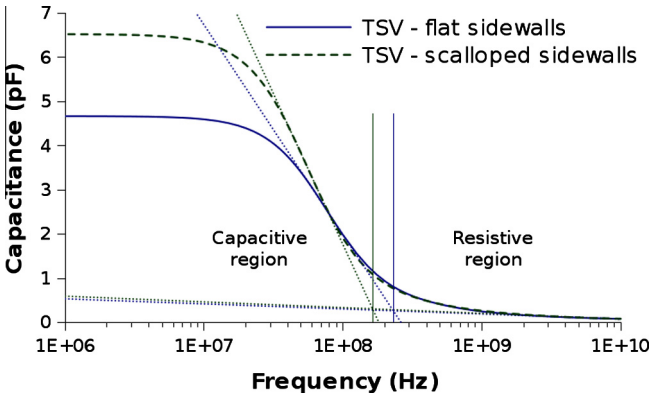

Fig. 5. Frequency-dependent capacitance. It is clear that the scalloped TSV has a higher low-frequency capacitance, while the high-frequency operation shows no significant variation.

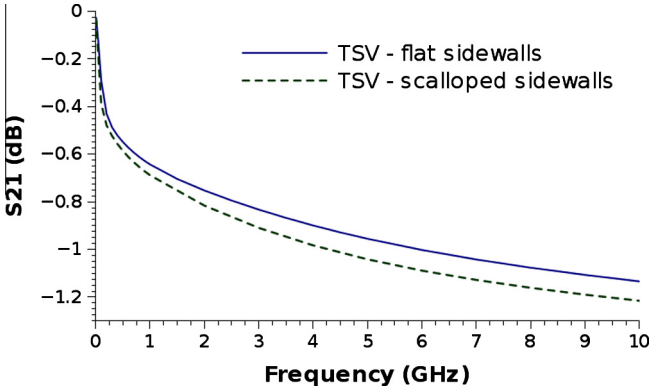

Fig. 6. Frequency-dependent signal loss S21 (dB). The input node is the tungsten metal at the TSV top, while the output is the aluminum at the TSV bottom. The silicon serves as the ground node.

structure, the 1D cuts suggest that there are locations where the stress peaks to levels above those seen in the flat structure. These peaks occur at locations where two scallops meet, while the immediate surrounding sees a stress reduction. If the bottom 1D cut from Fig. 8 is compared to the 1D cut of the TSV with flat sidewalls, this phenomenon is evident. In Fig. 9 the thermal stress through the silicon layer of the TSV, moving away from the oxide/silicon interface is shown. The effects of the scallops do not appear to be a factor in determining the rate at which the stress through the silicon decreases.

Further stress simulations have been performed, including applying pressure to the structures in the vertical direction and observing how the two TSVs distribute the stress. Once again, the scalloped structure was shown to have a smaller stress through the tungsten, since the scallops have some freedom of movement, while the flat structure can only displace to compensate for the stress at the TSV top.

3.4. Electromigration-induced stress

Simulations to determine the electromigration (EM) stress have been performed on both TSV structures. A 1 A current is applied through the structure at a stress-free temperature for a simulated one year period. The model used in order to calculate the EM-induced stress through the metal layers is given in [12]. The simulation is performed in order to detect early EM failures during the initial stages of stress build-up and void nucleation. As stress

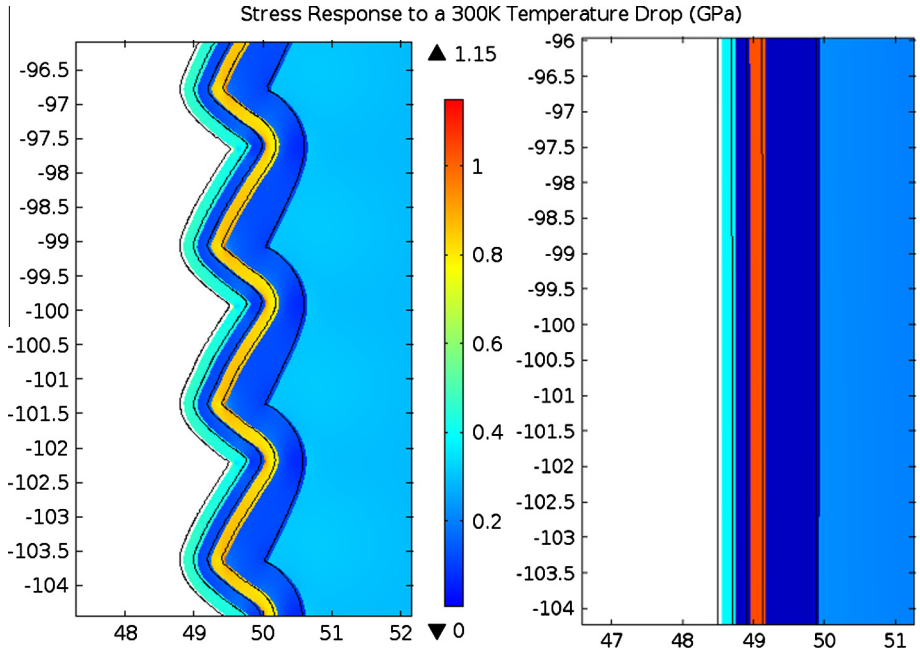

Fig. 7. Stress response (von Mises) to device cooling from 320 °C to 20 °C. The given stress-free temperature is 320 °C. The tungsten displacement at the middle of the TSV for the scalloped and flat structures is approximately 50 nm. However, the scalloped structure experiences more displacement at the TSV top, resulting in an average and a maximum displacement of 120 nm and 436 nm for the scalloped and 50 nm and 100 nm for the flat structure, respectively.

Table 3
Coefficients of thermal expansion for all relevant materials.

Material	Tungsten (W)	Silicon dioxide (SiO_2)	Silicon (Si)	Silicon nitride (Si_3N_4)
CTE (10^{-6}/K)	4.5	0.5	2.6	2.3

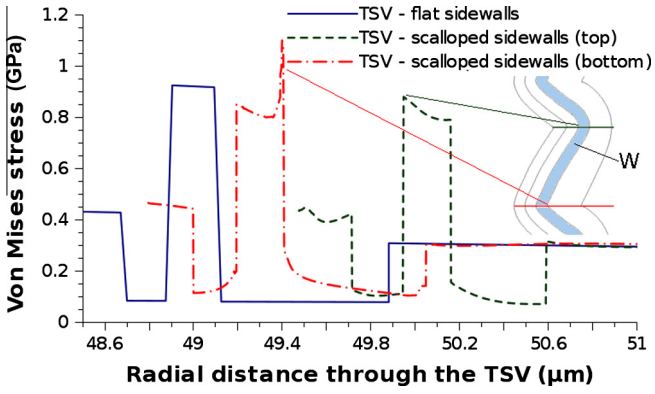

Fig. 8. Thermal stress through a 1D radial cut at the TSV middle. The top and bottom lines refer to the 1D cut lines shown in Fig. 4. An increased stress at pinch-off points where two scallops meet is evident, with a reduced stress in the direct vicinity, when compared to the TSV structure with flat sidewalls.

builds up in a metal line, the potential to reach the critical stress increases. Once the critical stress is reached, a void is nucleated and the device is likely to experience void growth, an increasing resistance, and eventual failure. Figs. 10 and 11 show the EM-induced stress after one year of operation for the flat-sidewalled and scalloped TSVs, respectively. The stress levels, distribution, and location do not vary with the presence of scallops, because the stress builds up in the aluminum layer at the TSV bottom, as opposed to the tungsten layer.

In Fig. 12, the EM-induced stress build-up in the aluminum layer over time is shown. It is evident that no major variation in

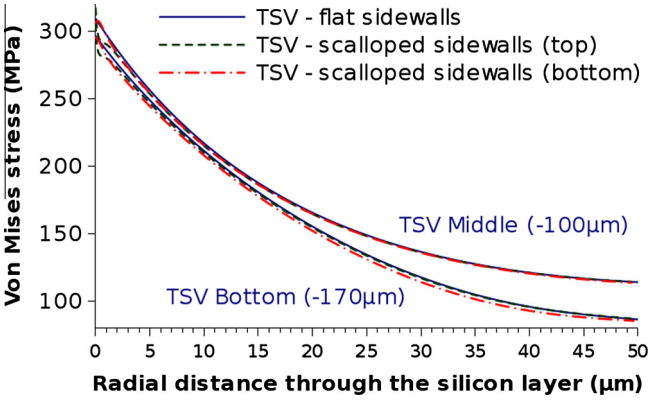

Fig. 9. Thermal stress through the silicon layer, starting at the oxide/silicon interface (0 µm) through the middle (−100 µm) and bottom (−170 µm) of the TSVs.

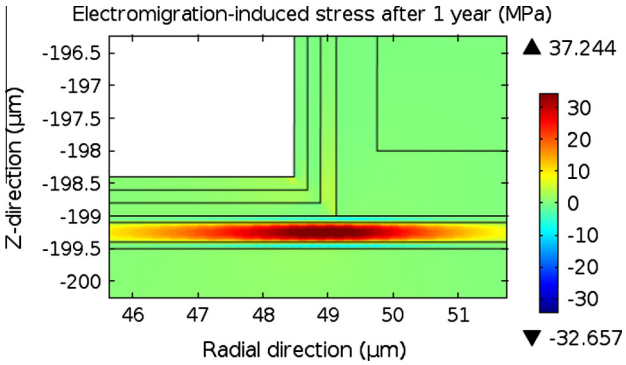

Fig. 10. Electromigration-induced stress (MPa) in the aluminum layer of the TSV structure with flat sidewalls, when a 1 A current is applied for a period of one year. The stress builds up in the aluminum layer, where it connects to the tungsten lining.

the stress build-up can be attributed to the sidewall scallops, meaning that the scallops have no effect on the electromigration reliability of the TSV structure. Although the calculations of the

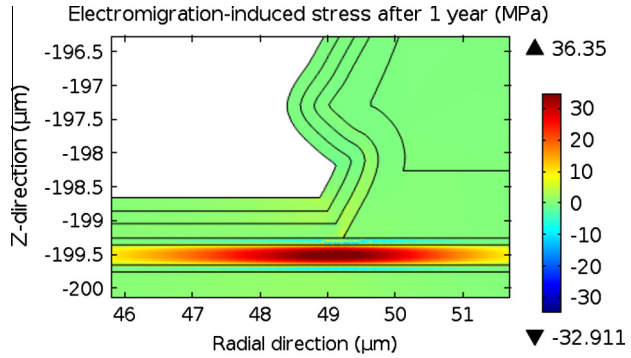

Fig. 11. Electromigration-induced stress (MPa) in the aluminum layer of the TSV structure with scalloped sidewalls, when a 1 A current is applied for a period of one year. Similar to Fig. 10, the stress builds up in the aluminum layer, where it connects to the tungsten lining. The stress level is very close to that observed in the flat structure.

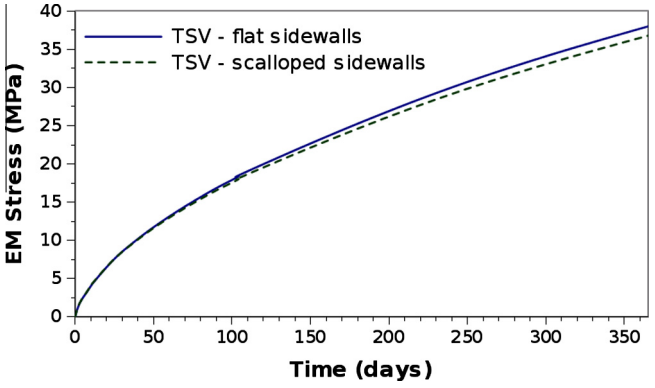

Fig. 12. Maximum EM-induced stress (MPa) through the aluminum layer in the two TSV structures, while operating at a 1 A current.

electrical parameters and thermal stresses require only minutes of simulation time, the EM simulations are much more demanding. Several hours are required to generate the EM results shown in Figs. 10–12, representing one year in TSV performance.

4. Conclusion

The effects of processing on the electrical performance and stress response of open TSV structures has been analyzed. In addition to analyzing the effects of a scalloped TSV sidewall, the influence of the oxide deposition step is also examined. This type of deposition results in oxide thinning towards the TSV bottom, but also in certain regions around the scallops themselves. The oxide thinning around the scallops leads to an increased parasitic capacitance and high-frequency signal loss when compared to the flat TSV alternative. Similarly, a scalloped structure results in an increased TSV resistance, due to the longer effective length of the deposited tungsten layer along the scalloped surface. However, the presence of scallops improves thermo-mechanical stress performance of the TSV. Although high stress peaks are found at locations where the scallops meet, an overall stress reduction is noticed. This reduction is due to the increased flexibility of the scalloped sidewalls, allowing for a larger displacement when pressure is applied to the structure. The electromigration-induced stress is shown to only affect the bottom aluminum layer and not the tungsten metal which is present along the scalloped surface. This results in no major influence of the scallops on the stress generation due to electromigration.

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