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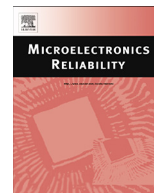

Refined NBTI characterization of arbitrarily stressed PMOS devices at ultra-low and unique temperatures

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ABSTRACT

We reexamine degradation and recovery dynamics in the negative bias temperature instability (NBTI) of p-channel metal oxide semiconductor field effect transistors (PMOSFETs) by making use of the recently developed in situ polyheater technique. The capability of switching the device temperature extremely fast and almost arbitrarily allows for measuring differently stressed devices directly after the termination of stress at a unique and much lower characterization temperature (e.g. −60 °C). This procedure ('degradation quenching') is a powerful extension of the conventional measure–stress–measure (MSM) technique and provides a cleaner way for comparing threshold voltage shifts and charge pumping (CP) currents of arbitrarily stressed devices. We find that increasing the stress bias predominantly activates a larger number of defects with similar (short) recovery time constants causing steeper threshold voltage recovery transients after the termination of stress. Increasing the stress temperature has a very similar effect on the threshold voltage shift as increasing the stress time. In both cases, defects with larger recovery time constants are activated while the number of defects with short recovery time constants remains essentially the same. A comparison of V_{TH} shift and CP data suggests that the total threshold voltage shift is due to at least two fundamentally different types of defects, one being readily recoverable and uncorrelated to the CP current while the other is 'quasi-permanent' and proportional to the CP current. By converting CP currents into corresponding threshold voltage shifts, we find that only about 50% of the 'quasi-permanent' V_{TH} damage is due to slowly-recoverable interface states. The remaining fraction is due to another, yet undefined, positively charged defect generated at virtually the same rate.

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1. Introduction

Various different NBTI degradation and recovery models are found in literature. Despite fundamental discrepancies in the microscopic details, most NBTI studies agree that the driving factors causing a threshold voltage shift during negative bias temperature stress (NBTS) are the stress temperature and the stress field [1–7]. A controversial point in literature is the creation and re-passivation of slowly-recoverable interface defects. While some groups argue that the whole NBTI effect can be fully explained by hydrogen release from Si—H bonds at the semiconductor/oxide interface and subsequent hydrogen diffusion [8–10], other groups attribute a considerable portion of the observed V_{TH} shift to hole trapping within the gate oxide and elastic or inelastic carrier exchange between the silicon substrate and stress induced oxide defects [5,6,11,12]. To better understand NBTI, is it important to correctly assess the contributions and dynamics of different defects to the measured threshold voltage shift and recovery. For AC applications (e.g. ring oscillators), it is important to understand how certain defect types react to fast switching of the gate bias. For modeling attempts and to enhance the physical understanding of NBTI, studying possible correlations between different types of defect is the key.

When attempting to determine the field and temperature dependence of NBTI, discrepancies in the interpretation of experimental data can easily arise from the fact that it is quite challenging to compare degradation and recovery dynamics of devices stressed at arbitrary fields and temperatures. When applying for example the conventional measure-stress-measure (MSM) technique, the stress phase has to be interrupted continuously in order to record changes in device characteristics. To monitor, for instance, the V_{TH} shift, one has to switch the gate bias from the stress level to a (much) lower recovery level close to the threshold voltage of the device. To record changes in the charge pumping (CP) current, which is a measure of fast interface state densities, one has to switch from the constant stress bias to high frequency gate pulsing between accumulation and inversion. Because the latter is

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experimentally harder to perform, CP data is typically presented with much larger time delays compared to V_{TH} shift data. In any case, a bias change and initialization of a subsequent (recovery) measurement involves an unavoidable stress-measure time delay, which results in unknown recovery prone to distort already the first measurement point after the termination of the stress. Because of the thermal activation of relaxation, the amount of V_{TH} recovery within this time delay and the following recovery transients depend on the characterization temperature [13]. Similar conclusions hold for 'recovery-free' on-the-fly measurements, where the initial degradation in the first reference measurement point depends on the temperature as well [14].

In this work we characterize NBTI degradation and recovery of PMOS devices stressed at different temperatures and fields. As opposed to previous attempts, which were limited to the constraint that the stress temperature must equal the recovery temperature, we decouple the stress and the recovery phase in the MSM experiment by making use of the in situ polyheater technique [15,16]. In-situ polyheaters are deposited poly-Si wires which embed the active device. Our key approach is to provide identical characterization conditions within a stress-measure time delay of only 10 ms for devices stressed at almost arbitrary fields and temperatures. Using this clean characterization technique, we reexamine NBTI dynamics of threshold voltage shift and CP current and evaluate the relative contributions of different defect types involved in threshold voltage degradation and recovery.

The study is performed on isolated lateral p-channel MOSFETs equipped with 30 nm pure SiO_2 gate oxides with n++ doped poly-Si on top. Beside the economical and scientific relevance of high voltage devices [17], thick oxide transistors provide considerable benefits for NBTI characterization. For example, due to the absence of gate tunneling currents at conventional stress biases ($j_G < 10^{-7}$ A/cm^2), we do not have to correct our CP data for leakage currents or worry about non-NBTI related degradation components due to e.g. fixed oxide charges caused by impact ionization. The use of pure SiO_2 gate oxides further guarantees that our general conclusions are not distorted by the strongly process dependent impact of nitridation [18]. Our main conclusions should hold for thin dielectric transistors as well since it has recently been shown by several independent studies that the basic mechanisms of NBTI are essentially the same in thin and thick SiO_2 and SiON technologies [19–22].

2. The role of temperature in NBTI characterization

All NBTI models agree that the temperature plays a significant role in both defect creation and relaxation. This and other arguments rule out defect neutralization by elastic tunneling which is almost temperature independent. On the other hand, diffusion or inelastic tunneling processes are considerably accelerated at elevated device temperatures. Assuming an Arrhenius-like recovery process [23,24], we can define the annealing time of a positively charged defect at a recovery temperature T by

$$\tau = \tau_0 \exp\left(\frac{\Delta E_B}{kT}\right) \tag{1}$$

In (1), τ is the annealing time of an arbitrary trap at a temperature T, τ_0 is the minimum time constant at barrier height zero, ΔE_B is an effective relaxation barrier, k is the Boltzmann constant, and T is the device temperature during recovery. To determine the degradation level at the very beginning of the recovery phase and, consequently, the exact value of τ_0, sophisticated test methods have been developed in the past that accomplish ΔV_{TH} measurements only a couple of microseconds after the removal of the stress bias [25]. In most reported cases the extracted recovery curves are straight lines in a semi-logarithmic time plot, suggesting that the activation energies are more or less uniformly distributed [26,27]. On small devices, discrete steps can be observed which are due to only a handful of defects with a few characteristic annealing time constants [28,29]. The fact that in general recovery starts almost immediately after the termination of stress [25,30–32] attaches considerable importance on the transition event between the stress and the relaxation phase. Eq. (1) and the discussion above suggest that it would be most expedient to either measure as fast as possible or at the lowest temperature possible (or both) in order to capture a maximum of the actual damage at the end of stress. Note that if the recovery temperature (i.e. the characterization temperature) is much lower than the stress temperature, recovery would be decelerated significantly. The exponential decrease of the recovery time constants with temperature can be interpreted as a stretching on the time axis [23,33]. For example, let's assume traps with an average barrier height ΔE_B of 0.3 eV. If on such a device the ΔV_{TH} shift is measured with a MSM time delay of 10 ms at a temperature as low as −60 °C, a larger fraction of the degradation can be captured compared to a measurement of ΔV_{TH} with a time delay of only 1 μs at a much higher (stress) temperature of 125 °C [16,33].

In summary, a clean comparison of devices stressed at different temperatures is challenging due to the strong temperature dependence of the recovery [23]. Data recorded with the same time delay but at different temperatures is afflicted with different recovery [16,23,33]. Additional theoretical difficulties with different stress and characterization temperatures arise when attempting to correlate the measured V_{TH} shift to CP data. The CP technique, traditionally used to characterize fast interface states [34–36], is inefficient at conventional stress temperatures since it covers just a narrow range of the silicon band gap when performed at high device temperatures. To convert the CP current to a corresponding V_{TH} shift at such high temperatures, the standard practice is to assume a flat density-of-states profile for the interface traps. However, this approach is known to be a very crude approximation [37–39] which likely introduces a considerable error into CP data measured at different temperatures. Similar difficulties also arise for V_{TH} shift data recorded at the same operating point but at different characterization temperatures [16,33].

To overcome all these experimental and theoretical difficulties, devices stressed at different stress temperatures must be characterized directly post stress at the same characterization/recovery temperature. To accomplish this, one needs a tool/technique that allows for ultra-fast temperature switches. Such a tool is the recently developed polyheater measurement technique [15,16,33]. Using in situ heated devices on test structures (i.e. devices embedded between electrically-isolated poly-Si wires), we can generate different stress temperatures by applying different heater powers. The ambient (characterization) temperature is defined by the ground temperature of the thermo chuck. During stress, the chuck temperature is constant and typically set to a much lower value (e.g. -60 °C) than the stress temperature. At the end of stress, the heater is turned off and the device cools down within 1–10 s [15]. After 0.1 s, the target temperature is reached within 3% accuracy, after 1 s within 1%, and after 10 s, the device temperature is less than 0.1% away from the target temperature (i.e. the chuck temperature of e.g. −60 °C). The time required for cooling the device from typical stress temperatures down to −60 °C within 0.1% accuracy is always about 10 s. During temperature quenching, the stress field (bias) is maintained. Since recovery is dominantly triggered by the switch from the stress bias to the read-out bias (i.e. the threshold voltage), maintaining the stress bias conserves the degradation level during the short cooling phase [16,23,33]. This procedure is called 'degradation quenching'. Note that since the stress bias remains applied during the cooling phase, there is

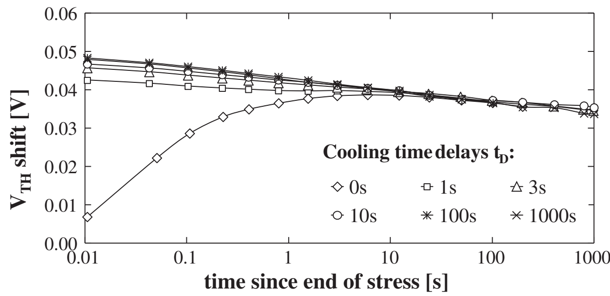


Fig. 1. Threshold voltage shift as a function of relaxation time, with delay time (t_D) as a parameter. Different devices were stressed for 1000 s at T_S = 125 °C and =6.0 MV/cm using the polyheater technique. The chuck temperature was −60 °C. After stress at 125 °C, the heater was turned off and the devices cooled down toward −60 °C. During t_D, we maintained the stress bias. After t_D, we switched the gate bias from the stress level to the threshold voltage (−1.1 V) and monitored the shift recovery for 1000 s at −60 °C. Note that for delay times t_D < 10 s, the V_{TH} shift data is afflicted with an error at the very beginning of the recovery measurement because the device was not yet at a constant target temperature. The error for t_D < 10 s is due to the fact that the reference curve for the conversion $\Delta I_D \rightarrow \Delta V_{TH}$ was recorded at −60 °C but the device was not precisely at −60 °C at the beginning of the recovery measurement. Considering this systematic error, there is neither recovery nor noticeable additional degradation for all tested delay times during t_D. This demonstrates the conservation of the degradation level during t_D.

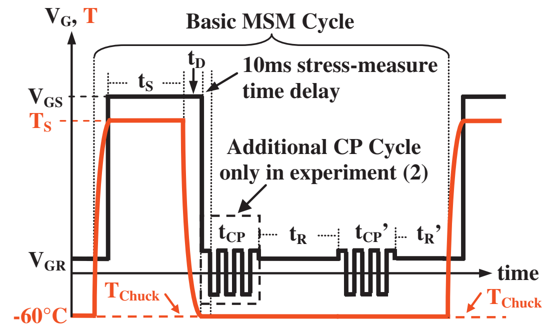


Fig. 2. A sketch of the two different MSM sequences used to monitor degradation and recovery of the V_{TH} shift and the CP current after stressing different devices at various gate biases (V_{GS}) and temperatures (T_S). During stress, the polyheater provides the stress temperature. 10 s before the recovery measurement is initiated (i.e. t_D), the heater is turned off and the device quickly cools down to a constant recovery temperature of −60 °C. Only then the gate bias is switched from the stress level to the read-out level, and this is the moment where recovery starts. Our first measurement is typically afflicted with a 10 ms recovery time delay. We subjected each device to four stress/recovery runs with increasing stress (t_S) and recovery (t_R) durations (1/10/100/1000 s). The CP cycles t_{CP} and t'_{CP} and the recovery phase t'_R each lasted for 0.5 s independently of t_S and t_R. The only difference between experiment (1) and experiment (2) is that the initial CP cycle right after stress (t_{CP}) was omitted in (1) and included in (2) (for details see text).

no recovery during cool-down, although some very small additional low-temperature degradation cannot be ruled out. This very small stress contribution, however, can be safely ignored compared to the much larger degradation during the actual stress phase performed at a much higher temperature [16,23,33]. This is demonstrated in Fig. 1. Different PMOS devices were stressed for 1000 s at 125 °C and 6.0 MV/cm. After the stress time had elapsed, the heater was turned off allowing the devices to cool down to the chuck temperature of −60 °C (with stress bias applied). The delay between turning off the heater and switching the gate bias from the stress level to V_{TH} is referred as time t_D. The true recovery time delay is the time between switching the gate bias from the stress level to V_{TH} and performing the ΔV_{TH} measurement. In Fig. 1, this time delay is labeled as 'time since end of stress'. Once the device can reach the chuck temperature (−60 °C) with sufficient accuracy (0.1%) before the measurement is initialized (>10 s after switching off the heater), the ΔV_{TH} measurements can reasonably be assessed at the same temperature and the obtained shifts and recovery traces are seen to be independent of t_D. This demonstrates the conservation of the degradation level during t_D: even with a 1000 s delay, neither more nor less shift is seen compared to a 1 s delay, which means that V_{TH}-relevant defects neither appeared nor disappeared during t_D. More detailed information on calibration and application of in situ polyheaters is given in [15,16,40].

3. Experimental setup

We designed the two MSM sequences illustrated in Fig. 2 to measure degradation and recovery dynamics of threshold voltage shift and CP current. We applied each sequence to a separate set of PMOS devices. In order to achieve a good correlation of the degradation levels after stress, devices from the same wafer were carefully selected by their virgin CP characteristics. This was done because preliminary investigations have indicated a good correlation between the degradation levels observed in equally fabricated devices provided they had identical CP characteristics before stress [16,41]. Each device set consisted of nine test structures, which were stressed at three different gate biases (−18.0/−16.0/−14.0 V) and three different stress temperatures (125/100/75 °C). The stress biases correspond to equivalent oxide electric fields of 5.6/5.0/4.3 MV/cm. During NBTS, the stress temperature was generated by applying a certain (pre-calibrated) power to the polyheater. We adjusted a low and unique characterization (i.e. recovery) temperature for all samples by setting the thermo chuck to −60 °C. During the constant bias phases (t_R and t'_R), the drain current was recorded at the threshold voltage of the device (−1.1 V). Later, changes in the drain current were converted into equivalent threshold voltage shifts [30]. During the CP phases (t_{CP} and t'_{CP}), we pulsed the gate for 0.5 s between accumulation (+1.0 V) and inversion (−2.0 V) while measuring the CP current at the substrate junction. We used a pulse frequency of 500 kHz and rising/falling times of 300 ns (rising/falling slopes of 10 V/μs).

In order to measure V_{TH} shift, CP current degradation, and recovery in an accurate manner, prior studies have shown that it is inevitable to perform experiments on two different sets of devices, because gate pulsing during CP invasively influences any subsequent V_{TH} measurements [41,42]. Experiment (1) differs from experiment (2) only in the way that the CP cycle (t_{CP}) directly after the termination of stress was omitted, leaving the V_{TH} shift measurement during t_R unaffected. In experiment (2), this CP measurement (t_{CP}) was included in order to record changes in fast interface state densities directly after stress. In both experiments, we monitored the CP current (during t'_{CP}) at the end of the constant bias recovery phase t_R and measured the V_{TH} shift (during t'_R) again after 0.5 s of gate pulsing. Each device was subjected to four subsequent stress/recovery runs (1/10/100/1000 s) with the recovery time t_R equaling the stress time t_S.

4. Results and general observations

The V_{TH} shifts recorded during t_R in experiment (1) are illustrated in Fig. 3. For clarity, we have grouped different stress biases and stress temperatures in nine separate graphs on the left hand side of Fig. 3. There are four separate measurement curves in each graph corresponding to the four subsequent stress/recovery runs (1/10/100/1000 s). The V_{TH} shift increases with stress time, stress bias and stress temperature. Within the observed experimental window, all recovery traces show a perfectly linear decrease on the semi-logarithmic time plot. Two features define the shape of the recovery traces: (i) the slope (mV/decade) and (ii) the offset at an arbitrary time. Considering that every recoverable defect

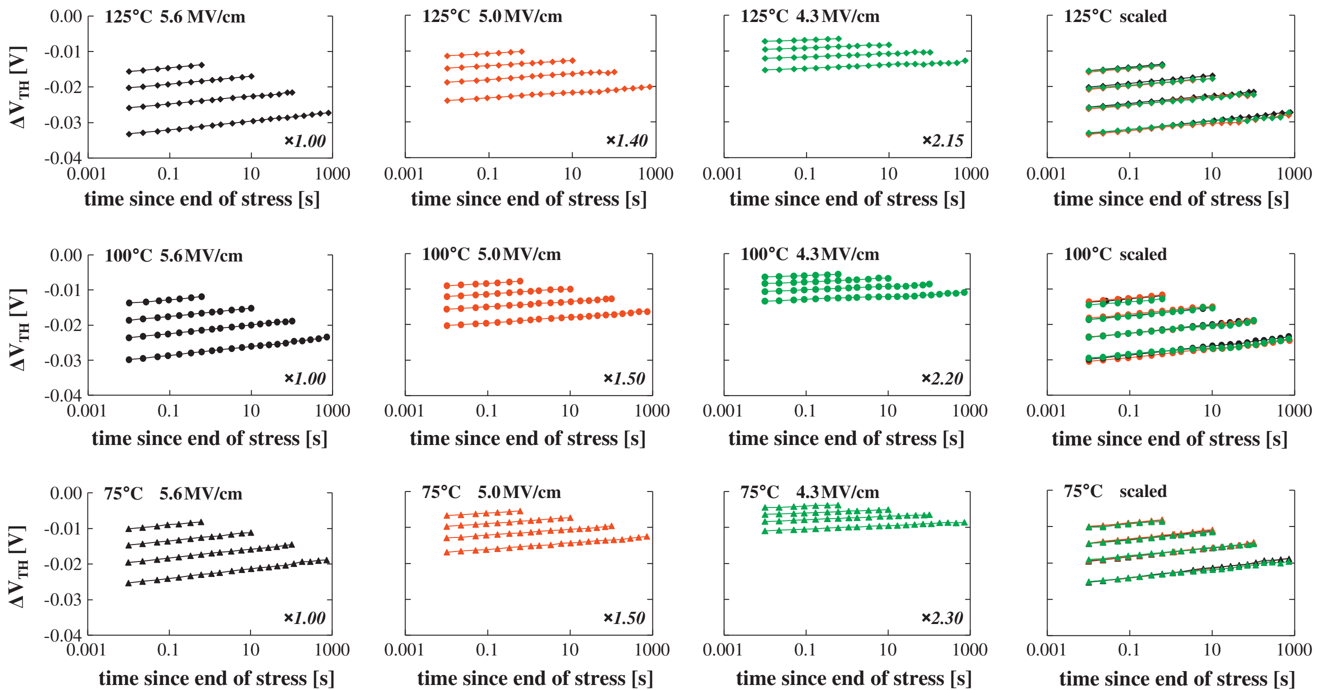


Fig. 3. ΔV_{TH} recovery traces measured during t_R at −60 °C in experiment (1). Nine different devices were stressed for 1/10/100/1000 s using three different stress temperatures (125/100/75 °C) and three different oxide fields (5.6/5.0/4.3 MV/cm). The results for different stress fields are illustrated from left to right, while different stress temperatures are illustrated as diamonds (125 °C), circles (100 °C) and triangles (75 °C) from the top to the bottom. On the right hand side, we show the raw data multiplied by appropriate scaling factors (factors are displayed in the lower right corner of each figure). Perfect scalability can be obtained for devices which were stressed at one particular stress temperature but different stress fields. The field-scaling factors for different stress temperatures are very similar. V_{TH} shifts recorded for different stress times and different stress temperatures are shifted parallel on the y-scale.

has a particular time constant that equals a point in time at which the probability of relaxation is largest, a steeper recovery slope indicates a larger number of recoverable defects with similar (short) time constants, whereas a larger offset on the y-axis (ΔV_{TH}) indicates a larger number of defects with recovery time constants longer than the duration of our recovery experiment [33]. Fig. 3 shows that provided the V_{TH} shifts after stress are measured at identical characterization conditions (bias and temperature), the stress field influences mainly the recovery slope whereas stress time and temperature shift the recovery traces by an additive constant. This is more obvious in Fig. 4, where we show the recovery slopes in mV/decade for all stress biases and stress temperatures as a function of the stress time. In fact, one can find a set of empirical scaling factors for each stress temperature that make the recovery traces in Fig. 3 overlap for different stress fields, c.f. right hand side of Fig. 3. Remarkably, these scaling factors are virtually identical for all tested stress temperatures. The scalability for different stress biases is consistent with classical MSM measurements where the stress temperature equals the recovery temperature

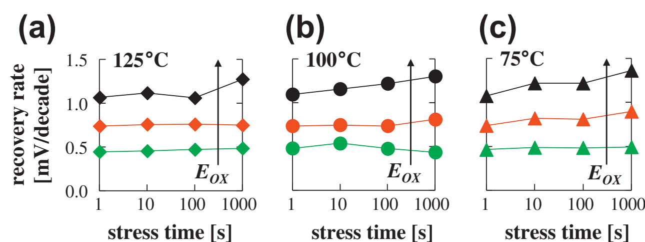


Fig. 4. Recovery rates (slopes of the recovery curves per decade) extracted from the data of Fig. 3. Different stress temperatures are illustrated as diamonds (125 °C), circles (100 °C) and triangles (75 °C). The stress field has a significant influence on the recovery rate. Stress time and stress temperature leave the recovery rates almost unaffected.

[6,7]. However, in the classical MSM approach the scaling factors did not coincide for different stress temperatures. In Fig. 3, devices stressed at different temperatures at the same stress bias show an offset in their V_{TH} recovery traces. This is different from results obtained by conventional MSM measurements which showed scalability for different stress biases *and* different stress temperatures [6,7]. The discrepancy is most likely due to the different characterization temperatures in the classical MSM approach which are known to affect the recovery rates.

Experiment (2) was performed to check whether recovery of fast interface defects (defects which contribute to 500 kHz CP) plays a significant role in the V_{TH} recovery illustrated in Fig. 3. Therefore, we compared CP currents recorded during t'_{CP} in experiment (1) to CP currents recorded during t_{CP} in experiment (2). Between t_{CP} and t'_{CP} the V_{TH} recovery was measured at a constant bias (t_R). Changes in the CP current (ΔI_{CP}) after different stress times are illustrated in Fig. 5a and b. The results for a stress temperature of 125 °C and a stress field of 5.6 MV/cm are representative for all other stress conditions which show similar characteristics and lead to the same conclusions. Remarkably, both experiments show very similar ΔI_{CP} values, although the CP measurement of experiment (1) is afflicted with a much larger stress-measure time delay (i.e. t_R). This indicates that the type of defect which contributes to CP is 'quasi-permanent' during t_R at −60 °C. Thus, this defect type cannot be responsible for the obtained V_{TH} recovery illustrated in Fig. 3. In the following, we denote defects which do not anneal within the scope of the performed recovery experiment as 'quasi-permanent'. We remark that this does not imply that these defects are permanent forever (or at all temperatures) [5,42,43]; however, such defects would appear permanent in comparison to other defects which recover on a much shorter time scale [5,42].

The finding that the defects which contribute to CP are 'quasi-permanent' during constant bias recovery is in contradiction to results obtained by on-the-fly charge-pumping (OTFIT)

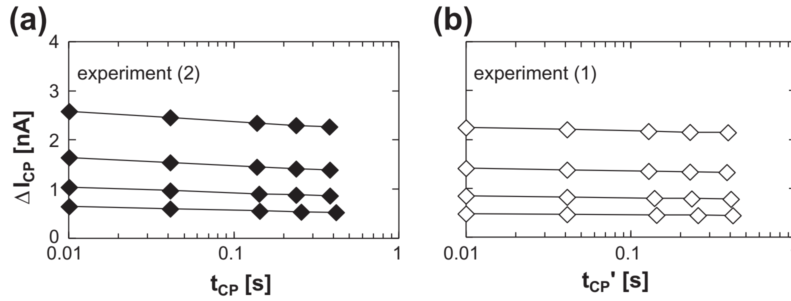


Fig. 5. Comparison of CP currents (ΔI_{CP}) after different stress times (1/10/100/1000 s) recorded at −60 °C. Stress conditions: 125 °C and 5.6 MV/cm. Due to effects of charge pumping on recovery, the different experiments have been carried out on different devices of the same wafer, carefully selected to be virtually identical by comparing electrical responses (and D_{it}) prior to any stress. The data in experiment (2) in (a) has been measured with only 10 ms stress-measure time delay between the removal of the stress bias and the CP measurement (full symbols). The data in experiment (1) in (b) has been measured with different stress-measure time delays t_R (1/10/100/1000 s) during which the device was biased at a constant gate voltage of −1.1 V (open symbols). Although the data in (b) is afflicted with a much longer stress-measure delay than the data in (a), the CP currents of experiment (1) and (2) are very similar. Thus, defects contributing to CP can be considered 'quasi-permanent' during t_R.

measurements reported in [44]. The disagreement could be a consequence of our low characterization temperature (−60 °C). Other possible reasons are given in [45].

5. Correlation between fast interface states and the total V_{TH} Shift

Having measured time, bias, and temperature dependent V_{TH} shifts as well as CP current degradation and recovery at identical characterization conditions, we proceed to check whether there is any correlation between the number of defects contributing to the CP signal and the total V_{TH} shift. To compare these two quantities, one has to convert the increase in the CP current (ΔI_{CP}) into an equivalent threshold voltage shift due to fast interface states (ΔV_{TH}^{it}). Similar attempts have been made by others, however, previous studies were always bound to the constraint that the analyzing temperature equals the stress temperature, the implications of which being quite significant, as will be shown in the following.

To accomplish the conversion from ΔI_{CP} into ΔV_{TH}^{it}, it is crucial to consider that the V_{TH} shift measurement (performed at DC gate bias) and the CP measurement (performed with pulsed gate bias) in general probe different ranges of the silicon band gap (ΔE_{VTH} and ΔE_{CP}). Furthermore, one has to consider the amphoteric nature of the fast interface traps contributing to CP [46,47]. In Si/SiO_2 systems these traps are most likely P_b centers [26]. P_b centers have their amphoteric transition level around mid-gap, i.e. the intrinsic Fermi level (E_i) [48,49]. Traps above E_i are considered as acceptor-like while traps below E_i are treated as donor-like. When measuring the V_{TH} shift at a particular read-out gate bias (V_{GR}), the Fermi level position (E_f) at the interface governs the charge state of the traps. At $V_{GR} = -1.1V$ and at −60 °C, E_f was simulated numerically (process simulator TSUPREM4; device simulator MEDICI) to be about E_V + 120 meV [50]. Due to the amphoteric nature of P_b centers, the states in the lower half of the silicon band gap (between E_i and E_f) are positively charged; traps above mid-gap are neutral → $\Delta E_{VTH} = E_i - E_f$.

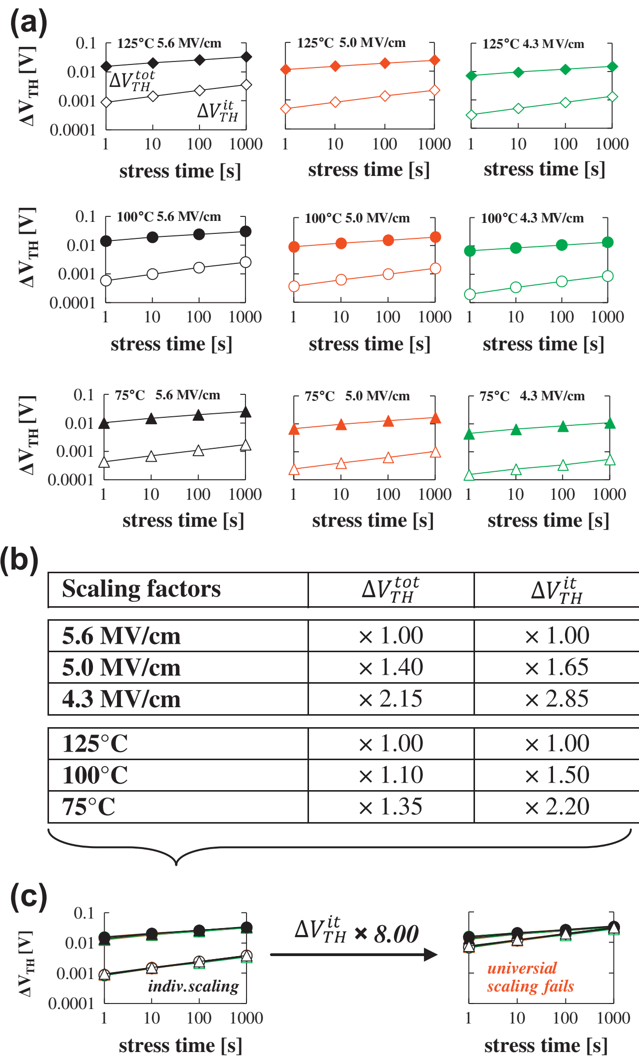
Following [35], we can also calculate the probed energy range during CP (ΔE_{CP}). At −60 °C and using our pulse setup, we obtain ΔE_{CP} = 800 meV, where we have assumed an energetically homogeneous capture cross section of $\sigma = 10^{-15}$ cm^2 [51,52]. The lower boundary of ΔE_{CP} (i.e. E_V + 150meV) almost perfectly coincides with the Fermi level position at V_{GR} (i.e. E_V + 120 meV). That is a particular benefit of our low characterization temperature (−60 °C). At typical stress temperatures (100 °C → 175 °C) and using the same pulse setup, ΔE_{CP} probes a considerably narrower fraction of the silicon band gap (500 meV → 300 meV). This leads to a significant mismatch between ΔE_{CP} and ΔE_{VTH} To account for the mismatch in the conversion, one has to assume a particular density-of-states profile. Using a characterization temperature of −60 °C, such an assumption is not required because ΔE_{CP} probes nearly the whole range of ΔE_{VTH}. Since we used a symmetrical pulse shape, ΔE_{CP} also probes about the same energy range in the upper half of the silicon band gap [35]. To exclude the neutral defect states above mid-gap in the conversion, we divide the CP current by a factor 2. This is reasonable since the density-of-states profile of fast interface traps is to a very good approximation symmetric around mid-gap [48,49,53]. The threshold voltage shift due to fast interface states (ΔV_{TH}^{it}) is then given by

$$\Delta V_{TH}^{it} \approx \frac{\Delta Q_{it}}{C_{OX}} = \frac{\Delta I_{CP}}{2fAC_{OX}} \quad (2)$$

In (2), ΔQ_{it} is the increase in positive interface charge, C_{OX} is the specific oxide capacitance, A is the device area, ΔI_{CP} is the increase of the maximum CP current and f is the gate pulsing frequency. Using (2), we can calculate ΔV_{TH}^{it} from ΔI_{CP} for every stress bias, stress temperature and stress time.

Fig. 6 illustrates an attempt to scale ΔV_{TH}^{tot} and ΔV_{TH}^{it}. We compare ΔV_{TH}^{tot} recorded 10 ms post stress in experiment (1) to ΔV_{TH}^{it} recorded (via CP) 10 ms post stress in experiment (2). In (a), ΔV_{TH}^{tot} and ΔV_{TH}^{it} are illustrated as a function of the stress time for all tested stress fields and stress temperatures. Both shifts show a power law-like increase with stress time (t_S): $\Delta V_{TH}^{it} \propto t_S^{n_{it}} and \Delta V_{TH}^{tot} \propto t_S^{n_{tot}}$, with n_{it} and n_{tot} being the characteristic power law exponents. Two different sets of scaling factors had to be used to scale ΔV_{TH}^{tot} and ΔV_{TH}^{it} individually for different stress conditions, c.f.(b) and (c). By multiplying the scaled ΔV_{TH}^{it} shifts with a factor of eight, scalability can be n_{it} obtained for a stress time of 1000 s but fails for all shorter stress times. The fact that ΔV_{TH}^{tot} and ΔV_{TH}^{it} are not simply proportional to each other indicates that they are most likely not coupled in a direct way.

In Fig. 7, the extracted power law exponents of ΔV_{TH}^{tot} (n_{tot}) and ΔV_{TH}^{it} (n_{it}) are illustrated for different stress temperatures and stress fields. Apparently, n_{it} and n_{tot} differ by almost a factor of two, the first being around 0.22 while the latter is around 0.12. The different degradation dynamics emerge because in DC V_{TH} measurements (Fig. 3), different types of traps contribute to the power law exponent (n_{tot}) whereas in CP measurements performed at high frequencies (500 kHz) and with moderate pulse amplitudes, the majority of contributing traps are fast interface states (n_{it}). This finding is consistent with the results of Teo et al. [54] on p-channel MOSFETs with 2.8 nm SiO_2 gate dielectrics. Using CP with ultra-fast 100 ns pulses, they found a power law exponent of roughly 0.15 (c.f. 0.12). Using a conventional CP MSM sequence, they reported a considerably reduced CP current and a different



Scaling factors	ΔV_{TH}^{tot}	ΔV_{TH}^{it}
5.6 MV/cm	× 1.00	× 1.00
5.0 MV/cm	× 1.40	× 1.65
4.3 MV/cm	× 2.15	× 2.85
125°C	× 1.00	× 1.00
100°C	× 1.10	× 1.50
75°C	× 1.35	× 2.20

Fig. 6. A scaling attempt of ΔV_{TH}^{tot} (full symbols) and ΔV_{TH}^{it} (open symbols). The unscaled V_{TH} shifts, recorded 10 ms after stress, are illustrated as a function of the stress time in (a). Different stress temperatures are illustrated by diamonds (125 °C), circles (100 °C) and triangles (75 °C). One can find two different sets of scaling factors that make the two individual V_{TH} shifts overlap for all stress temperatures and stress fields, c.f. (b and c). However, universal scalability between ΔV_{TH}^{tot} and ΔV_{TH}^{it} cannot be obtained. ΔV_{TH}^{tot} and ΔV_{TH}^{it} are not proportional to each other.

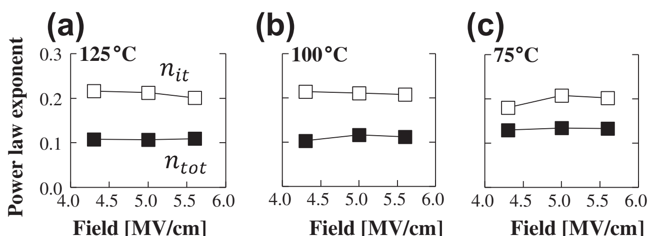


Fig. 7. The power law exponents of ΔV_{TH}^{tot} (n_{tot}-full symbols) and ΔV_{TH}^{it} (n_{it}-open symbols) illustrated as a function of the stress field. n_{it} (≈0.22) is about a factor 2 larger than n_{tot} (≈0.12). Stress bias and temperature do not seem to affect the power law exponents significantly within the experimental range.

power law exponent of 0.25–0.27 (c.f. 0.22). The discrepancy was attributed to the contribution of fast interfacial oxide traps which can constitute a significant contribution to the CP current at high temperatures, low gate pulsing frequencies, and large gate pulsing amplitudes, e.g. when the pulse levels are re-used as stress bias. The same conclusions were also drawn by Hehenberger et al. in [45]. Since we perform CP at −60 °C applying 500 kHz gate pulses with only 3.0 V pulse amplitudes to 30 nm dielectrics, our CP measurements can be considered "conventional" and virtually unaffected by near interfacial oxide traps. Most of these traps recover either within the switching time delay between the end of DC stress and the start of AC gate pulsing during which the gate is floating or during the CP measurement itself.

Within the range of our experiment (75–125 °C), the exponents n_{it} and n_{tot} appear almost independent of the stress temperature and the stress field. While independence of the electric field was already observed by others, independence of the stress temperature is in contradiction to most previous studies [43,55] that suggested a *kT*-like increase of n_{it} with the stress temperature. Teo et al. [54] attributed the apparent variations in the power-law exponents with temperature to an artifact due to different activation energies of oxide and interface trap generation. Another reason could be the temperature dependence of the scanned energy range during CP [35]. In our experiments, we measure CP only 10 ms post stress always at the *same low* characterization temperature while others compare CP currents measured with larger time delay at *different and much higher* temperatures where different regions of the silicon band gap (ΔE_{CP}) are probed. It has been shown [41,42] that long continuous gate pulsing at elevated temperatures leads to enhanced recovery of the CP current, a phenomenon possibly linked to a process known as recombination enhanced defect reaction [56,57].

To check whether the reported larger values of n_{it} and its strong temperature V_{TH} dependence are measurement artifacts due to different characterization temperatures, we have repeated experiment (2) on our devices using the conventional MSM approach, where the stress temperature *equals* the recovery temperature (stress field 5.6 MV/cm). The results are compared to our original data in Fig. 8. Consistent with our hypothesis, the conventional MSM technique gives completely different power law exponents for n_{it} which also increase with temperature, just as reported in literature [43,45,58,59].

All evidence collected in these experiments suggests that the total V_{TH} shift must be due to at least two or more different types of defects which have different bias and temperature acceleration as well as different recovery behavior. One of them recovers readily as a function of bias, temperature and time while the other appears 'quasi-permanent' within the scope of our experiment. Consistent with previous studies [5,43,62], we believe that the 'quasi-permanent' fraction in the total shift is related to the defects detected in

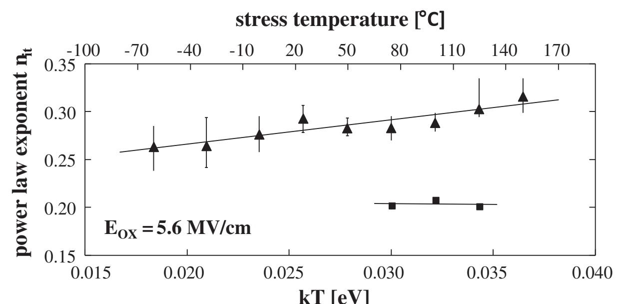
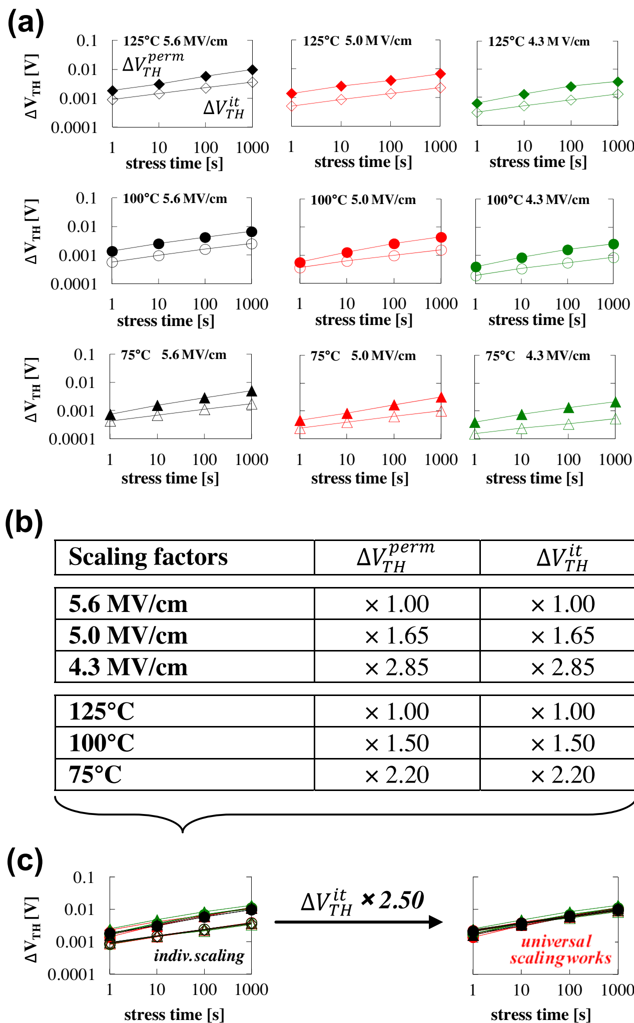


Fig. 8. The power law exponent n_{it} as a function of the stress temperature; (i) measured in the conventional MSM scheme with the stress temperature *equaling* the recovery temperature (triangles); (ii) using our new approach with a constant recovery temperature of −60 °C (squares). Using the conventional MSM scheme, n_{it} clearly increases with stress/characterization temperature. Using a constant recovery temperature of −60 °C, the values for n_{it} are smaller and almost independent of the stress temperature within the experimental range.

CP, while the fast recoverable fraction is of somewhat different origin. To retrieve the 'quasi-permanent' component (ΔV_{TH}^{perm}) from the total V_{TH} shift (ΔV_{TH}^{tot}), we have the option to either monitor constant bias recovery at V_{TH} until the curves flatten, which may take more than 10^{10} seconds [42,45,60], or try to accelerate the recovery by providing electrons at the interface [6,32,61–62], i.e. biasing the device for a short time in accumulation. Practicability dictates the use of the latter method. During CP, the gate bias is switched periodically from inversion to accumulation. After CP, we obtain a considerably smaller and virtually constant ΔV_{TH} degradation level (not shown). This suggests that most recoverable components (with short time constants) have been annealed. It should be noted, however, that recovery will eventually continue after a long enough time interval [23,33].

In Fig. 9 we compare the 'quasi-permanent' V_{TH} shift (ΔV_{TH}^{perm}), recorded during t'_R in experiment (1), to ΔV_{TH}^{it}, calculated from the CP current in experiment (2). In (a), ΔV_{TH}^{perm} and ΔV_{TH}^{it} are illustrated as a function of the stress time for all analyzed stress biases and stress temperatures. We obtain almost exactly the same bias and temperature scaling factors for ΔV_{TH}^{perm} and ΔV_{TH}^{it}, c.f. (b). In (c), the scaled V_{TH} shifts are illustrated as a function of the stress time. The evolutions of ΔV_{TH}^{perm} and ΔV_{TH}^{it} are almost parallel, indicating similar power law factors and a direct correlation between the two components. However, apparently the magnitude of ΔV_{TH}^{perm} and ΔV_{TH}^{it} is not the same. In fact, ΔV_{TH}^{it} is universally about a factor 2.5 smaller than ΔV_{TH}^{perm}. If ΔV_{TH}^{perm} would be exclusively due to defects which also contribute to the CP current, ΔV_{TH}^{it} and ΔV_{TH}^{perm} would be identical which would give a scaling factor of one. The actually obtained scaling factor of 2.5 indicates that the defects detected in CP only account for about 50% of the total 'quasi-permanent' damage in the V_{TH} shift. This suggests that ΔV_{TH}^{perm} most likely includes another type of positively charged defect which is tightly related to fast interface states but does not show up in the CP measurement [63–65].



Scaling factors	ΔV_{TH}^{perm}	ΔV_{TH}^{it}
5.6 MV/cm	× 1.00	× 1.00
5.0 MV/cm	× 1.65	× 1.65
4.3 MV/cm	× 2.85	× 2.85
125°C	× 1.00	× 1.00
100°C	× 1.50	× 1.50
75°C	× 2.20	× 2.20

Fig. 9. A scaling attempt of ΔV_{TH}^{perm} (full symbols) and ΔV_{TH}^{it} (open symbols). The unscaled data, obtained 10 ms post stress, is depicted in (a) as a function of the stress time. Different stress temperatures are illustrated by diamonds (125 °C), circles (100 °C) and triangles (75 °C). Remarkably, *one single* set of scaling factors is sufficient to make the individual V_{TH} shifts overlap for all stress temperatures, stress fields and stress times, c.f. (b and c). Also, universal scalability (factor 2.5) between ΔV_{TH}^{perm} and ΔV_{TH}^{it} can be obtained. This is strong indication for a tight coupling of the two quantities.

Alternatively, one may argue that ΔV_{TH}^{it} could have been underestimated in (2) by making the assumption of an amphoteric nature of fast interface traps. In fact, ΔV_{TH}^{it} would be about a factor of two larger when assuming pure donor-like interface defects which cover the whole silicon band gap [18]. However, such an assumption would be in contradiction with most of the defect literature. For example, it has been shown that fast interface states charge up negatively in NMOS devices, where the Fermi level is pinned close to the conduction band edge at the threshold voltage, causing a net smaller or even positive threshold voltage shift after NBTS [2,44].

6. Discussion on the defect structure

Our results indicate three different types of NBTS induced defects: (i) a defect which recovers readily as a function of bias and temperature, (ii) another positive defect which cannot be annealed easily by biasing the device in accumulation and which does not contribute to CP at −60 °C and 500 kHz; this defect is considered 'quasi-permanent' since it has recovery time constants beyond the range of our experiments and (iii) fast interface states that contribute to CP; these defects were found 'quasi permanent' too, at least as long as the device is biased at the negative threshold voltage at -60 °C. We could further establish a universal correlation between defect type (ii) and defect type (iii). The defects are created at virtually the same rate and in a ratio of approximately 50:50 [5].

While electrical measurements can study densities, energy levels and time constants of traps, they do not provide information on the microscopic nature of point defects. Electron paramagnetic resonance (EPR) [66] and electrically detected magnetic resonance (EDMR) [67] have the analytical power to study the atomistic structure of defects. EPR and EDMR studies of irradiated Si/SiO_2 systems have revealed E' and P_b centers [68,69]. The E' center is an oxide defect which consists of a dangling bond on a silicon atom and an adjacent positive defect in a puckered configuration (the $E'\gamma$ center) [70,71]. The P_b center is a dangling bond defect on a silicon, located at the semiconductor/oxide interface. P_b centers are conventionally assumed to be created through hydrogen release from passivated Si–H bonds at the interface. Recent EPR investigations [72] and EDMR studies via spin dependent recombination [73,74] have shown that similar defect types also emerge after NBTS in significant portion. In the following, we attempt to relate the three different defect types to defects identified with EPR and EDMR. For better readability, the different defect types, their recovery behavior, their appearance in the electrical measurement as well as their possibly related point defect are summarized in Table 1.

Defect (i): It is known from random telegraph noise and EPR experiments that near interfacial oxide defects like E' centers can act as a switching traps which can be either positively charged or neutral, depending on the Fermi level position at the interface [75,76]. A microscopic degradation/recovery model developed by

Table 1
Summary of defect characteristics.

Defect Type	Annealing behavior	Detection in electrical measurement	Possible point defect
Defect i	Recovers readily with time, bias and temperature	Recoverable fraction of ΔV_{TH}^{tot}	Oxide defect, E' center
Defect iii	Quasi-permanent, no annealing by bias	CP current related fraction of ΔV_{TH}^{perm}	Interface defect, P_b center
Defect ii	Quasi-permanent, no annealing by bias	Difference between ΔV_{TH}^{perm} and ΔV_{TH}^{it}	Oxide defect proportional to P_b center

Lelis et al. [77] and extended by Grasser et al. [6,78,79] suggests oxygen vacancies close to the interface as precursors for E' centers. In the positive charge state, the E' center is stable. In the neutral charge state, after capturing an electron from the substrate, the E' center may undergo a structural relaxation which anneals the defect permanently by reforming the oxygen vacancy precursor. This behavior is very similar to our recoverable defect (i). Thus, it is likely that defect (i) is the E' center.

Defect (iii): These defects are traps which can respond to 500 kHz gate pulsing at −60 °C (i.e. CP). From EPR and EDMR studies it is well known that P_b centers exist at the Si/SiO_2 interface and that they follow fast Shockley–Read-Hall like trapping/detrapping. Thus, defect (iii) is most likely the P_b center. It should be noted that E' centers close to the semiconductor/oxide interface can under certain circumstances also contribute to the CP current [42,45,54]. However, as already pointed out previously, the relative contribution of E' centers to the CP current is only relevant at low pulsing frequencies, large pulse amplitudes and high temperatures, c.f. for instance Hehenberger et al. in Ref. [45].

Defect (ii): These defects are positively charged traps which contribute to the V_{TH} shift but do not respond to 500 kHz CP at −60 °C. The microscopic origin of defect (ii) is, at the present state of knowledge, not fully clear. One might argue that defect (ii) is simply a more stable variant of defect (i) with considerably longer response/recovery times (e.g. an E' center deeper in the oxide or with a different energy level). However, our measurement data does not support this idea. The lacking correlation between defect (i) and defect (ii) suggest a different microscopic structure of defect (ii). EPR studies [80,81] and theoretical studies using density functional theory calculations [82–85] suggest E' center-hydrogen complexes and/or P_b center-hydrogen complexes [86] as possible alternatives. If such hydrogen centers exist, the obtained correlation between defect (iii) and defect (ii) could be due to a mechanism involving hydrogen transition between Si–H bonds at the interface and E' centers in the oxide [6,87,88]. The release of hydrogen from the Si–H bond would create a P_b center; the capture of hydrogen at the E' center's dangling bond site would block its recovery and lock its positive defect site in a puckered configuration. A correlation between NBTI induced amphoteric interface states and fixed positive oxide charges was also suggested by Ushio et al. [89] for Si/SiO_2 and Si/SiO_xN_y interfaces based on density functional calculations. They explained the simultaneous creation of fixed positive oxide charges and interface states through Si–H bond breakage (which leaves behind an amphoteric P_b center) and subsequent H capture at a Si–O–Si group within the gate-oxide, near the interface. The H transition is promoted by hole capture thereby forming a positive oxide charge. Consistent with our results, Denais et al. [90] also reported three different types of traps, namely interface trapped charges, fixed charges and oxide trapped holes for advanced node technologies containing nitrogen and Aoulaiche et al. [91] for high-κ metal gates.

7. Conclusions

We have measured V_{TH} shift and CP current dynamics of identically processed PMOS devices, stressed at different electric fields and temperatures. By making use of degradation quenching and the polyheater technique, devices stressed at various temperatures and fields could be characterized right after stress at a *much lower and unique* characterization temperature. Our investigations reveal that the degradation and recovery dynamics of V_{TH} shifts and CP currents are different and widely uncorrelated. While the CP current seems to be almost permanent at −60 °C, the V_{TH} shift recovers readily after the removal of the stress bias. We attributed the different behavior and the lack in universal scalability to a recoverable oxide defect which shows up in the V_{TH} shift, but does not contribute to the CP current. We have shown that the number of recoverable defects with similar (short) time constants is mainly determined by the stress field, while defects with larger time constants are more likely generated at higher stress temperatures and longer stress times. Once the majority of the recoverable component has been removed from the total V_{TH} shift (e.g. by gate pulsing), universal scalability between the CP current and the remaining 'quasi-permanent' V_{TH} shift is obtained. However, only about 50% of the 'quasi-permanent' fraction of the V_{TH} shift can be explained by fast interface states. This suggests a third type of defect which is 'quasi-permanent' and strongly coupled to the formation of fast interface states. By comparing our observations to characteristics of various point defects reported in literature, we found good agreement between the fast recoverable defect and the E' center as well as between the CP defect and the P_b center. The structure of the third defect which is created at virtually the same rate as the P_b center remains uncertain at the present date. The defect may be created through hydrogen exchange between passivated P_b centers (Si−H bonds) and recoverable E' centers or alternatively through hydrogen exchange between passivated P_b centers and Si–O–Si groups. Such reactions or similar hydrogen transitions between Si−H bonds at the interface and intrinsic interface/oxide defects could explain the universal coupling of the 'quasi-permanent' V_{TH} shift and the CP current.

Acknowledgments

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