Microelectronics Reliability 54 (2014) 2310–2314

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Mixture of negative bias temperature instability and hot-carrier driven threshold voltage degradation of 130 nm technology p-channel transistors

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ARTICLE INFO

Article history:
Received 26 June 2014
Accepted 8 July 2014
Available online 20 August 2014

Keywords:
Hot-carrier Degradation (HCD)
Negative bias temperature instability (NBTI)
Recovery
Capture emission time maps
Stress voltage matrix
Drift minimum

ABSTRACT

We present measurement results in form of threshold voltage drift plots, recovery traces and continuous capture emission time maps (CET maps) including Negative Bias Temperature Instability (NBTI) and Hot-Carrier driven Degradation (HCD). The measurements were performed on a 130 nm MOS transistor technology which is used for automotive and analog applications and has a nominal voltage of 1.5 V. Devices of $l = 100$ nm, $w = 10$ µm have been stressed using a 2-dimensional parameter space of gate and drain voltage combinations at elevated temperature (125 °C). The chosen stress conditions include the homogeneous ($V_{ds} = 0$) and inhomogeneous ($V_{ds} \ll V_{nom}$) NBTI case, the pure HCD ($V_{gs} < V_{nom}$) case as well as the mixture of NBTI and HCD. The results clearly show that for increasing $V_{ds} > V_{nom}$ NBTI recovery becomes less severe and mainly the permanent degradation due to HCD endures after the end of stress. Furthermore there is a drift minimum of NBTI observable for a specific V_{ds}. Using CET maps it is quite evident that for high stress times the probability density of emission becomes very small whereas for shorter stress times there is a recoverable component notable.

1. Introduction

Typically, devices are either tested under NBTI or HCD critical stress conditions and their interplay is not analyzed in detail. On the other hand for analog circuits this knowledge is urgently needed to estimate the degradation of the device during its life time. For modern technologies with small channel lengths it was shown that the drift caused by HCD can only be described correctly by considering both the influence of the drain and gate voltage [1] because different drift effects can either be facilitated by single or by multiple particle mechanisms. The results of this work underline that also for NBTI there are several drift effects possible and therefore also the influence of the gate and drain voltage needs to be taken into account. Because of that the analysis of only the homogeneous NBTI case ($V_{ds} = 0$) is insufficient and also several inhomogeneous NBTI ($V_{ds} \ll V_{nom}$) conditions, the mixture of NBTI and HCD ($V_{gs} > V_{nom}, V_{ds} > V_{nom}$) and pure HCD ($V_{gs} < V_{nom}$) need to be taken into account. The findings can be directly implemented into a voltage based transistor degradation model to allow more realistic circuit simulations where a full V_{ds} and V_{gs} dependence and a detailed picture of the time behavior [2] are needed. This covers not only digital circuits where e.g. the hot-carrier degradation of inverters is dependent on the rise and fall times of the used gates but also analog circuits where comparators, current mirrors or I/O devices are implemented. Therefore only the analysis of the results of a 2-dimensional stress voltage matrix gives a complete picture of the drift behavior under various stress modes.

2. Measurements

The measurements were performed on production quality pFETs with 2.2 nm thick plasma nitrided single gate oxides.

The threshold voltage was measured by an ultra-fast measurement setup with a measurement delay after stress of 10^{-6} s using a measure-stress-measure technique. For each stress time in the range 1 s, ..., 10^4 s a 10^4 s recovery curve was recorded. For stress times below 1 s the recovery traces were recorded until the change of the threshold voltage over time was negligible. The cumulative stress time of each experiment was 1.1×10^4 s.

Data from a wide range of drain and gate voltages (36 combinations, Fig. 1), additional homogeneous NBTI ($V_{ds} = 0, V_{gs} =$

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http://dx.doi.org/10.1016/j.microrel.2014.07.040
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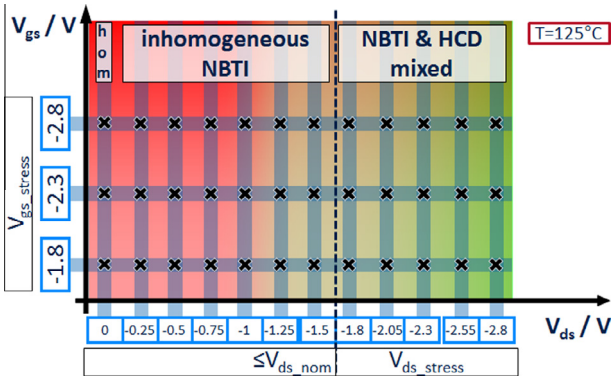


Fig. 1. Stress voltage matrix (2-dimensional parameter space with combinations of V_{gs} and V_{ds}). The experiments were performed at 125 °C. Crossings denote a measurement condition. The pure HCD conditions are not included in this graph.

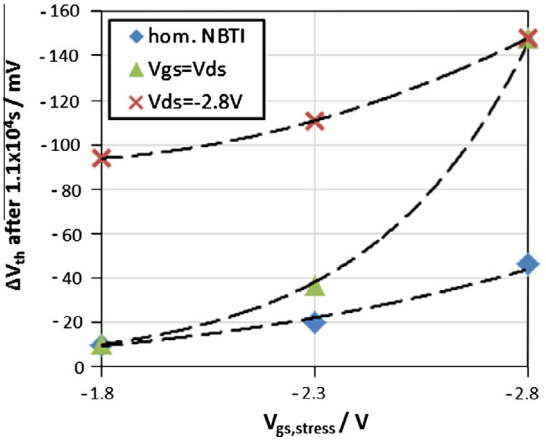


Fig. 3. Drift of different stress voltage regimes, homogeneous NBTI ($V_{ds} = 0$), NBTI mixed with HCD where $V_{ds} = V_{gs}$ and where $V_{ds} = -2.8$ V. The lowest degradation is observable for homogeneous NBTI (blue), drain stress voltages lead to higher degradation (green, red). Lines are guides to the eyes. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

$(-1.9, \ldots, -2.7)$ V) as well as pure HCD stress measurements have been recorded ($V_{ds} = (-1.8, \ldots, -2.8)$ V, $V_{gs} = (0, \ldots, -1.5)$ V) to give a full picture of the drift behavior in the inversion region.

3. Results

The threshold voltage drift (after a measurement delay of 10^{-6} s) for a given V_{gs}, V_{ds} combination after 1.1×10^4 s at 125 °C is presented in Fig. 2. A comparison of the drift results for different stress voltage regimes is shown in Fig. 3.

For homogeneous NBTI stress ($V_{ds} = 0$) the threshold voltage drift shows an increase with the absolute applied gate stress voltage. The maximum drift at $V_{gs} = -2.8$ V is 31% of the mixed HCD and NBTI stress condition ($V_{gs} = V_{ds} = -2.8$ V). For a gate voltage of −2.3 V the fraction is 13% and for $V_{gs} = -1.8$ V 7%.

The degradation results for inhomogeneous NBTI ($V_{ds} < V_{nom}$) show a drift minimum at ($V_{ds} = -0.5$ V) (Fig. 4).

For the mixed stress condition $V_{gs} = V_{ds}$ the drift also shows an increase with the absolute applied gate stress voltage. The drift amount compared to $V_{gs} = V_{ds} = -2.8$ V is 25% at $V_{gs} = V_{ds} = -2.3$ V and about 7% at $V_{gs} = V_{ds} = -1.8$ V.

The results for $V_{gs} = -1.8, \ldots, -2.8$ V, $V_{ds} = -2.8$ V show the highest degradation of the threshold voltage. Here the drift at $V_{gs} = -1.8$ V, $V_{ds} = -2.8$ V is 63% and at $V_{gs} = -2.3$ V, $V_{ds} = -2.8$ V 75% of the maximum drift which is around 148 mV.

The recovery traces of homogeneous NBTI show the well-known recovery behavior (Fig. 5(a)). The longer the stress time the longer the recovery of the threshold voltage degradation can be observed. At this stress condition the maximum change of the threshold voltage within one recovery trace can be found after the longest stress time of 10^4 s which is about 32 mV (Fig. 6(e)). In addition to that the CET maps [4,5] for homogeneous NBTI clearly show that the threshold voltage recovers from its degradation for all stress decades (Fig. 6(a)).

Interestingly, at the inhomogeneous NBTI stress voltage condition causing the observed drift minimum, the recoverable component is slightly shifted to longer emission and shorter capture times Fig. 6(b).

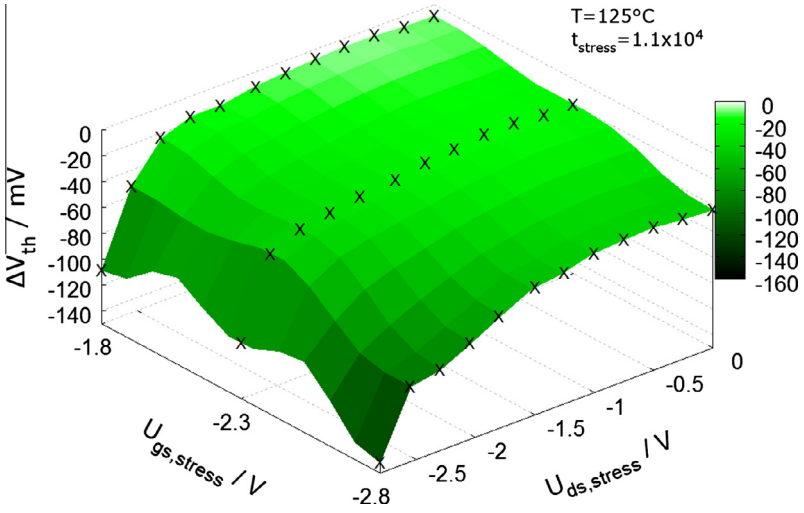


Fig. 2. Stress voltage matrix results showing the threshold voltage drift after 1.1×10^4 s at 125 °C. With increasing V_{gs} NBTI becomes more severe and with increasing V_{ds} HCD becomes more severe. The maximum drift for each series of fixed V_{gs} is dominated by HCD (x: measured data point).

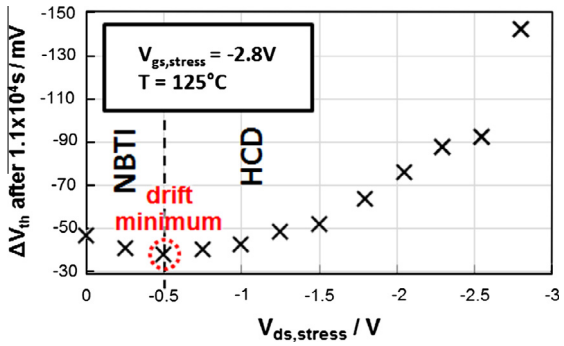
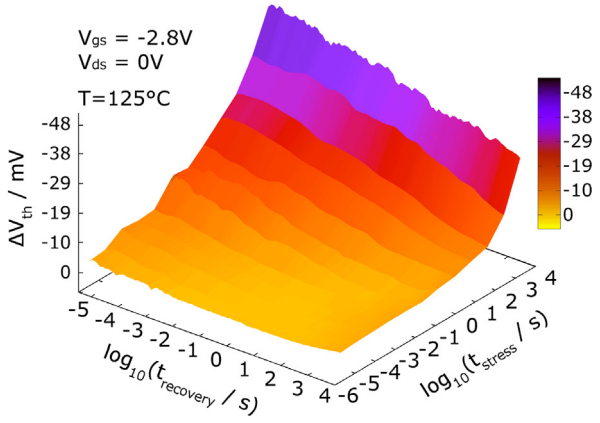
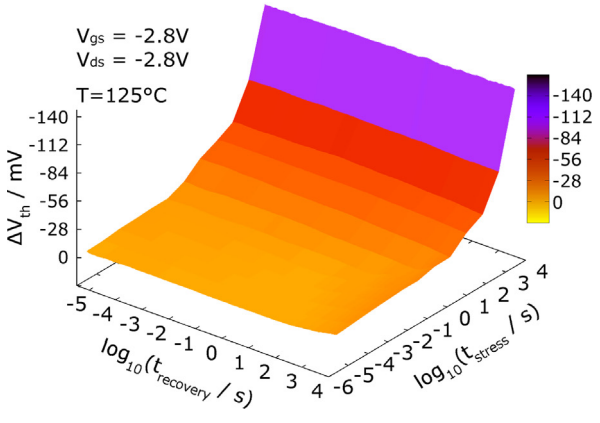


Fig. 4. Drift dependence for fixed $V_{gs} = -2.8$ V and varied $V_{ds} = (0, \ldots, -2.8)$ V. At $V_{gs} = -2.8$ V, $V_{ds} = -0.5$ V the interplay of NBTI and HCD leads to a drift minimum. The measurements were performed on adjacent chips to eliminate the global drift variation.



(a) homogeneous NBTI, $V_{gs} = -2.8$V, $V_{ds} = 0$V



(b) mixture of NBTI and HCD, $V_{gs} = V_{ds} = -2.8$V

Fig. 5. Three-dimensional plots of recovery traces for given stress times showing the strong influence of HCD on the drift and recovery behavior. For (a) homogeneous NBTI ($V_{ds} = 0$) the recovery of the threshold voltage drift is clearly recognizable whereas for (b) high drain stress voltages the recovery is almost negligible.

A further increase of the drain stress voltages leads to the mixture of NBTI and HCD. At this condition the amount of recoverable degradation diminishes with increasing stress time (Fig. 5(b)). For the last decades of stress time the recoverable component can be neglected. The details for the stress condition $V_{ds} = V_{gs}$ can be found in the corresponding CET map (Fig. 6(c)). Here the recoverable component is present for short stress times but vanishes for long stress times. In the case of pure HCD (Fig. 6(d)) the recoverable component is absent with respect to the very low change of the threshold voltage over time.

The device-to-device variation of the measured chips is below 5% regarding the drift for the same stress voltage condition.

4. Discussion

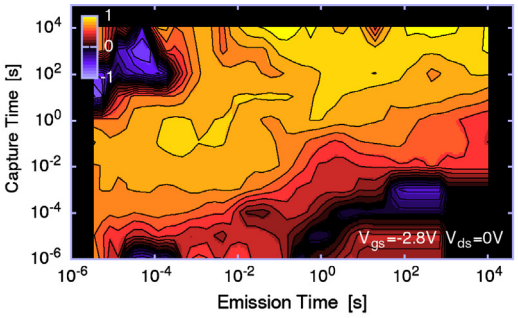
The observed recovery of the threshold voltage as well as the non-recoverable degradation component induced by HCD of the aged transistors are in good agreement with the literature [1,6,7]. As one compares the recovery traces shown in Fig. 5(a) and (b) with the corresponding CET maps (Fig. 6(a) and (c)) the recoverable component of the threshold voltage for the mixture of NBTI and HCD ($V_{gs} = V_{ds} = -2.8$ V) can nicely be observed in the CET map. For all stress decades above 1 s one has to consider the offset of the following recovery traces which is caused by non-discharged oxide traps and interface traps with recovery times above 10^4 s, contributing to a permanent degradation component [3].

By applying low drain voltages to the device under test the oxide field becomes inhomogeneous. The maximum electrical field ($E_{max} \approx V_{gs}/t_{ox}$) over the oxide can be found at the source side whereas the minimum ($E_{min} \approx (V_{gs} - V_{ds})/t_{ox}$) is located near the drain. Therefore the maximum NBTI-related degradation and recovery is expected at the source side.

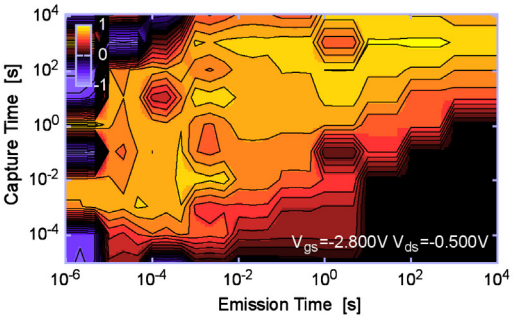
The drain voltage dependence of the threshold voltage drift shows a minimum for -0.5 V and is caused by the interplay of two degradation mechanisms. On the one hand the NBTI voltage condition causes holes to interact with the defects in the gate oxide and its interface [3]. On the other hand the HCD voltage condition enhances multiple particle mechanisms for the investigated short channel ($l = 100$ nm) device. Impact ionization [8], Auger recombination [9], electron–phonon [10,11] and electron–electron scattering [12,13] lead to an injection of holes into the gate oxide interface causing a positive oxide charge near the drain and resulting in a decrease in the transconductance [14]. The minimum of the threshold voltage degradation which is found for $V_{gs} = -2.8$ V, $V_{ds} = -0.5$ V is related to the energy distribution of the carriers in the channel which can cause either NBTI or HCD (Fig. 4). This effect has already been reported in the literature for older technologies and is with respect to the device length in good agreement with those results [15,16].

For high drain stress voltages HCD shows a huge impact on the permanent component of the threshold voltage shift and NBTI as well as its recovery become less severe. This can nicely be seen in the drift data after 1.1×10^4 s (Fig. 4), the recovery traces for each stress decade (Fig. 5(b)) and the CET map (Fig. 6(c)) for the case of mixed hot-carrier and NBTI degradation. In addition to that a shift of the recoverable component to about 100× shorter stress and 100× longer recovery times is observable if one compares the CET maps of homogeneous NBTI (Fig. 6(a)) with mixed NBTI and HCD (Fig. 6(c)).

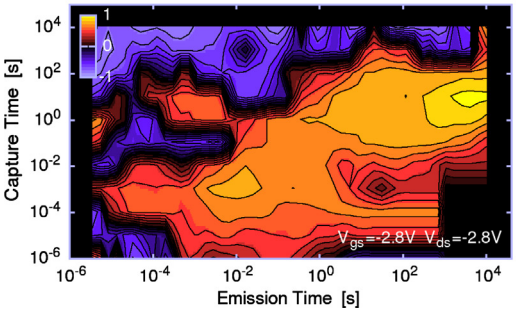
If one chooses a low gate voltage to suppress the NBTI degradation but applies a high drain voltage to emphasize pure hot-carrier induced degradation a recoverable component cannot be found in the CET map (Fig. 6(d)). The absence of a recoverable component underlines that for the investigated thin-oxide transistor (in



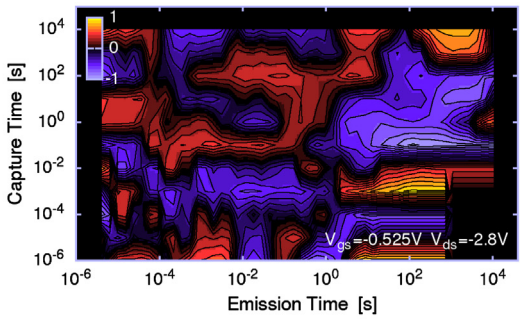
(a) homogeneous NBTI, $V_{gs} = -2.8V$, $V_{ds} = 0V$. The maximum threshold voltage shift of a single recovery trace compared to the other recovery traces was $\Delta V_{th,max} = 32mV$



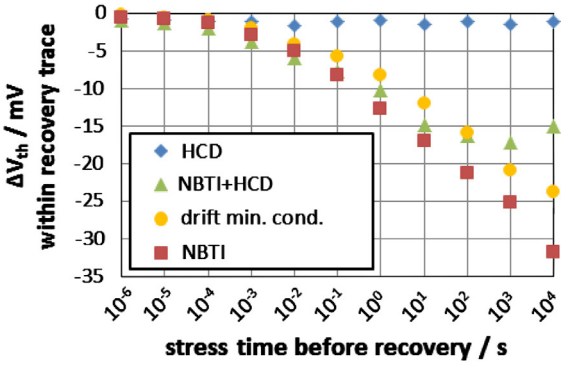
(b) inhomogeneous NBTI, $V_{gs} = -2.8V$, $V_{ds} = -0.5V$, at drift minimum condition (Fig. 4), $\Delta V_{th,max} = 24mV$



(c) mixture of NBTI and HCD, $V_{gs} = V_{ds} = -2.8V$, $\Delta V_{th,max} = 17mV$. Compared to homogeneous NBTI the recoverable component is shifted to shorter capture times and longer emission times



(d) pure HCD, $V_{gs} = -0.525V, V_{ds} = -2.8V$, $\Delta V_{th,max} = 2mV$ is very small compared to homogeneous NBTI and the mixture of NBTI and HCD



(e) Comparison of recovery signal after given stress time for HCD (blue), NBTI (red), their mixture (green) and the drift minimum condition (yellow, Fig. 4)

Fig. 6. (a–c) Continuous capture emission time maps for different stress conditions showing the influence of V_{ds} on the recoverable component and (d) the absence of a recoverable component for a pure HCD stress condition. (e) The change of the threshold voltage within a recovery trace after stress is strongly dependent on the drain voltage. For long stress times one has to consider that the device has not recovered completely.

contrast to a thick-oxide power device [17]) a recovery of the threshold voltage has only to be considered for NBTI degradation.

As the ultra-fast measurement technique allows the shortest delay between stressing the transistor and measuring the threshold voltage compared to other available commercial setups, the focus of the experiments is to acquire threshold voltage data. To provide a comparison between the threshold voltage and other important device parameters (e.g. $I_{ds,lin}, I_{ds,sat}$) additional data have been recorded (Fig. 7). These data show that for the investigated technology the threshold voltage shift is a perfect key parameter to allow a comparison among the different stress voltage regimes as it shows an apparent degradation not only for NBTI but also for a wide range of gate voltages under HCD stress conditions.

As recently discussed [18] the interaction between HCD and NBTI has to be determined to get a more realistic reliability assessment. Along these lines the additional information about the recovery behavior of a device obtained from CET maps can be used to simulate the aging of circuits more accurately in contrast to the usage of a superposition of compact models for NBTI and hot-carrier degradation. Following this approach it is ensured that the drift is neither over- nor underestimated by the simulation because all relevant voltage conditions are covered by the measurement data.

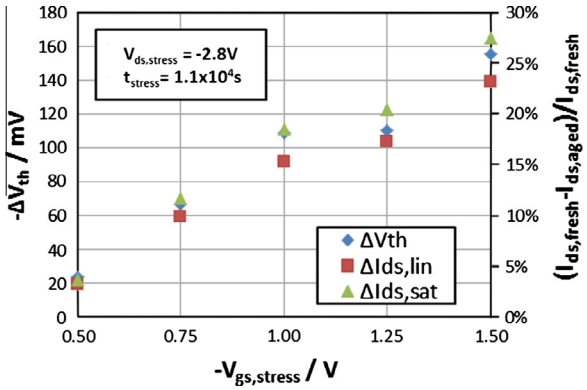


Fig. 7. Comparison of the drift of important device parameters after 1.1×10^4s hot-carrier degradation. All parameters (blue: ΔV_{th}, red: $\Delta I_{ds,lin}$, green: $\Delta I_{ds,sat}$) show an apparent drift over a wide gate voltage range thus showing their relevance for HCD. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

5. Conclusion

Two degradation mechanisms (NBTI, HCD) and their interplay were presented in form of threshold voltage drift results of a 2-dimensional parameter space of gate and drain stress voltage combinations for the investigated 130 nm technology. The homogeneous NBTI case shows the well-known recovery behavior. In contrast to that the recovery behavior of NBTI mixed with HCD for high drain voltages can best be shown and understood in the scope of CET maps which reveal the details of the threshold voltage recovery. In addition to that the interplay of NBTI and HCD leads to a minimum of the drift for high gate voltages combined with a low drain voltage.

Acknowledgments

This work has been supported by the German ministry of education and research (BMBF) within the project "Design for Reliability of SoCs for Applications like Transportation, Medical, and Industrial Automation" (RELY), 16M3091A, and the European research project "Modelling Reliability under Variability" (MoRV), 619234.

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