Microelectronic Engineering 109 (2013) 250–256

Contents lists available at SciVerse ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Superior reliability of high mobility (Si)Ge channel pMOSFETs

J. Franco [a,*], B. Kaczer [a], M. Toledano-Luque [a], Ph.J. Roussel [a], M. Cho [a], T. Kauerauf [a], J. Mitard [a], G. Eneman [a], L. Witters [a], T. Grasser [b], G. Groeseneken [c]

[a] imec, Kapeldreef 75, 3001 Leuven, Belgium
[b] Institute for Microelectronics, Technische Universität Wien, Gußhausstraße 27-29, 1040 Wien, Austria
[c] ESAT Dept., KU Leuven, 3001 Leuven, Belgium

ARTICLE INFO

Article history:
Available online 21 March 2013

Keywords:
pMOSFET
SiGe
Ge
NBTI
Reliability
Variability

ABSTRACT

With a significantly reduced Negative Bias Temperature Instability (NBTI), SiGe channel pMOSFETs promise to virtually eliminate this reliability issue for ultra-thin EOT devices. The intrinsically superior NBTI robustness of the MOS system consisting of a Ge-based channel and of a SiO_2/HfO_2 dielectric stack is understood in terms of a favorable energy decoupling between the SiGe channel and the gate dielectric defects. Thanks to this effect, a significantly reduced time-dependent variability of nanoscale devices is also observed. Other reliability mechanisms such as low-frequency noise, channel hot carriers, and time-dependent dielectric breakdown are shown not to be showstoppers.

1. Introduction

Due to the ever increasing electric fields in scaled CMOS devices, reliability is becoming a showstopper for further scaled technology nodes. Although several groups have already demonstrated functional devices with aggressively scaled EOT down to ~5 Å [1,2], the stability of their parameters at operating conditions cannot be guaranteed [3,4]. Meanwhile, the use of high-mobility channels is being considered for further device performance enhancement in future CMOS technology nodes [5,6]. The SiGe channel quantum well technology (Fig. 1) in particular is considered for yielding enhanced mobility and pMOS threshold voltage tuning [7].

While the interface passivation of non-Si channel materials is typically considered a challenging and critical issue, extremely promising device performance was recently obtained by growing epitaxially a thin Si passivation layer on top of a pMOS (Si)Ge channel [8]. However, open questions exist about the reliability of such complex gate stacks.

In this paper we review our recent studies regarding the reliability of Ge-based pMOSFETs. We show that this technology offers a significant intrinsic reliability improvement which we ascribe chiefly to a reduced interaction between channel carriers and oxide defects. Furthermore, we show that the (Si)Ge-based technology also considerably alleviates the time-dependent variability [9], which arises as devices scale toward atomistic dimensions [10]. The extensive experimental results summarized here strongly support (Si)Ge pMOS technology as a clear frontrunner for future CMOS technology nodes.

2. Negative bias temperature instability

Negative Bias Temperature Instability (NBTI) is considered as the most severe reliability issue for scaled CMOS technologies [11,12]. It affects pMOSFETs during operation, causing significant shifts of the device electrical parameters (e.g., threshold voltage shift ΔV_{th}) due to oxide defect charging and interface state creation. The quasi-constant supply voltage scaling proposed by the international technology road map [13] for the recent and upcoming technology nodes enhances NBTI due to the ever increasing oxide electric field (E_{ox}) [14]. As a consequence, a 10 year lifetime at operating conditions cannot be guaranteed anymore for Si channel pMOSFETs with ultra-thin (UT-) EOT (Fig. 2 diamonds).

Already in 2009 [15], we reported that the Ge-based technology promises a significantly improved NBTI robustness. To benefit from this property, the SiGe gate-stack was optimized for enhanced reliability, including a high Ge fraction (55%) in the channel, a sufficiently thick quantum well (6.5 nm) and a Si passivation layer of reduced thickness (0.8 nm) [16,17]. By means of such optimization, we demonstrated sufficiently reliable ultra-thin EOT SiGe pMOSFETs with a 10 year lifetime at operating conditions in both gate-first and gate-last process flows (Fig. 2) [18]. The main gate-stack parameter affecting the NBTI robustness was found to be the Si passivation layer thickness, with thinner Si caps consistently observed to yield a significant boost of the device reliability while

* Corresponding author.
E-mail address: Jacopo.Franco@imec.be (J. Franco).

0167-9317/$ - see front matter © 2013 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.mee.2013.03.001

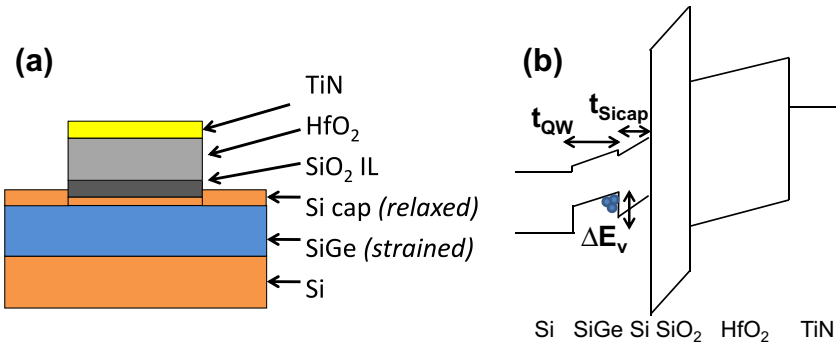

Fig. 1. (a) Sketch of the gate-stack of SiGe devices used in this work. (b) Band diagram in inversion. Channel holes are confined into the SiGe quantum well due to the valence band offset (ΔE_v) between the SiGe channel and the Si cap. The Si cap thickness (t_{Sicap}) therefore contributes to the capacitance equivalent thickness in inversion (T_{inv}) of the gate stack.

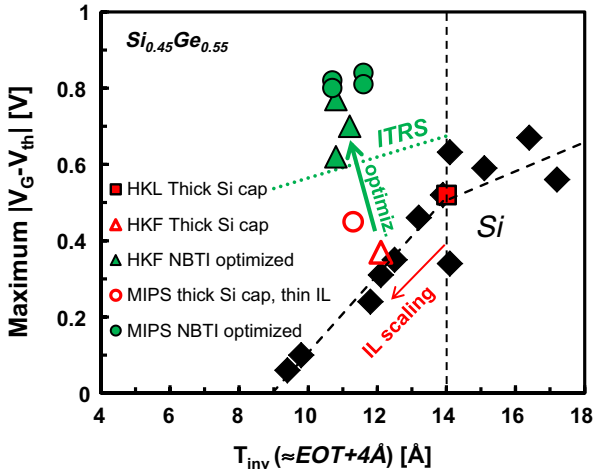

Fig. 2. A high Ge fraction (55%) in a 6.5 nm thick quantum well, combined with a thin Si cap (0.8 nm) boost the maximum operating overdrive ($|V_G - V_{th0}|$) to meet the target V_{DD} at ultra-thin EOT in a MIPS flow (solid circles, as compared to open circle). The optimization was also implemented in a RMG flow: high-k last SiGe sample with thick Si cap (solid square) shows poor NBTI robustness; an IL reduction by means of O-scavenging in a high-k first process flow (open triangle), further increases NBTI; however, the SiGe gate-stack optimization (solid triangles) boosts the maximum operating overdrive above the ITRS target. The results were reproduced for several process thermal budgets.

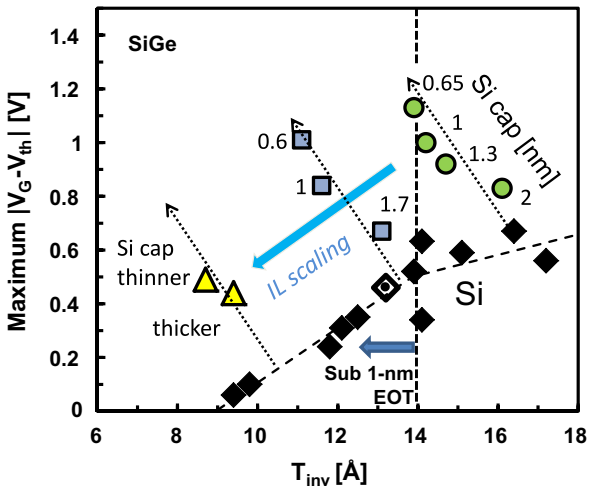

Fig. 3. Maximum operating overdrive for 10 year lifetime ($T = 125$ °C, failure criterion $\Delta V_{th} = 30$ mV) vs. T_{inv}. SiGe devices with a thin Si cap offer improved NBTI reliability, i.e. higher maximum operating overdrive.

reducing the capacitance equivalent thickness in inversion (T_{inv}) of the gate stack (Fig. 3). Furthermore, the reliability improvement was observed to be readily transferable to different device structures such as pure Ge channel pMOSFETs and wrapped SiGe channel pfinFETs [19]. These process- and architecture-independent results suggest the superior reliability to be an intrinsic property of the MOS system consisting of a Ge-based channel and a SiO_2/HfO_2 dielectric stack. It is therefore eminently relevant to understand in detail the physical mechanisms behind this property.

By comparing with Si reference devices with an identical high-k/metal gate stack, we have reported several experimental observations about the NBTI degradation kinetic in optimized SiGe channel devices [19], which can be summarized as:

(1) Similar time dependence (i.e., the same power-law exponent) of the overall threshold voltage shift (ΔV_{th});
(2) Similar apparent temperature activation [12] of the overall ΔV_{th} ($E_A \approx 60$ mV);
(3) Reduced interface state generation (ΔN_{it}, the so-called *permanent* component of NBTI [20]) and significantly reduced hole trapping in pre-existing bulk oxide

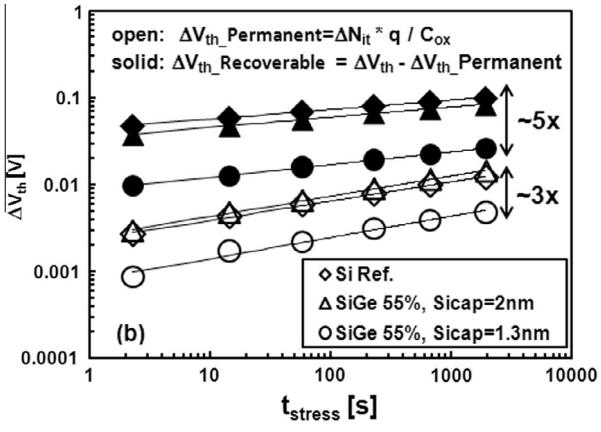

Fig. 4. Total ΔV_{th} split into the so-called permanent (P) ΔV_{th}, assumed to be caused by ΔN_{it}, and the recoverable (R) ΔV_{th}, assumed to be caused by filling of pre-existing oxide traps (N_{ot}). ΔN_{it} measured with charge pumping during NBTI stress were converted to $\Delta V_{th\_Permanent}$ ($=\Delta N_{it}.q/C_{ox}$) in order to decouple their contribution from the total measured ΔV_{th}. Three samples are compared (Si Reference, SiGe with thick and thin Si caps): ΔN_{it} follows a power law on the stress time with the same exponent (~0.25) on all the samples. However SiGe devices with thinner Si cap show both reduced P and R, with the reduction of R having a higher impact on the total ΔV_{th}.

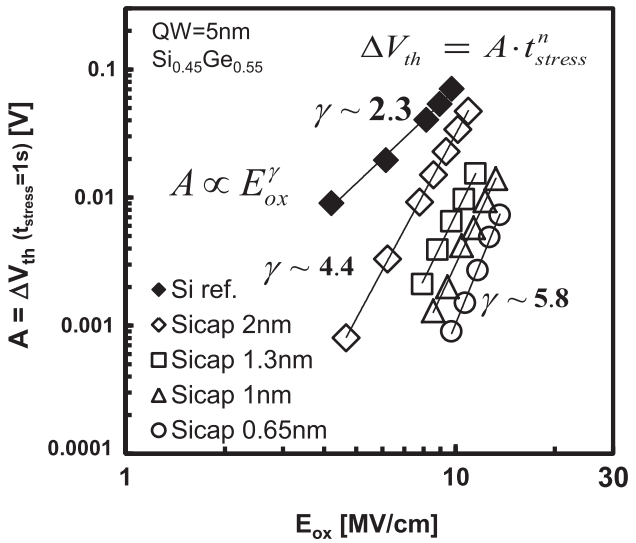

Fig. 5. Extracted NBTI ΔV_{th} power-law pre-factors (i.e. ΔV_{th} after a stress period of 1 s): a significant reduction for the SiGe devices is observed, especially with a reduced Si cap thickness. A stronger field-acceleration for SiGe with respect to the Si Ref. device is also noted, leading to further improvement at lower operating fields.

defects($\Delta N_{ot,}$ the so-called *recoverable* component of NBTI [20]), with the latter reduction being of greater relevance (Fig. 4);

(4) Similar time dependence (power-law exponent ~0.25, see Fig. 4) and field dependence of the NBTI-induced interface state generation (ΔN_{it});

(5) Stronger field-dependence of the overall ΔV_{th} (Fig. 5) caused by a stronger field dependence of the dominant trapping component (ΔN_{ot}).

The observations related to the generation of interface states suggest that the same bond breaking process at the Si/SiO_2 interface, i.e. the de-passivation of H-passivated Si dangling bonds (P_{b0}), is likely to be taking place also in (Si)Ge channel devices. We have previously reported [17] Electron Spin Resonance Spectroscopy (ESR) [21] measurements on a Ge substrate with a thick Si cap which revealed a high P_{b0} density (~1×10^{12} cm^{-2}), while these defects could not be detected (<10^{11} cm^{-2}) on a very thin Si cap. This observation suggests that the Ge segregation at the Si/SiO_2 reported for Ge-based channels and enhanced by the use of a Si cap with reduced Si cap thickness [22] can reduce the N_{it} precursor defect density and therefore the ΔN_{it} during NBTI stress.

However, while this reduced creation of interface states cartainly plays a role in the improved NBTI reliability observed for SiGe channel devices, it cannot completely explain the strongly reduced overall NBTI degradation which is mainly caused by a significant reduction of the hole trapping component (ΔN_{ot}, see Fig. 4). We propose that the ΔN_{ot} reduction is related to a favorable alignment shift of the Fermi level in the SiGe channel with respect to the pre-existing bulk oxide defect energy levels (Fig. 6) [19]. Larger misalignment can cause carriers to interact with a smaller fraction of accessible oxide traps. To model this effect, we assume the existence of defect bands both in the SiO_2 IL and in the high-k layer. We note that the interacting defects have to be located in both dielectric layers since the same NBTI trends on SiGe with different Si caps were consistently observed when scaling the IL thickness (cf. Fig. 3). As depicted in Fig. 6, the Fermi level in the channel determines which part of the defect band is accessible to channel holes. Thanks to the band alignment of the (Si)Ge channel toward the gate stack, fewer defects are energetically favorable for channel holes. However, the additional voltage drop over a thicker Si cap (when benchmarking at fixed gate overdrive voltage or at fixed equivalent oxide electric field, as customary for NBTI studies), '*pushes*' down the channel holes energy level and therefore more defects become energetically favorable for charging (Fig. 6b). We implemented this model concept by representing the defect bands as Gaussian distributions over energy in order to calculate the induced ΔV_{th} caused by accessible defects for different gate stacks and as a function of the applied gate overdrive voltage. The mean values of the distributions were pinned at 0.95 eV below the Si valence band for the IL (corresponding to the $E'_{\gamma}[E_{0/+}]$ center in SiO_2 [23]) and at 1.4 eV below the Si valence band for the high-k (corresponding to the neutral oxygen vacancy [O_o] level in HfO_2 [24]). All the defects located above the channel Fermi level are considered occupied by trapped holes, while all the defects below are neutral (note: no trapping/de-trapping kinetics is included in this calculation, i.e. the thermodynamic equilibrium is represented). The model was first calibrated using the NBTI data on the Si reference devices: the standard deviations of the Gaussian distributions were used as a fitting parameter (in the range of 0.3–0.5 eV) in order to capture the correct electric field dependence, while the defect densities were fitted in order to match the observed ΔV_{th} magnitude. The scaled ΔV_{th} contribution of defects located at varying depths due to their electrostatic effect was also included. Then, with the same defect band parameters, the expected ΔV_{th} was calculated for SiGe channel devices, including the valence band offset of

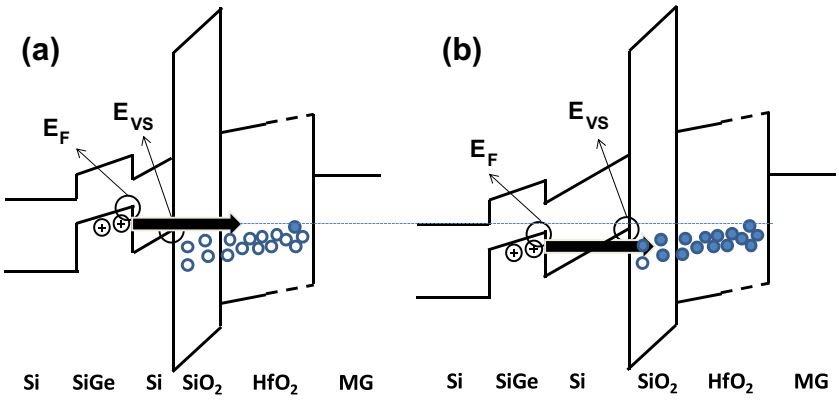

Fig. 6. A model including defect bands in the IL and in the HfO_2. (a) Fewer defects are energetically favorable for trapping channel holes thanks to the higher Fermi level in SiGe as compared to Si. (b) The additional voltage drop on a thicker Si cap 'pushes' down the Fermi level in the channel (when benchmarking at constant electric field or constant gate overdrive) and therefore more oxide defects become energetically favorable for hole trapping.

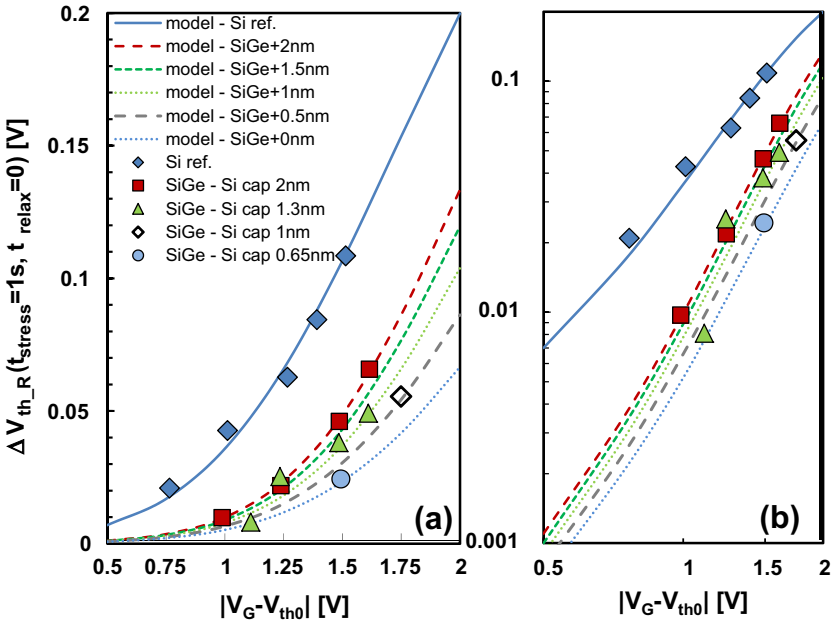

Fig. 7. Calculated ΔV_{th} vs. experimental data of the recoverable component. The model was first calibrated on the Si reference data, then the same defect band parameters were used to calculate the expected ΔV_{th} for SiGe devices (including the valence band offset between the SiGe and the Si cap, and the voltage drop on Si caps of varying thickness). The simple model matches the experimental data remarkably well. (a) Lin–lin, (b) log–log scales.

+0.35 eV in the channel and including the varying voltage drop on Si cap with varying thicknesses.

As shown in Fig. 7 the simple model matches excellently the experimental recoverable component (ΔN_{ot}) of NBTI. Both the reduced degradation and the stronger field dependence observed for SiGe devices with reduced Si cap thicknesses are readily captured.

The model explains also the other experimental observations previously made concerning the Ge fraction and the quantum well thickness. In order to minimize the fraction of accessible defects, i.e. in order to 'push up' the Fermi level in the channel with respect to the defect band, the valence band offset between SiGe and Si has to be maximized—higher Ge fraction (reduced bandgap and higher ΔE_v) and thick quantum well (to reduce quantization) are therefore beneficial. Moreover, this model explains the distinct relation between the fresh device V_{th0} and the NBTI observed in SiGe devices with varying process parameters (Fig. 8a): as calculated with MEDICI for, e.g., a Si cap thickness split, gate-stacks with lower

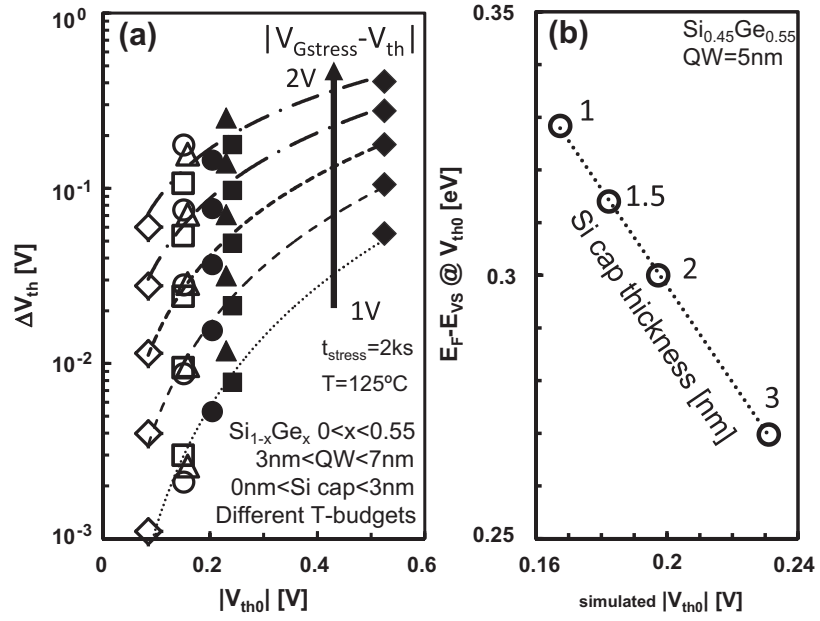

Fig. 8. (a) A clear correlation between the initial V_{th0} and NBTI-induced ΔV_{th} is consistently observed on SiGe devices with different gate-stacks: devices with lower initial V_{th0} always showed reduced V_{th}-instability, at any given stress condition ($|V_{Gstress}-V_{th0}|$). This was not observed for Si devices. (b) A lower device V_{th0} corresponds to a higher channel Fermi level energy (E_F) with respect to the Si valence band (E_{VS}), as shown with MEDICI simulations. The higher Fermi level in the channel is beneficial for reducing the carrier-trap interaction, according to the model proposed here (cf. Fig. 7).

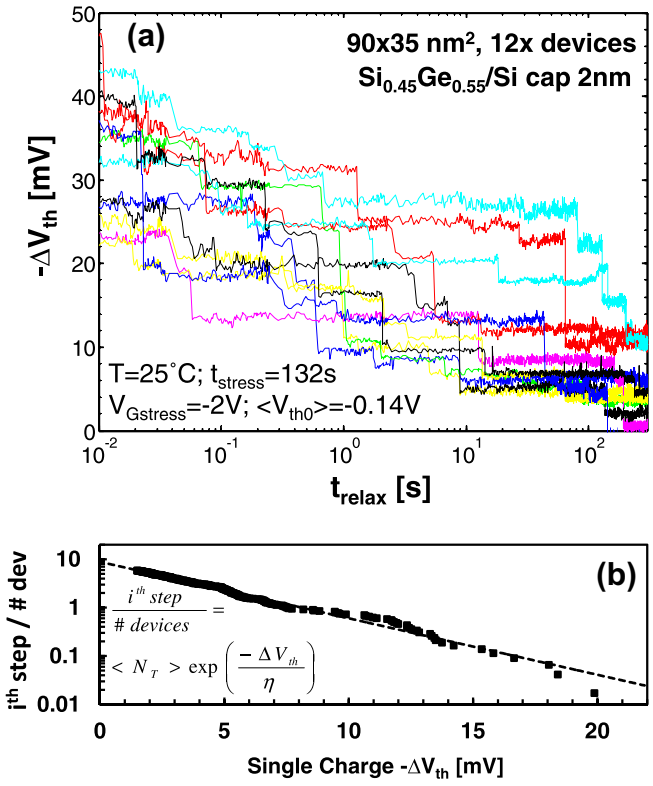

Fig. 9. (a) NBTI relaxation transients recorded on nanoscaled SiGe devices. For each device, multiple single defect discharge events are visible. (b) Weighted complementary Cumulative Distribution Function (CCDF) plot of the individual ΔV_{th} step heights observed on multiple (41) devices. Despite the intentionally undoped epitaxially grown SiGe channel, the ΔV_{th} step heights appear to be exponentially distributed [25], with an average value $\eta \approx 3.9$ mV. The average number of defects per device, $\langle N_T \rangle$, can be easily read in this plot as the intersection of the distribution with the y-axis [29].

$|V_{th0}|$ have higher channel Fermi level energy (Fig. 8b) and therefore benefit from reduced interaction between holes and oxide defects.

Finally we note that the proposed representation of the defect levels as Gaussian distributions is a mere assumption serving the sole purpose of simplifying the mathematical treatment of the model. Different energy distributions of the defects in the dielectric layer might exist in reality. Nevertheless, a similar beneficial effect by shifting up the Fermi level energy in the channel will be obtained independently of the chosen defect level representation [e.g. even for a uniform energy distribution of defect levels, a fraction of defects would become unfavorable for holes at the (Si)Ge channel Fermi level]. Furthermore, we also note that an additional contribution to the enhanced NBTI for gate stack with thicker Si caps could be related to a spill-over of inversion holes into the cap at high oxide fields: according to the proposed model, holes at the valence band of the Si cap would be favorably trapped in the dielectric defects and therefore the benefit of using a Ge-based channel would be partially lost.

3. Time-dependent variability

With the ever decreasing device size, the number of dopant atoms, but also the number of defects, in each device reduces to numerable levels [10]. This results in increased time-zero (i.e., as-fabricated) variability, but also considerable time-dependent variability (i.e., reduced reliability) [9,25]. We and others have recently shown that the properties of individual charged gate oxide defects can be observed in the NBTI ΔV_{th} relaxation transients [9,12,26]. A representative set of typical NBTI relaxation transients recorded on nanoscale SiGe devices is shown in Fig. 9a. Several observations can be made:

(1) The total ΔV_{th} observed after the same NBTI stress strongly varies from device to device;
(2) Single discharge events are visible, each causing a different ΔV_{th} step;
(3) Each device shows a different number of charging/discharging events (i.e. a different number of active oxide traps, N_T);
(4) The ΔV_{th} step heights appear to be approximately exponentially distributed (Fig. 9b), with average value η (i.e. the slope of the exponential distribution) but with some single charged oxide defects easily causing gigantic ΔV_{th} [25].

Such anomalous large ΔV_{th} are commonly ascribed to the percolative nature of the current in nanoscale devices associated with channel potential non uniformity induced by variability sources (e.g. random dopant distribution, line edge roughness, metal gate granularity, etc.) [10].

SiGe pFETs with a reduced Si cap thickness showed a ~10× reduced average number of charge/discharge events per device, i.e. a reduced average number of active defects $\langle N_T \rangle$ (Fig. 10a) and a ~2× reduced average ΔV_{th} step height η (Fig. 10b) with respect to their Si counterparts [27]. These two experimental observations are readily explained with the model already discussed in the previous section (cf. Fig. 6): fewer oxide defects are energetically favorable for SiGe channel holes, with the accessible defects located on the gate side of the dielectric, resulting in a reduced electrostatic impact on the channel [28].

Thanks to the reduced $\langle N_T \rangle$ and η, the optimized SiGe channel technology promises a significantly enhanced reliability when considering a realistic population of billions of nanoscaled devices, as illustrated in Fig. 11 [29].

4. Other reliability mechanisms

Low-frequency noise

Similarly to BTI, $1/f$ noise is ascribed to trapping and de-trapping of channel carrier into oxide defects with widely distributed characteristic time constants. The reduced interaction between carriers and oxide defects observed for SiGe devices – owing to the energy decoupling (cf. Fig. 6) – also yields a reduced $1/f$ noise, as we showed in [27].

Channel hot carrier reliability

The use of a small bandgap semiconductor favors electron–hole pair generation in the channel by means of impact ionization. This effect is expected to enhance hot carrier degradation. Indeed, poor hot carrier robustness has been reported for pure Ge-channel devices [30,31]. However, during a typical CHC stress ($V_G = V_D = V_{stress}$) a significant fraction of the total degradation in pMOS devices is related to the residual NBTI effect at the source side of the channel [32]. The enhanced NBTI robustness of the optimized SiGe devices significantly reduces also the total degradation caused by CHC stress (Fig. 12a). As we reported in [17], CHC do not constitute a showstopper for the optimized SiGe devices reliability (Fig. 12b).

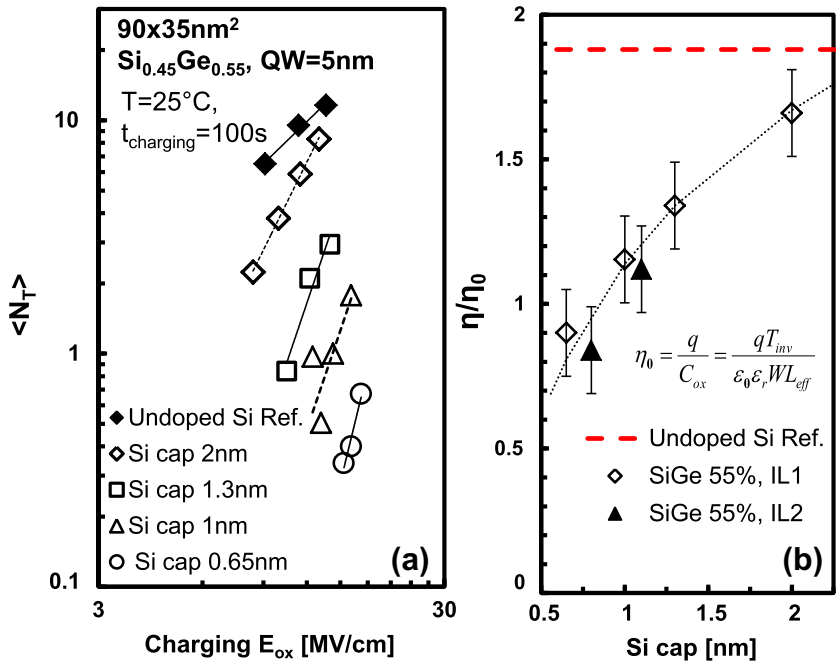

Fig. 10. (a) Consistently with large area device data (cf. Fig. 5), nanoscaled SiGe channel pMOSFETs with a reduced Si cap thickness show reduced average number of charging/discharging defects per device $\langle N_T \rangle$, and a stronger field acceleration. Note: very high equivalent oxide fields were needed for the charging phase in order to be able to observe active defects in SiGe devices with the thinnest Si cap ($\langle N_T \rangle$ as low as ~0.33 at 15 MV/cm, i.e. one defect observed for every three measured devices). (b) Extracted average ΔV_{th} step heights η for SiGe devices with different Si cap and for undoped Si channel devices, after a charging phase at $E_{ox} \approx 12$ MV/cm. The extracted values of η are normalized for the charge sheet approximation (η_0) for the electrostatic of a single charge. SiGe devices with the thinnest Si cap show a significantly lower η (~2×). The observation is confirmed on SiGe devices with two different SiO_2 interfacial layer thicknesses. The red dashed line demarcates the benchmark value experimentally estimated on undoped Si channel Ref. devices. The error bars on the estimated η values are related to the lower $\langle N_T \rangle$ observed for SiGe.

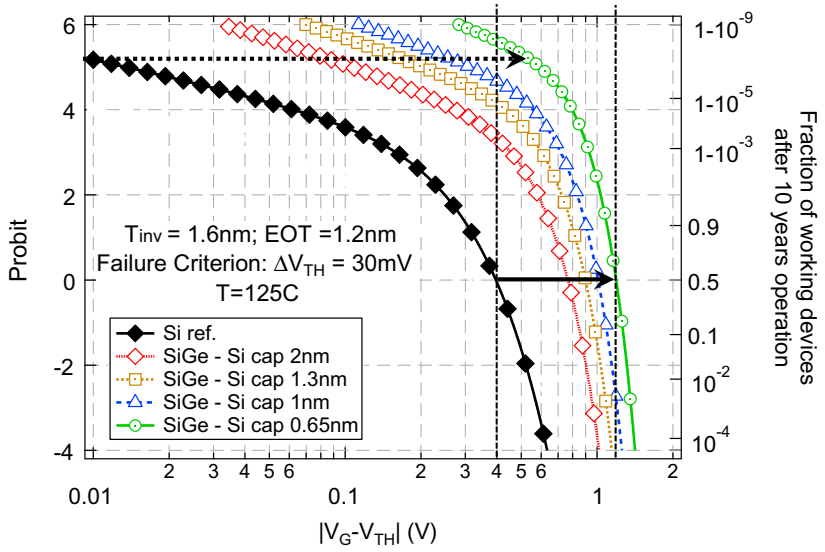

Fig. 11. Calculated fractions of working devices after 10 year continuous operation at varying operating voltages [29] for the different gate stacks studied here. A dramatic improvement of the distributions is apparent for SiGe devices with reduced Si cap thickness. Note: large area device lifetime would appear in this plot as a vertical dashed line (whole population fails above maximum allowed operating voltage, while it passes for lower voltages) with same median value (Probit = 0) of the respective nanoscaled device distribution. The reliability improvement previously observed in large area SiGe devices (demarcated by the solid arrow at Probit = 0) is expected to be magnified at high percentiles (demarcated by the dotted arrow, at ~1 ppb).

Time dependent dielectric breakdown

As already noted for Ge devices in [33], no significant difference in the TDDB characteristic of SiGe with respect to their Si counterparts having the same SiO_2/HfO_2 dielectric stack was observed. Although a few non-destructive (i.e. *soft*) breakdown events could be expected [17], TDDB is not considered the showstopper for UT-EOT devices [34].

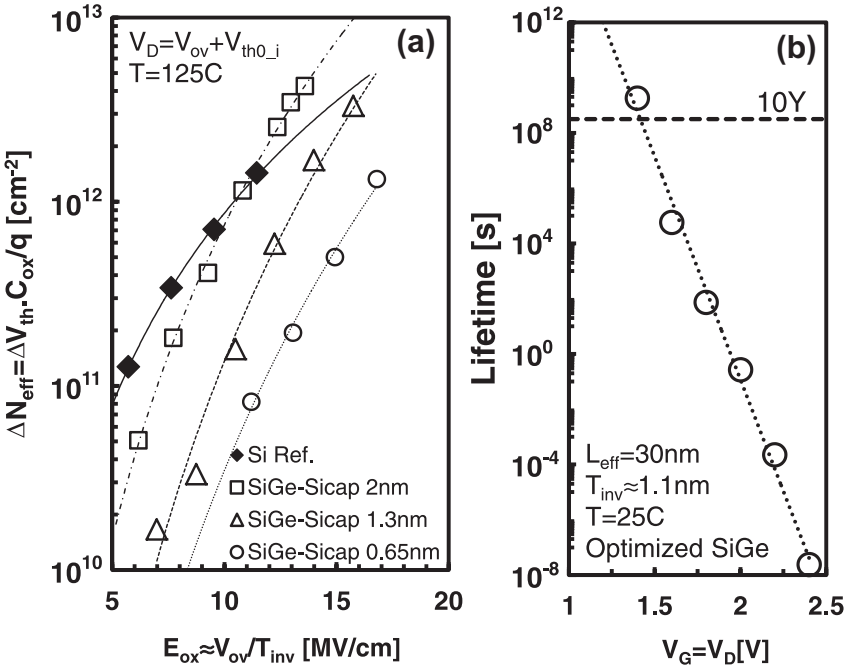

Fig. 12. (a) SiGe devices with a thick Si cap show lower CHC degradation with respect to Si Ref. devices only at low stress conditions, while at high stress conditions a higher degradation is apparent likely due to enhanced impact ionization in the small bandgap channel [30]. However, the optimized SiGe gate-stacks with a reduced Si cap thickness consistently show an overall reduced CHC degradation over Si Ref. devices. (b) Extrapolated device lifetime under CHC stress for a ~0.7 nm EOT ($T_{inv} \approx 1.1$ nm) NBTI-optimized SiGe gate stack. CHC do not constitute a showstopper for SiGe devices.

5. Conclusions

The NBTI reliability of Ge-based channel pMOSFETs was investigated. The results clearly show significantly improved NBTI reliability for this family of high-mobility channel devices. A reliability-aware gate-stack optimization, with a high Ge fraction, a sufficiently thick quantum well and reduced Si cap thickness was developed to demonstrate ultra-thin EOT SiGe devices with 10 year NBTI reliability at operating V_{DD}. The NBTI reduction was ascribed mainly to a favorable alignment shift of the Fermi level in the SiGe channel with respect to pre-existing defect energy levels in the dielectric layers.

Owing to this beneficial effect, a reduced time-dependent variability of nanoscaled SiGe pFETs is also expected. In particular, we reported a significant reduction of the average number of active oxide defects $\langle N_T \rangle$ causing charge/discharge events, and of the average impact on the device characteristic per each trapped charge (η). Furthermore, a reduced low-frequency noise was also observed in SiGe devices.

Other reliability mechanisms, such as channel hot carriers and time-dependent dielectric breakdown were shown not to be showstoppers. The extensive experimental results here summarized strongly support SiGe technology as leading candidate for future CMOS technology nodes, offering a complete solution to the reliability issue for ultra-thin EOT nanoscaled pMOSFET devices.

Acknowledgments

This work was performed as part of imec's Core Partner Program. It has been in part supported by the European Commission under the 7th Framework Programme (Collaborative project MORDRED, Contract No. 261868). Discussions with Prof. M. Heyns (imec and KU Leuven) are gratefully acknowledged. Prof. V. Afanas'ev and Prof. A. Stesmans (Physics and Astronomy Dept., KU Leuven) are gratefully acknowledged for providing the Electron Spin Resonance spectroscopy data discussed in this paper and for relevant discussion.

References

[1] L.-Å. Ragnarsson et al., Proc. Int. Electron Dec. Meet. (2009) 663–666.
[2] T. Ando et al., Proc. Int. Electron Dec. Meet. (2009) 423–426.
[3] E. Cartier et al., Proc. Int. Electron Dev. Meet. (2011) 18.4.1–18.4.4.
[4] M. Cho et al., IEEE Trans. Electron Dev. 59 (8) (2012) 2042–2048.
[5] L. Witters et al., Proc. Symp. VLSI Technol. (2010) 181–182.
[6] J. Mitard et al., Proc. Int. Electron Dec. Meet. (2010) 249–252.
[7] S. Krishnan et al., Proc. Int. Electron Dev. Meet. (2011) 28.1.1–28.1.4.
[8] J. Mitard et al., Proc. European Solid-State Device Research Conference (ESSDERC) (2009) 411–414.
[9] V. Huard et al., Proc. Int. Rel. Phys. Symp. (2008) 289–300.
[10] A. Asenov, R. Balasubramaniam, A.R. Brown, J.H. Davies, *IEEE* Trans. Electron Dev. 50 (3) (2003) 839–845.
[11] V. Huard et al., Micr. Rel. 46 (1) (2006) 1–23.
[12] T. Grasser et al., IEEE Trans. Electron Dev. 58 (11) (2011) 3652–3666.
[13] International Technology Roadmap for Semiconductors. Available from: <http://public.itrs.net>.
[14] G. Groeseneken, R. Degraeve, B. Kaczer, K. Martens, Proc. European Solid-State Device Research Conference (ESSDERC) (2010) 64–72.
[15] B. Kaczer et al., Micr. Eng. 86 (7–9) (2009) 1582–1584.
[16] J. Franco et al., Proc. Int. Rel. Phys. Symp. (2010) 1082–1085.
[17] J. Franco et al., Proc. Int. Electron Dec. Meet. (2010) 70–73.
[18] J. Franco et al., Proc. Int. Electron Dec. Meet. (2011) 445–448.
[19] J. Franco et al., IEEE Trans. Electron Dev. 60 (1) (2013) 396–404.
[20] T. Grasser et al., Proc. IEEE Int. Rel. Phys. Symp. (2011) 605–613.
[21] A. Stesmans, V. Afanas'ev, Characterization of Semiconductor Heterostructures and Nanostructures, Elsevier, 2008. pp. 435–489.
[22] M. Caymax et al., J. Electrochem. Soc. 156 (12) (2009) H979–H985.
[23] W. Gös, Dissertation, T.U. Wien. Available from: <http://www.iue.tuwien.ac.at/phd/goes/dissse19.html>.
[24] A.S. Foster, F. Lopez Gejo, A.L. Shluger, R.M. Nieminen, Phys. Rev. B (65) (2002).
[25] B. Kaczer et al., Proc. Int. Rel. Phys. Symp. (2010) 26–32.
[26] M. Toledano-Luque et al., Proc. Int. Rel. Phys. Symp. (2011) 364–371.
[27] J. Franco et al., IEEE Trans. Electron Dev. 60 (1) (2013) 405–412.
[28] J. Franco et al., Micr. Eng. 88 (7) (2011) 1388–1391.
[29] M. Toledano-Luque et al., Proc. VLSI Symp. (2011) 152–153.
[30] D. Maji et al., IEEE Trans. Electron Dev. 56 (5) (2009).
[31] J. Franco et al., J. Vac. Sci. Technol. B 29 (1) (2011) 804.1–804.4.
[32] J. Franco et al., Proc. Int. Rel. Phys. Symp. (2011) 624–629.
[33] B. Kaczer et al., Micr. Eng. 84 (9–10) (2007) 2067–2070.
[34] T. Kauerauf et al., Proc. Int. Rel. Phys. Symp. (2011) 7–16.