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Bias-temperature instability in single-layer graphene field-effect transistors

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We present a detailed analysis of the bias-temperature instability (BTI) of single-layer graphene field-effect transistors. Both negative BTI and positive BTI can be benchmarked using models developed for Si technologies. In particular, recovery follows the universal relaxation trend and can be described using the established capture/emission time map approach. We thereby propose a general methodology for assessing the reliability of graphene/dielectric interfaces, which are essential building blocks of graphene devices. © *2014 AIP Publishing LLC*.
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Graphene has attracted a considerable amount of attention due to its unique physical and electrical properties, such as an extremely high room-temperature carrier mobility[1,2] and high saturation velocity.[3] Moreover, graphene is remarkably compatible with standard complimentary metal oxide semiconductor (CMOS) technology,[4] and is therefore considered as a promising material for advanced electronic devices, which could enhance the performance or functionality of silicon (Si) integrated circuits. Since the discovery of graphene in 2004, many attempts at fabricating graphene field effect transistors (GFETs)[5–10] and related electronic devices[11,12] have been undertaken. Beyond such demonstrations of device functionality for potential applications, process integration issues such as low resistance electrical contacts[13] and reliable dielectric interfaces with graphene are urgent research topics to assess the true potential of graphene technology. In particular, a rigorous method for the quantification of dielectric quality and reliability in terms of the charged trap density is needed. Few attempts have been made at trying to describe the dielectric reliability in terms of bias-temperature instability (BTI),[14–17] one of the key figures of merit for reliability in conventional Si metal oxide semiconductor field effect transistors (MOSFETs).[18,19] However, none of these works reports a systematic method to benchmark BTI dynamics in GFETs based on models known from Si technologies.

Here, we perform a detailed study of BTI on the aluminum oxide (Al_2O_3) high-k top gate of double-gated GFETs. We demonstrate that BTI can be understood using standard methods previously developed for Si technologies if the degradation dynamics are expressed in terms of a Dirac point voltage shift rather than an ill-defined threshold voltage shift. While the measured defect densities are still noticeably larger than those known from Si technologies, the dynamics of BTI are in general found to be comparable, allowing for quantitative benchmarking of the graphene/dielectric interface quality.

In our devices, the graphene channel is sandwiched between Al_2O_3 as a top gate insulator and SiO_2 as a back gate insulator. Typical channel lengths were between 1 and 4 μm, with widths ranging from 4 to 80 μm. The devices were fabricated on a thermally oxidized Si substrate using a standard contact lithography process;[4] the top gates and source/drain contacts were made of TiAu and the back gates of Al. In our first measurements, a significant device-to-device variability could be observed which prevented a systematic reliability study. However, in the spirit of the standard forming-gas anneal of Si technology,[16] by baking the devices at $T = 300\,^{\circ}C$ in a H_2/He mixture, a significant decrease in variability has been obtained (Fig. 1(a)). As such, this thermal treatment before electrical characterization appears to be essential for reliability studies, which require the comparison of degradation data taken on various devices.

The electrical characteristics have been measured in vacuum (10^{-6} Torr) in order to avoid the detrimental impact of the environment.[17,20] Initially, GFET transfer and output characteristics were investigated, which look similar to those published previously[14] (Figs. 1(b) and 1(c)). In particular, we observe a modulation of the Dirac point voltage V_{Dirac} by the back gate bias V_{BG}, as well as a hysteresis related to charging/discharging of fast oxide traps.[14] The output characteristics measured at different top gate biases V_{TG} show a rather strong saturation at high V_d in some devices. Also, some kinks related to ambipolar channel effects are visible at negative V_{TG}.[21]

The impact of BTI stress on the top gate transfer characteristics was examined as follows: first, the transfer characteristic of the fresh device was measured. After this a constant V_{TG} was applied for a certain time, taking care to avoid additional degradation factors (e.g., hot carrier degradation) by setting V_{BG} and V_d to zero during the top gate BTI stress. Also, for the same reason it was necessary to use narrow top gate voltage sweep intervals in the measurements, in our case ($\pm$1–2 V around V_{Dirac}). Then the evolution of the transfer characteristics during recovery was monitored for several hours/days. Since the observed drifts were very large, the experiments were repeated on the same device using increasing stress times ($t_s = 1$, 10, 100, and 1000 s) with re-adjusted

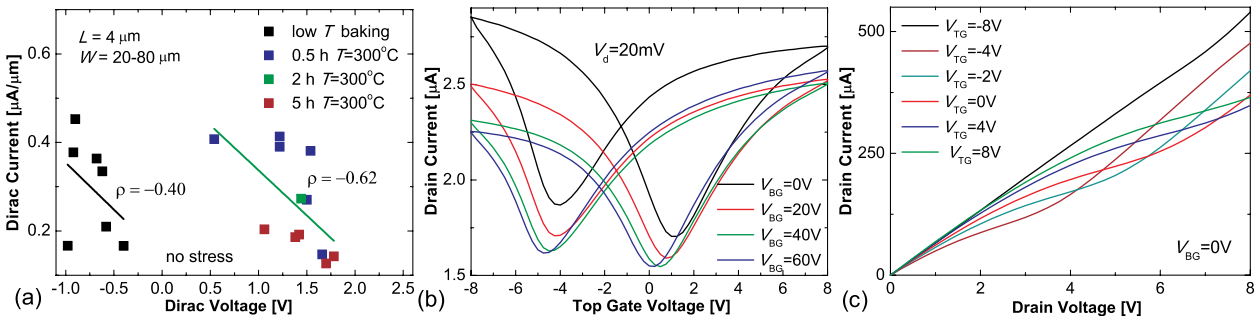

FIG. 1. (a) Device-to-device variability is determined by the distribution of the current normalized to the channel width W and voltage values at the Dirac point. After baking, the variability is reduced (see correlation coefficients ρ). At the same time the Dirac voltage is shifted towards positive values, which reflects a change in the charged trap density. (b) The top gate transfer characteristics of the double gated GFETs show a hysteresis due to charging/discharging of fast traps as well as a modulation of the Dirac point position by V_{BG}. (c) The output characteristics show signs of saturation and ambipolar channel effects.

V_{TG} - V_{Dirac} (t_s) ≈ const. This adjustment was done to maintain an approximately constant oxide field. The measurements have been repeated at two different temperatures (25 and 75 °C) with an intermediate baking step, which allowed us to reuse the devices to minimize complications due to device-to-device variations.

Fig. 2(a) shows that negative BTI (NBTI) stress on the top gate results mainly in a horizontal shift of the Dirac point voltage, V_{Dirac}. However, some vertical drift of the characteristics ΔI_{Dirac} is also present. These effects are most likely related to a change in the concentration of charged border traps which affect electrostatics and mobility. The presence of ΔI_{Dirac} makes the frequently used (but somewhat arbitrary) definition[15–17] of the threshold voltage V_{th} as the gate bias at which $I_d = (I_{dmax} + I_{dmin})/2$ questionable, also because I_d depends on other factors (e.g., contact resistance) and I_{dmax} is determined by the width of the V_{TG} interval. Thus, we suggest to use the Dirac point shift ΔV_{Dirac} as the main quantity for expressing GFET reliability, since ΔV_{Dirac} is directly linked to the variation of charged traps N_T and also independent of other factors. To further simplify the analysis, we always measured our devices at constant $V_d = 20$ mV and $V_{BG} = 0$. Experimental results illustrating the time evolution of the transfer characteristics during and after NBTI stress at two temperatures are shown in Fig. 2(b). As expected, a longer NBTI stress causes a stronger shift of V_{Dirac} towards more negative voltages. Significant drifts are recorded even at very low stress voltages, corresponding to about 1 MV/cm (compare to the typically used 4–8 MV/cm stress in Si technologies). During the recovery, V_{Dirac} returns back to its initial position which happens faster at higher temperature. We thus extract ΔV_{Dirac} for each of the measured characteristics and obtain the recovery traces versus the relaxation time.

The transfer characteristics given in Fig. 2 were measured by sweeping V_{TG} from positive to negative values (V^-

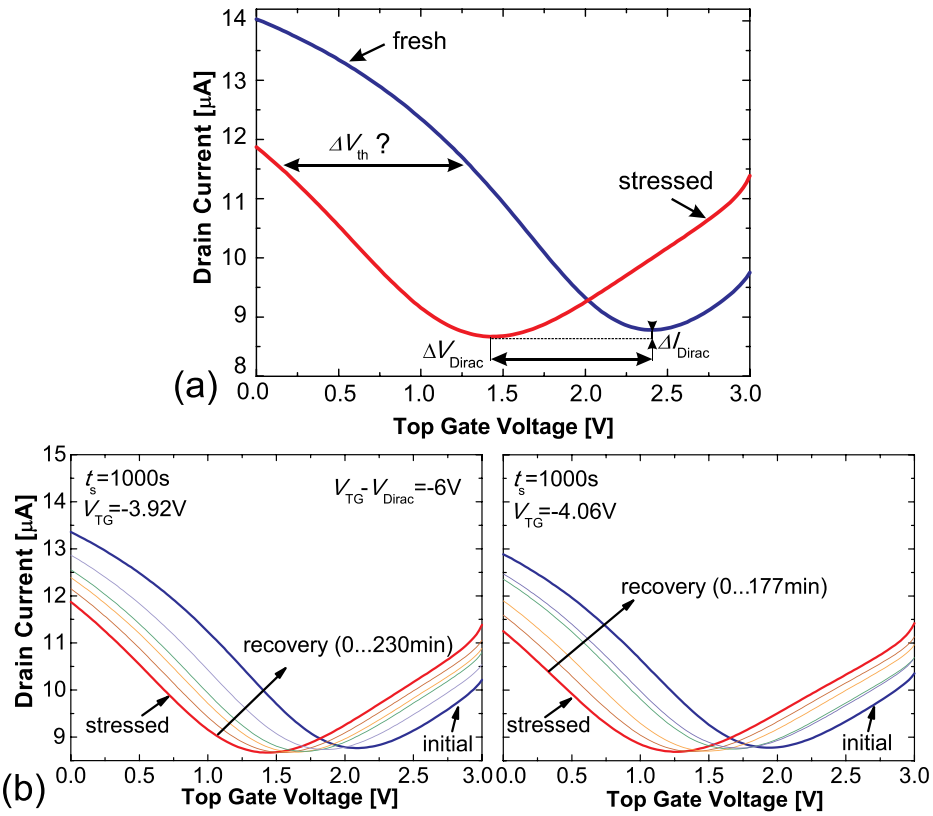

FIG. 2. (a) The typical impact of NBTI stress on the top gate results in both a horizontal and vertical shift of the Dirac point, expressed by ΔV_{Dirac} and ΔI_{Dirac}, respectively. (b) Time evolution of the top gate transfer characteristics after NBTI stress (shown for $t_s = 1000$ s) with V_{TG} - V_{Dirac} (t_s) ≈ const at 25 °C (left) and 75 °C (right).

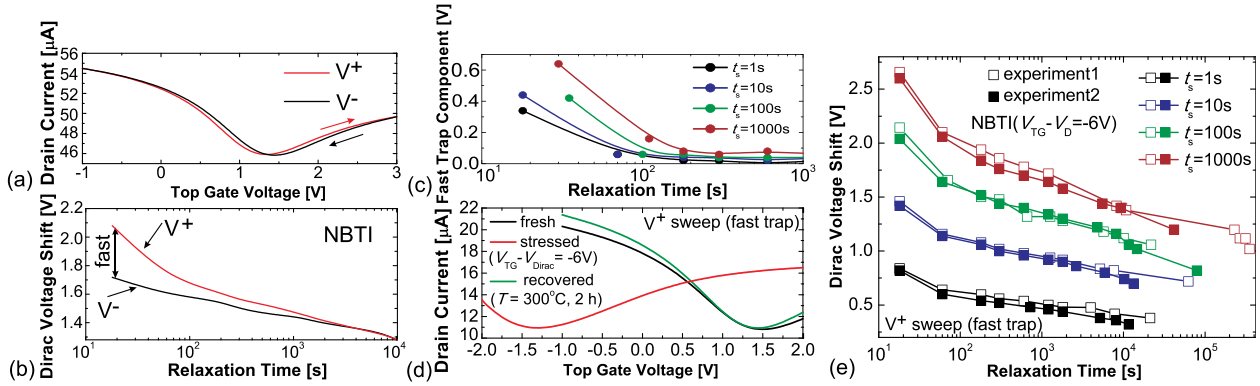

FIG. 3. (a) The presence of the fast trap component leads to a hysteresis-like impact on the transfer characteristics. (b) Recovery traces measured after NBTI-like stress in V^+ mode also contain a fast trap component. (c) The fast trap component strongly depends on the degradation magnitude and recovers quickly. (d) Baking of the device leads to a nearly complete recovery of NBTI stress. (e) The recovery traces obtained for the same device after baking are well reproducible.

mode). However, it has been observed that when the measurements are performed from negative to positive V_{TG} (V^+ mode), the initial NBTI degradation is more severe which is due to the presence of a fast trap component (Figs. 3(a) and 3(b)). This fast trap component is responsible for the pronounced hysteresis (cf. Fig. 1(b)) but also becomes stronger for larger ΔV_{Dirac} and recovers within about 100 s (Fig. 3(c)). However, contrary to NBTI, the sweep direction has almost no impact on the positive BTI (PBTI) magnitude. Fig. 3(d) illustrates that high-temperature baking at 300 °C for 2 h leads to a nearly complete recovery of NBTI degradation. This allows to minimize the impact of device-to-device variations by performing numerous measurements on the same device which makes the results easier to interpret. In Fig. 3(e), one can see the two sets of recovery traces measured for the same device at $T = 25$ °C, with an intermediate baking step at $T = 300$ °C for 2 h. The results are well reproducible, despite the presence of both fast and slower trap components. This allows us to capture the temperature dependence of BTI dynamics on the same device, which will thus be independent of variability issues.

However, since we are here primarily interested in the slow long-term degradation rather than the hysteresis, results similar to Fig. 2 (i.e., measured in V^- mode) are used for a detailed analysis. We demonstrate that the normalized ΔV_{Dirac} recovery traces measured without the fast trap component follow the universal relaxation relation $1/(1+B\xi^{\beta})$ with the normalized relaxation time $\xi = t_r/t_s$, with t_s and t_r being the stress and recovery times and B and β empirical fitting parameters (Figs. 4(a) and 4(b)). This observation was previously made for Si technologies.[22,23] Moreover, the parameters given in Fig. 4(c) are very similar to those obtained from Si data, *confirming the similarity in the underlying physical degradation processes*. However, contrary to Si technologies, no permanent ('dangling bond') component needed to be taken into account during the extraction.

For a final comparison with Si technologies, we show that the obtained recovery traces can be fitted with the capture/emission time (CET) map model[24] for both NBTI and PBTI. The CET map model assumes that BTI is the collective response of independent defects which exchange charges with the channel, each following a first-order non-radiative multiphonon process. Confirmed by extensive Si datasets, the essential ingredients of the model are the widely distributed, correlated, and temperature dependent capture and emission times, which can be well described using bivariate Gaussian distributions of the respective activation energies. The sets of experimental ΔV_{Dirac} recovery traces fitted with the simulation results and the corresponding CET map distributions are given in Fig. 5 for both NBTI and PBTI; the same absolute value of V_{TG} - V_{Dirac} and two different temperatures have been used. The charged trap density can be roughly estimated as $\Delta N_T = \Delta V_{Dirac}\, C_{ox}/q$, where the oxide capacitance C_{ox} is considered to be a superposition of the geometrical and quantum capacitances, i.e., $C_{ox} = C_{geom}C_q/(C_{geom}+C_q)$ with the quantum capacitance estimated as

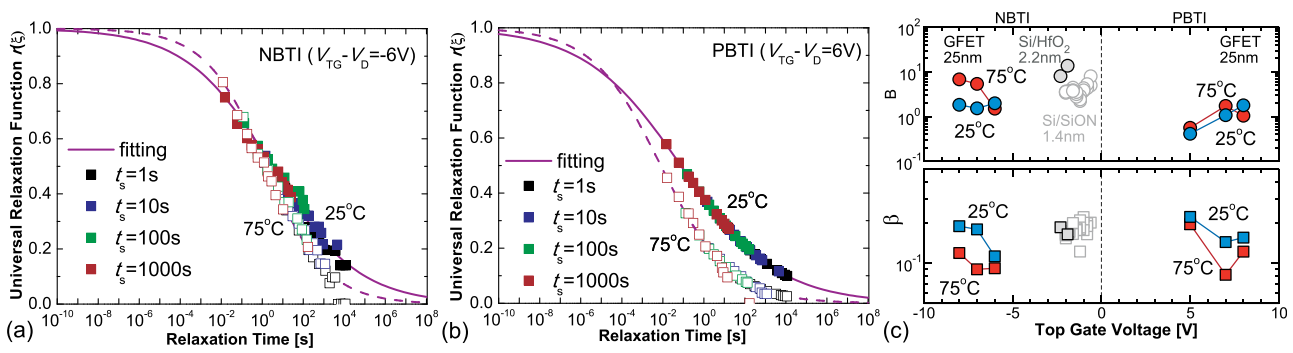

FIG. 4. In Si technologies, it has been observed that BTI recovery follows a universal relaxation relation which is also the case for NBTI (a) and PBTI (b) recovery in GFETs. Quite remarkably, the parameters (c) are very similar to those required to fit Si data.

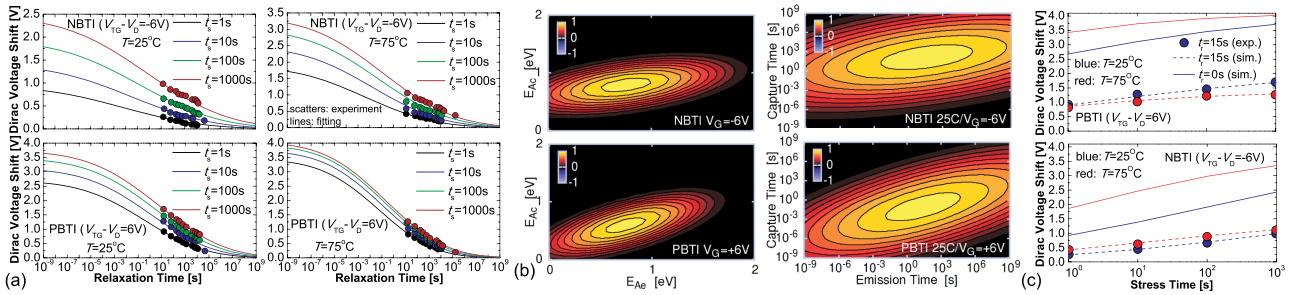

FIG. 5. (a) The $\Delta V_{\mathrm{Dirac}}$ recovery traces for NBTI and PBTI at two different temperatures fitted with the CET map model. (b) The underlying Gaussian distributions for activation energies and time constants (25 °C). The extracted CET distributions closely resemble those for Si technologies.[24] (c) Back-extrapolation to zero measurement delay using the CET map model allows to obtain $\Delta V_{\mathrm{Dirac}}$ values at $t_r \approx 0$.

$C_q = 1\ \mu\mathrm{F/cm}^2$. The typical initial ΔN_T values for GFETs are around $10^{12}\,\mathrm{cm}^{-2}$ which is considerably larger than for Si technologies ($10^{10}\,\mathrm{cm}^{-2}$).

In our first studies,[25] when the measurements were done without an intermediate high-temperature baking/recovery step, we had to investigate the BTI dynamics for various stress conditions on different devices. In that case simultaneous fits of data for different stress conditions were often difficult to obtain, because the detrimental effects of variability (cf. Fig. 1) are not considered in the CET map model. However, the experimental results measured on the same devices (Fig. 5) are fully consistent with the theory. For example, at higher T the degradation is stronger and recovery is faster, similarly to Si technologies (Fig. 5(a)). As a consequence of the relatively large measurement delay caused by the full I_d - V_{TG} sweeps, in some cases the degradation appears to be lower at higher T, in agreement with the previous results.[15,17] By correction of the measurement delay using the CET map extrapolation to $t_r = 0$ we suggest this to be an artefact (Figs. 5(a) and 5(c)). Note that the obtained CET distributions (Fig. 5(b)) are very similar to the ones extracted for Si technologies.[24]

In Si technologies, two Gaussian distributions have to be used to describe the NBTI recovery data.[26,27] The first one dominates the experimentally observed recovery and has mean activation energies for capture and emission slightly below 1 eV, just like our GFETs. The second distribution has mean activation energies at about 1.5 eV/2 eV for capture and emission, respectively. This second distribution has been tentatively assigned to dangling bonds (P_b centers). Interestingly, this distribution is absent in our graphene transistors, consistent with the Van der Waals bonding between graphene and Al_2O_3. Overall, we conclude that the CET map model established for Si MOSFETs can be applied to GFETs as well.

In summary, we have performed a detailed study of BTI degradation and recovery in GFETs. High-temperature baking of the devices allowed to decrease device-to-device variability and to perform numerous measurements on the same device. Together with an optimized experimental technique, in which a constant oxide field is sustained during all measurements, experimental results fully consistent with Si technologies could be obtained. This BTI assessment methodology is thus suitable for quantifying the quality and reliability of graphene FETs and graphene/dielectric interfaces in general.

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