Asymmetric Gate Schottky-Barrier Graphene Nanoribbon FETs for Low-Power Design

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***Abstract*— The ambipolar behavior limits the performance of Schottky-barrier-type graphene nanoribbon field-effect transistors (SB-GNRFETs). We propose an asymmetric gate (AG) design for SB-GNRFETs, and show that it can significantly reduce the $I_{\rm OFF}$. Simulation results indicate at least 40% and 5× improvement in the subthreshold swing and the $I_{\rm ON}/I_{\rm OFF}$ ratio, respectively. We build an accurate semianalytical closed-form model for the current–voltage characteristics of SB-GNRFETs. The proposed Simulation Program with Integrated Circuit Emphasis (SPICE)-compatible model considering various design parameters and process variation effects, which enables efficient circuit-level simulations of SB-GNRFET-based circuits. Simulation results of benchmark circuits show that the average energy-delay product of the AG SB-GNRFETs is only ∼22% of that of a symmetric gate for the ideal case and ∼88% for devices with line edge roughness.**

***Index Terms*— Asymmetric gate (AG), graphene nanoribbon field-effect transistor (GNRFET), Schottky-barrier (SB).**

I. Introduction

GRAPHENE has received much attention as a base material for nanoelectronic devices because of the outstanding physical and electrical properties. There are two varieties of graphene nanoribbon field-effect transistors (GNRFETs): Schottky-barrier (SB)-type and MOSFET-type [1]. In MOS-type GNRFETs, the reservoirs are doped with donors or acceptors. In SB-type devices, metals are used for contacts and graphene as the base channel material, which results in the formation of SBs at the interfaces. One advantage of SB-GNRFETs is that they require no additional doping in the contacts or the channel. Therefore, it reduces the technical difficulties in the fabrication and eliminates doping variation. Most reported GNRFETs are SB type [2]. However, one drawback of SB-GNRFET is its ambipolar behavior that results in performance limitation, and SB-GNRFETs demonstrate a low $I_{\rm ON}/I_{\rm OFF}$ ratio in comparison with their MOS-type counterparts. Meanwhile, a relatively large $I_{\rm OFF}$ results in large power consumption in the OFF-state.

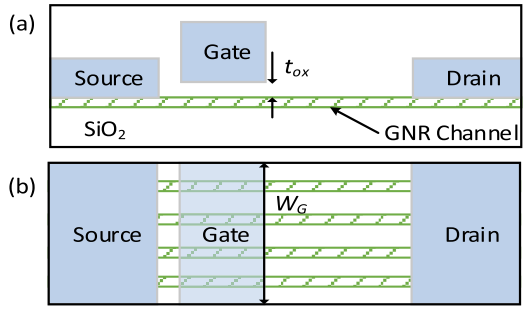

Fig. 1. (a) Structure of an AG SB-GNRFET device. (b) Structure of a four-ribbon SB-GNRFET.

The ambipolar current conduction in SB-GNRFETs is due to the parasitic tunneling current through the SB at the drain contact. This problem exists also in carbon nanotube-based FETs [3]. To suppress the parasitic tunneling current in SB carbon nanotube FETs, a double-gate structure has been proposed [3]–[5]. In [3], the first gate controls carrier injection from the source contact, whereas the second gate makes the band-edge profile near the drain nearly flat. Therefore, the parasitic tunneling current is reduced and the ambipolar behavior is suppressed. An additional gate, however, poses some fabrication difficulties. In this paper, we propose a SB-GNRFET with a single asymmetric gate (AG) and show that this avoids parasitic carrier injection at the drain and the device characteristics are improved. A semianalytical model for this structure is derived, implemented in Simulation Program with Integrated Circuit Emphasis (SPICE), and is applied to evaluate circuit level performance. Our results indicate that the AG device outperforms the symmetric gate (SG) structure.

II. Device Structure and Modeling

The proposed AG device is shown in Fig. 1(a) (cross-sectional view) and Fig. 1(b) (top view). In an SG device, where the gate covers the whole channel, as the voltage difference between the gate and drain increases, the SB at the drain contact gets thinner, and as a result, the tunneling current increases [Fig. 2(a)]. For AG structure, the thickness of the SB at the drain contact is only weakly affected by the gate

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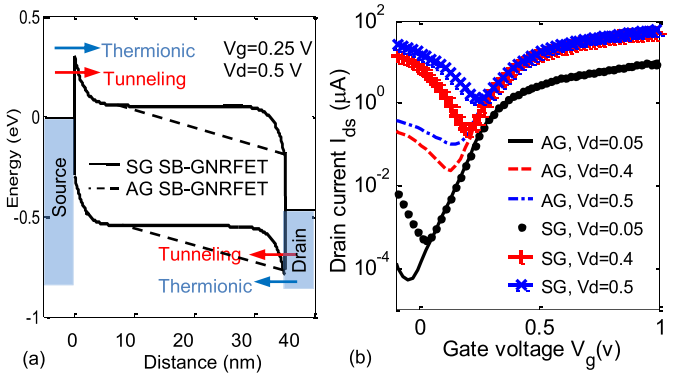

Fig. 2. (a) Band-edge profile along the channel of the AG and SG devices. (b) Transfer characteristics of the AG and SG devices. Device simulations are performed by employing an atomistic tight-binding model for the electron bandstructure along with the nonequilibrium Green's function formalism for the electronic transport [4].

voltage, and as a result, the tunneling current is significantly smaller than that of a SG structure. In the double-gate structure proposed in [3], the parasitic tunneling current can be completely suppressed, whereas for the AG structure, the parasitic current is not completely suppressed [Fig. 2(b)]. However, in comparison with the double-gate structure proposed in [3], the AG structure can be more easily fabricated while still having an acceptable performance.

The proposed structure is similar to conventional MOSFETs, except that the gate only partially covers the channel. Therefore, its scaling is similar to that of MOSFETs. Furthermore, this structure has the advantage that it can be scaled on the basis of the number of ribbons in each transistor [6].

We proposed a semianalytical model for the current-voltage (I–V) characteristics of SB-GNRFETs, which allows complete and thorough exploration and evaluation of SB-GNRFET circuits [6]. This is a physics-based semianalytical model for the I–V characteristics of SB-GNRFETs. We carry out accurate approximations of SB tunneling, channel charge, and current, which provide improved accuracy while maintaining compactness. The proposed model considers various design parameters and process variation effects, including graphene-specific line edge roughness, which allows complete and thorough exploration and evaluation of SB-GNRFET circuits.

The tunneling through the SB of the device with the oxide thickness $t_{\rm ox}$ is computed using the Wentzel–Kramers–Brillouin (WKB) approximation according to the barrier profile

$$E_{\rm SB}(Z) = A_s e^{-\pi z/2t_{\rm ox}} \tag{1}$$

with $A_s = q\varphi_{\rm ch}$, the classical turning points $z_1 = 0$ and $z_2 = -2t_{\rm ox}\ln(E/A_s)/\pi$, and the wavevector

$$k_z(E) \simeq \sqrt{M_\alpha(E_\alpha^2 - \varepsilon_\alpha^2)/\hbar^2\varepsilon_\alpha} \tag{2}$$

which is obtained by a second-order expansion of the GNR E–k dispersion relationship

$$E_\alpha(k) = \pm\tau\sqrt{1 + 4A_\alpha\cos\frac{\sqrt{3}a_l k}{2} + 4A_\alpha^2}. \tag{3}$$

The resulting transmission coefficient is obtained as

$$T(E) = \exp\left\{-8t_{\rm ox}\sqrt{M_\alpha/h^2\varepsilon_\alpha}\left[(E+\varepsilon_\alpha)\left(\frac{\pi}{2} - \operatorname{atan}\frac{\varphi_\alpha}{\gamma_1}\right) + \gamma_1 + \gamma_2\left(\operatorname{atan}\left(\frac{\gamma_1\gamma_2}{A_s(E+\varepsilon_\alpha) - E(E+2\varepsilon_\alpha)}\right) - \theta_0\right)\right]\right\} \tag{4}$$

where h is the Planck's constant, $E = E_\alpha(k) - \varepsilon_\alpha$ is the energy with respect to the band edge energy $\varepsilon_\alpha = E_\alpha(0)$, M_α is the effective mass, and the other parameters are defined as

$$\gamma_1 = \sqrt{\varepsilon_\alpha^2 - \varphi_\alpha^2}, \quad \gamma_2 = \sqrt{(\varphi_\alpha + A_s)^2 - \varepsilon_\alpha^2}$$
$$\varphi_\alpha = \varepsilon_\alpha + E - A_s, \quad \theta_0 = \begin{cases} \pi & E(2\varepsilon_\alpha + E) < A_s(\varepsilon_\alpha + E) \\ 0 & \text{otherwise} \end{cases} \tag{5}$$

In the case of $\varphi_{\rm ch}$ greater than the $E_g = 2\varepsilon_\alpha$, the spatial band diagram curvature becomes high enough to trigger band-to-band tunneling. In this case, a carrier with energy $0 < E < A_s - 2\varepsilon_\alpha$ experiences an SB of a height $A_s = E + 2\varepsilon_\alpha$.

The effect of the AG is considered in the hole's tunneling through the SB at the drain side. Tunneling through this barrier is proportional to the drain voltage (V_d). Lower drain voltage results in a flatter band diagram at the drain contact, which in turn reduces the tunneling current [Fig. 2(a)]. We derived an empirical equation for the effective tunneling coefficient of the holes at drain contact as

$$T_{\rm eff}(E) = T(E)\cdot {V_d}^3/70. \tag{6}$$

The equivalent circuit of the GNRFET, which is shown in Fig. 3(a), consists of channel current source $I_{\rm ds}$, parasitic capacitors $C_{{\rm ch},d}$, $C_{{\rm ch},s}$, $C_{g,{\rm ch}}$, and $C_{\rm sub,ch}$, and the voltage-controlled voltage source $V_{\rm ch}$ representing the channel voltage $V_{\rm ch}$. The capacitors $C_{\rm gd}$ and $C_{\rm gs}$ are modeled using FastCap. Intrinsic capacitor $C_{{\rm ch},d}(s) = \partial Q_{\rm ch}/\partial V_{d(s)}$ is implemented in SPICE as voltage-controlled capacitor by defining the charge equations. The total channel charge $Q_{\rm ch}$ of carriers subband α can be expressed as

$$Q(\varphi_{\rm ch}) = q\int D\cdot G_Q dE \tag{7}$$

where q is the electron charge, $D = (2/\pi\hbar)/(M_\alpha/2E)^{1/2}$ is the density of states, and G_Q is defined as

$$G_Q(E) = \frac{T_s(2-T_d)f(E_{\alpha,s}) + T_d(2-T_s)f(E_{\alpha,d})}{T_s + T_d - T_sT_d} \tag{8}$$

in which

$$f(x) = \frac{1}{1+\exp(x/k_bT)} \tag{9}$$

is the Fermi–Dirac distribution function with the Boltzmann constant k_b and the temperature T. The term G_Q should be computed for both electrons and holes with

$$E_{s(d)}^e = E + \varepsilon_\alpha - q\varphi_{\rm ch} + V_{s(d)}$$
$$E_{s(d)}^h = E - \varepsilon_\alpha + q\varphi_{\rm ch} - V_{s(d)}. \tag{10}$$

In our model, all subbands are considered and different SBs exist for each subband. The first subband, however, contributes

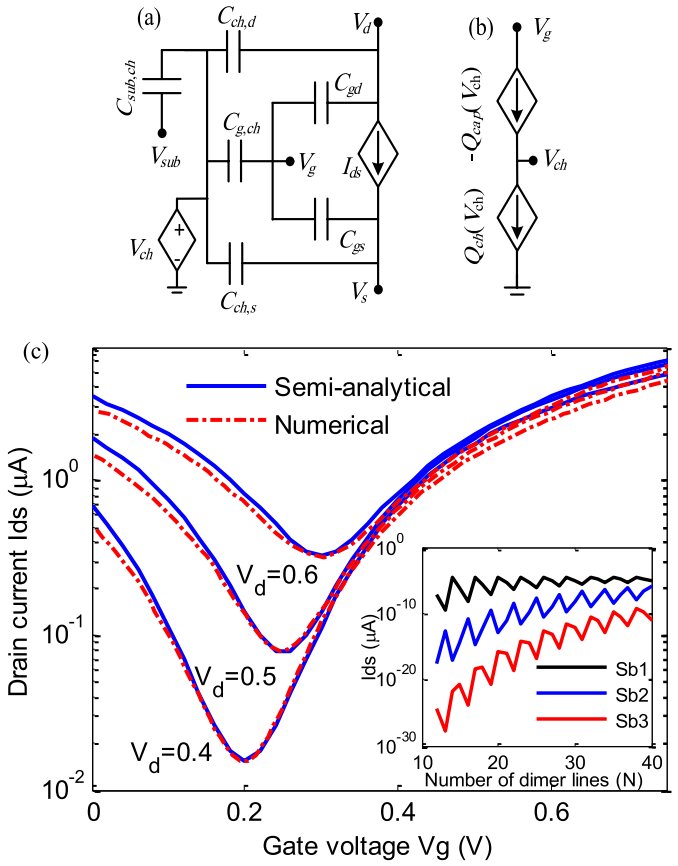

Fig. 3. (a) Schematic of the developed compact circuit model of a SB-GNRFET. (b) SPICE setup for self-consistent solution of the channel potential V_{ch}. (c) Comparison with atomistic device simulation ($N = 12$, $t_{ox} = 2$ nm) [6]. Inset: contribution of three lowest subbands to the current of GNRFETs with different width.

the most to the total current and the contribution of higher subbands exponentially decreases as the energy of the subband increases [Fig. 3(c), inset].

We analytically calculated G_Q by piecewise linear approximation defined by four values $E_{c1}, E_{c2,Q}, G_{Q,0} = G_Q(0)$, and $G_{Q,1} = G_Q(E_{c1})$. The local maximum point of G_Q, the energy E_{c1}, is obtained as

$$E_{c1} = k_b \cdot T[W(\exp(E_f/k_bT - 1) + 1)] \tag{11}$$

where $W(\cdot)$ is the Lambert W function that is approximated as constant, parabolic, or linear functions according to the typical ranges of T and $E_f = -\varepsilon_\alpha + q\varphi_{ch} - V_s$ as

$$E_{c1}(E_f, T) = \begin{cases} k_bT & E_f < -0.05 \\ p_1E_F^2 + p_2E_F + p_3 & -0.05 < E_f < 0.145 \\ p_4E_F + p_5 & E_f > 0.145 \end{cases} \tag{12}$$

where $p_i, i = 1, 2, \ldots, 5$ is temperature-dependent coefficient as $p_i = \eta_{i,1} \cdot T + \eta_{i,2}$. Values of $\eta_{i,1}$ and $\eta_{i,2}$ obtained by curve fitting are given in Table I.

The term $E_{c2,Q}$ is approximated using

$$f(E_{c2,Q} - E_f) \simeq G_{Q,1}/10. \tag{13}$$

TABLE I
VALUES OF TEMPERATURE-DEPENDENT COEFFICIENTS

i	1	2	3	4	5
$\eta_{i,1}$	-0.0041	-1.33e-4	1.016e-4	-4.47e-4	6.29e-5
$\eta_{i,2}$	3.4092	0.2827	0.0035	1.0082	-0.0315

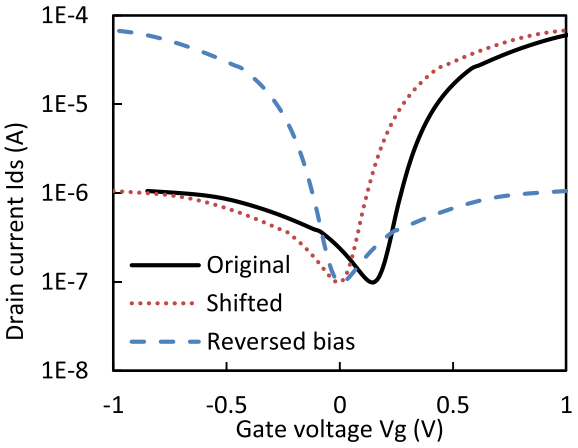

Fig. 4. Transfer characteristics of the AG SB-GNRFET device with proper shifting and reversed bias.

TABLE II
SUBTHRESHOLD SWING AND I_{ON}/I_{OFF} RATIO OF EACH DEVICE. FOR GNRFETS, DEVICES OF DIFFERENT EDGE ROUGHNESS (P_R) ARE LISTED

Device	p_r	S (mV/dec)	I_{on}/I_{off}	V_{DD} (V)
Si-CMOS (HP)	-	93.46	3.49E+3	0.7
SG SB-GNRFET	0	145.14	3.21E+01	0.5
	0.1	735.29	2.11E+00	0.5
AG SB-GNRFET	0	86.96	3.04E+02	0.5
	0.1	197.24	9.98E+00	0.5

The integration introduced by Q_α can be therefore analytically computed as

$$Q = \left(4q\sqrt{2M_\alpha}/3\pi\hbar\right)\left[\sqrt{E_{c1}} \cdot G_{Q,0} + G_{Q,1} \cdot E_{c2,Q}/\left(\sqrt{E_{c1}} + \sqrt{E_{c2,Q}}\right)\right]. \tag{14}$$

The same method can be used to compute the hole's charge by using $E_f = -(-\varepsilon_\alpha + q\varphi_{ch} - V_d)$. The total mobile charge $Q_{ch} = \sum_\alpha (Q^h - Q^e)$ must be equal to the charge Q_{cap} across the gate, source, and drain capacitors that couple with the channel and are modeled empirically from data extracted from FastCap. Equating Q_{ch} and Q_{cap} yields a solution of φ_{ch}, which can be obtained using the equation solver circuit as shown in Fig. 3(b) [7]. Given φ_{ch}, the current through the channel is computed using the Landauer–Büttiker formalism

$$I = \frac{q}{\pi\hbar}\int G_I(E)dE \tag{15}$$

$$G_I(E) = T_I[f(E - E_{\alpha,s}) - f(E - E_{\alpha,d})] \tag{16}$$

$$T_I = \frac{T_sT_d}{T_s + T_d - T_sT_d} \tag{17}$$

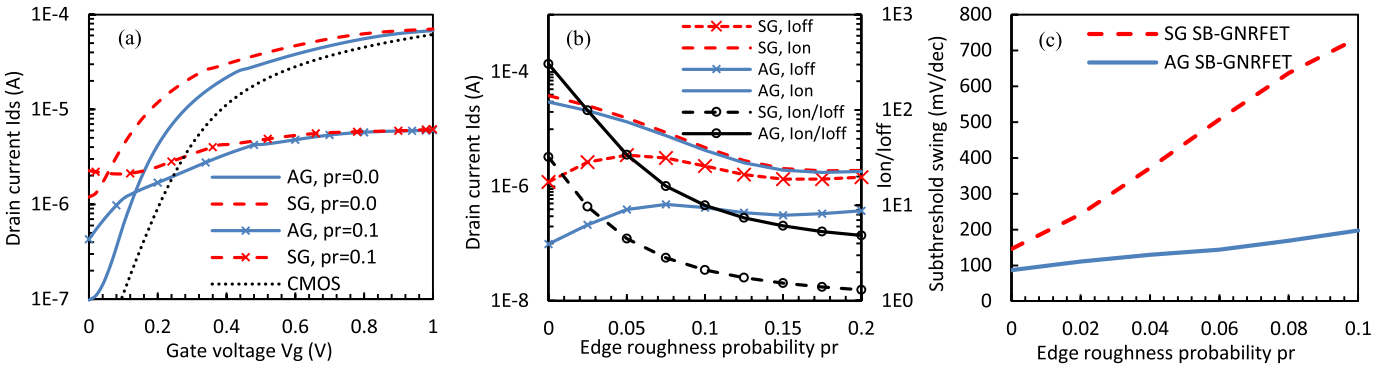

Fig. 5. (a) Comparison between the transfer characteristics of the AG and SG devices. (b) I_{ON} and I_{OFF} of AG and SG devices and I_{ON}/I_{OFF} ratio as functions of p_r. (c) Subthreshold swing of the AG and SG devices as functions of p_r.

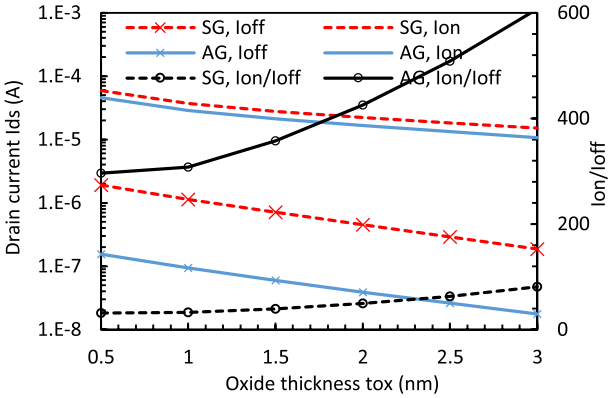

Fig. 6. I_{ON}, I_{OFF}, and I_{ON}/I_{OFF} versus oxide thickness t_{ox}.

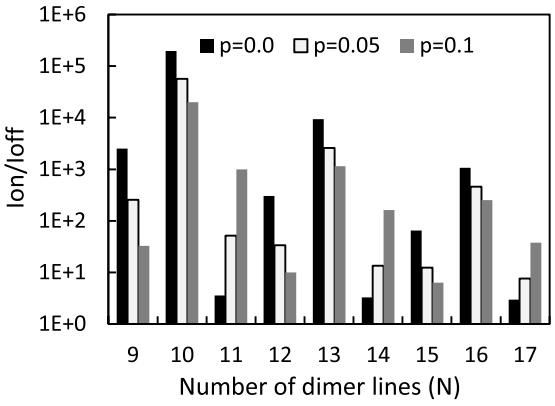

Fig. 7. I_{ON}/I_{OFF} versus dimer lines of AG SB-GNRFET.

which can be analytically approximated using the same method for channel charge as

$$I = (q/2\pi\hbar)[G_{I,0} \cdot E_{c1} + G_{I,1} \cdot E_{c2,I}]. \tag{18}$$

The absence of some atoms at the edges of GNR can significantly affect electronic transport in GNRs [1], [4], [6], [8]. The degree of roughness of the edges of a GNR is considered in our model through the line edge roughness probability p_r, which is the probability that any atom at the edges of a GNR is removed [8]. The effects of line edge roughness are modeled as $I_{\text{rough}} = A \cdot I_{\text{DS}}(\varepsilon_{\alpha,\text{eff}})$, where the scattering coefficient, A, and the effective subband, $\varepsilon_{\alpha,\text{eff}}$, are empirically obtained [8]. The accuracy of the developed compact model is verified with the atomistic nonequilibrium Green's function device simulator NanoTCAD ViDES [9] [Fig. 3(c)].

We consider ambipolar devices, where the metal Fermi level is located in the middle of the GNR band gap at each contact. The minimum current in SB-GNRFETs occurs at the so-called *ambipolar conduction point* [6]. Ideally, the minimum current should occur in the OFF-state when $V_{GS} = 0$. The minimum current point, however, can be shifted to a different V_{GS} by tuning the gate work function by using various gate materials [10], [11]. The AG SB-GNRFET can operate as a p-type device just by reversing the polarity of the applied voltages, which suppress the electron's parasitic current [3], [5]. An example of AG SB-GNRFETs working under $V_{DD} = 0.5$ V with ideal amount of 0.15 V shifting is shown in Fig. 4.

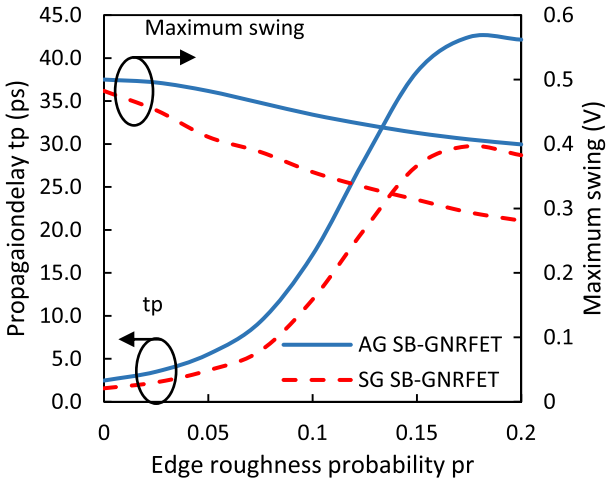

Fig. 8. Effect of line edge roughness on inverter propagation delay, t_p, and maximum output swing of inverter.

III. Simulation Results and Performance Assessment

For comparison purpose, we used the 16 nm high-performance (HP) CMOS from predictive technology models (PTM). Minimum CMOS transistor dimension is chosen as $(W/L) = (32\text{ nm}/16\text{ nm})$. The transistor dimensions of the GNRFETs are scaled to match the PTM libraries. We choose an SB-GNRFET device with $t_{ox} = 1$ nm, and six ribbons in

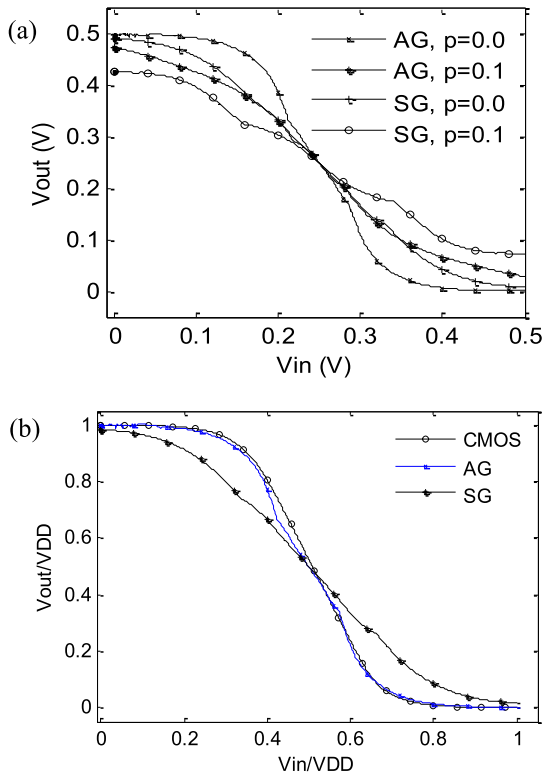

Fig. 9. Inverter dc characteristic. (a) Effect of p_r for AG and SG-based inverter. (b) Comparison of different technologies. Voltages are normalized to V_{DD} in each technology.

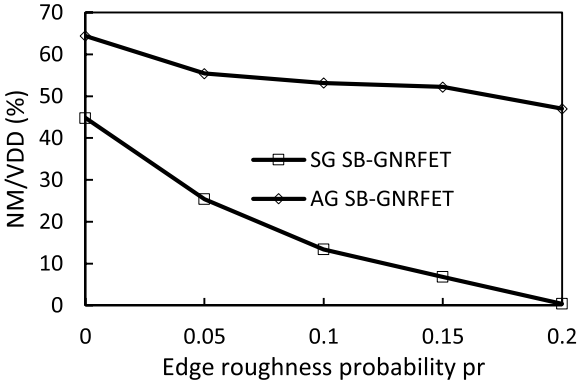

Fig. 10. Normalized noise margin of an AG- and SG-based inverters.

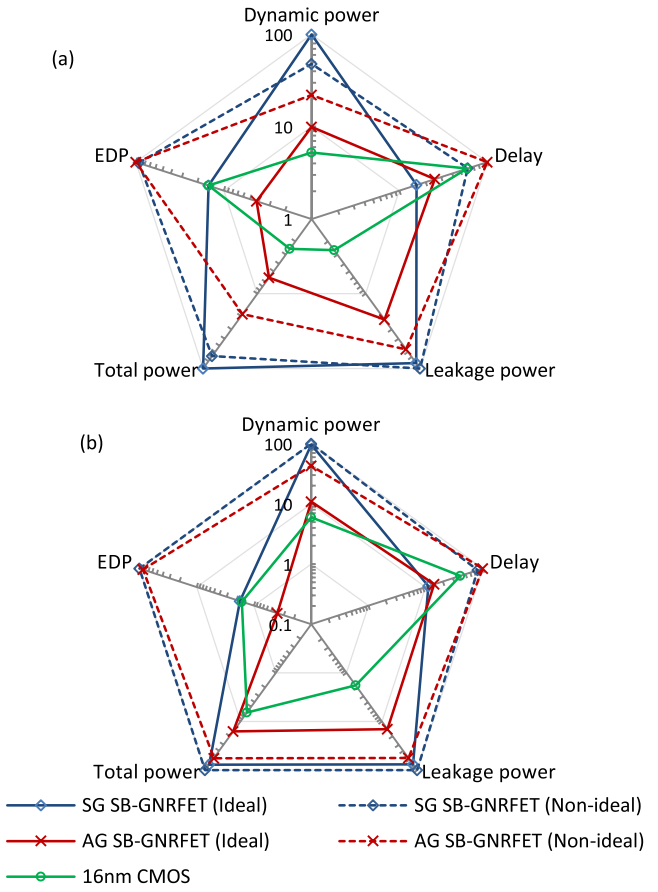

Fig. 11. Comparison of different technologies based on five figures of merits: delay, dynamic power, leakage power, total power, and EDP. The number for each figure of merit is the average value that is normalized to the maximum value of that category and presented in percentage. Each axis has a maximum value of 100%. (a) Basic logic gates. (b) Benchmark circuits.

the channel each with $N = 12$ dimer lines (with the band gap $E_g \approx 0.6$ eV) for the rest of our paper [Fig. 1(b)] [1], [6], [8]. Both the ideal cases ($p_r = 0$) and the nonideal cases with $p_r = 0.1$ are investigated. The supply voltage for 16 nm CMOS and SB-GNRFET are 0.7 and 0.5 V, respectively.

Fig. 5(a) shows the comparison of the transfer characteristics of SG and AG SB-GNRFETs for the ideal (GNR edges are smooth) and nonideal cases (GNR edges are rough). I_{ON} of the AG is nearly the same as the SG device, whereas the I_{OFF} of AG is considerably smaller ($\sim 11\times$) than that of the SG device. As a result, the AG SB-GNRFET in the ideal case shows about a $10\times$ improvement in the I_{ON}/I_{OFF} ratio; however, as shown in Fig. 5(b), the I_{ON}/I_{OFF} ratio improvement is smaller ($\sim 5\times$) in the presence of GNR line edge roughness. Fig. 5(c) shows that by employing the AG device, the subthreshold swing is improved by at least 40%. Table II shows the subthreshold swing S and I_{ON}/I_{OFF} ratio of each device under, respectively, chosen V_{DD}. It is shown that ideal AG SB-GNRFETs have the lower subthreshold swing and higher I_{ON}/I_{OFF} ratio than SG SB-GNRFETs. However, the AG SB-GNRFET device has still lower I_{ON}/I_{OFF} ratio than that of the CMOS because of the large V_d and thin SB tunneling distance due to the scaled oxide thickness.

Fig. 6 shows the effect of t_{ox}. A higher t_{ox} implies a smaller tunneling probability through the SB, which results in the lower current. However, I_{ON}/I_{OFF} ratio increases with the increase in oxide thickness. Furthermore, AG device has much higher ratio than SG. Fig. 7 shows the effect of dimer lines N, which tracks the periodic effect on band gaps [12]. For $N = 3q + 2$, ($q \epsilon \mathbb{N}$), the band gap is very small, resulting in a low I_{ON}/I_{OFF} ratio. For $N = 3q$, there is a moderate band gap, which results in a high I_{ON}/I_{OFF} ratio and a high I_{ON}. For $N = 3q + 1$, the band gap is the largest, which results in the highest I_{ON}/I_{OFF} ratio. Also note that the I_{ON}/I_{OFF} ratio tends to increase as N decreases.

We analyze properties of an inverter built with SG and AG SB-GNRFETs under $V_{DD} = 0.5$ V. We used our SPICE model to perform dc and transient analysis of the inverter. As shown

TABLE III
SIMULATION RESULTS OF BASIC LOGIC GATES

	Delay (ps)				Dynamic power (μW)				Leakage power (μW)				EDP (J.s)			
	SG SB-GNRFET		AG SB-GNRFET		SG SB-GNRFET		AG SB-GNRFET		SG SB-GNRFET		AG SB-GNRFET		SG SB-GNRFET		AG SB-GNRFET	
Circuit	pr=0.0	pr=0.1	pr=0.0	pr=0.1	pr=0.0	pr=0.1	pr=0.0	pr=0.1	pr=0.0	pr=0.1	pr=0.0	pr=0.1	pr=0.0	pr=0.1	pr=0.0	pr=0.1
inv1	1.00	9.00	3.30	17.00	3.47	0.82	0.13	0.64	0.52	0.69	0.10	0.35	3.47E-30	6.64E-29	1.46E-30	1.85E-28
nand2	3.00	12.00	5.20	20.30	3.28	1.06	0.15	0.72	0.70	0.79	0.17	0.43	2.95E-29	1.52E-28	3.98E-30	2.97E-28
nand3	4.00	15.00	6.00	23.00	1.54	0.87	0.10	0.56	0.67	0.75	0.20	0.39	2.47E-29	1.96E-28	3.70E-30	2.95E-28
nor2	3.00	11.00	5.00	22.00	2.26	1.15	0.15	0.28	0.67	0.75	0.13	0.42	2.03E-29	1.39E-28	3.83E-30	1.37E-28
xor2	6.00	17.00	8.00	23.00	5.01	2.50	0.79	1.02	3.37	4.07	0.64	2.38	1.80E-28	7.23E-28	5.05E-29	5.40E-28
nor3	4.00	13.00	7.00	29.00	1.28	1.25	0.37	0.37	0.72	0.80	0.42	0.42	2.05E-29	2.11E-28	1.81E-29	3.10E-28
nand4	4.00	19.00	6.00	25.00	1.22	1.04	0.10	0.39	0.65	0.76	0.26	0.36	1.96E-29	3.75E-28	3.47E-30	2.45E-28
Average	3.57	13.71	5.79	22.76	2.58	1.24	0.26	0.57	1.04	1.23	0.27	0.68	4.26E-29	2.66E-28	1.21E-29	2.87E-28

TABLE IV
SIMULATION RESULTS OF BENCHMARK CIRCUITS

	Delay (ps)				Dynamic power (μW)				Leakage power (μW)				EDP (J.s)			
	SG SB-GNRFET		AG SB-GNRFET		SG SB-GNRFET		AG SB-GNRFET		SG SB-GNRFET		AG SB-GNRFET		SG SB-GNRFET		AG SB-GNRFET	
Circuit	pr=0.0	pr=0.1	pr=0.0	pr=0.1	pr=0.0	pr=0.1	pr=0.0	pr=0.1	pr=0.0	pr=0.1	pr=0.0	pr=0.1	pr=0.0	pr=0.1	pr=0.0	pr=0.1
c17	10.00	62.00	10.00	70.00	5.57	6.74	1.13	4.24	4.65	5.77	0.91	3.34	5.57E-28	2.59E-26	1.13E-28	2.08E-26
b02	10.00	72.00	14.30	116.00	53.99	60.10	5.32	20.37	21.99	28.95	4.09	16.37	5.40E-27	3.12E-25	1.09E-27	2.74E-25
s27	12.20	92.00	17.00	114.00	11.78	13.19	1.98	7.95	8.95	12.61	1.65	6.98	1.75E-27	1.12E-25	5.72E-28	1.03E-25
cla	7.00	59.00	8.00	49.00	9.97	4.62	0.83	3.76	3.80	4.56	0.82	2.51	4.88E-28	1.61E-26	5.34E-29	9.02E-27
Average	9.80	71.25	12.32	87.25	20.33	21.16	2.31	9.08	9.85	12.97	1.87	7.30	2.05E-27	1.16E-25	4.56E-28	1.02E-25

in Fig. 8, high line edge roughness probability p_r results in a higher propagation delay due to the smaller transistor current. Both low and high output voltage levels of the inverter degrade with line edge roughness, which results in the lower maximum swing. AG-based inverter has better properties than SG one.

Fig. 9(a) shows the voltage transfer curves of an inverter built with AG and SG SB-GNRFETs with different line edge roughness settings. V_{in} and V_{out} are the input and output voltages of the inverter, respectively. High line edge roughness probability p_r results in a lower voltage swing. Fig. 9(b) shows the voltage transfer curves of the inverters in different technologies which are normalized to the corresponding V_{DD}. Fig. 10 shows the normalized noise margin of different inverters. AG-based inverter has better noise margin than the SG. The line edge roughness significantly reduces the noise margin of SG-based inverter, while it has small effect on AG.

To evaluate the AG SB-GNRFET performance on the circuit level, basic gates (*inv*, *nand*2, *nand*3, *nor*2, *xor*2, *nor*3, *nand*4), and benchmark circuits are studied, including circuits *c17* from ISCAS '85, *b02* from ITC '99, *s27* from ISCAS '89, and carry generator for the third bit of a carry look-ahead adder (*cla*). Simulation results of basic gates and benchmark circuits are presented in Tables III and IV, respectively. The reported values are the maximum delay, dynamic power, leakage power, and Energy-delay product (EDP) values.

Fig. 11 shows the performance of each technology node in terms of maximum delay, dynamic power, leakage power, total power, and EDP values. An ideal AG SB-GNRFET has the best EDP, but its leakage power is higher than that of CMOS. The nonideal AG SB-GNRFET has the worse delay because of its relatively lower I_{ON}. Because of a lower I_{OFF} of AG SB-GNRFET, the circuits, either ideal or nonideal, have lower power than that of the SG SB-GNRFET (e.g., 73% or 44% lower leakage power for basic gates). Nonideal SB-GNRFET (both AG and SG) consumes more leakage power than the ideal one because its I_{OFF} is increased in the presence of line edge roughness. This also reduces the $I_{\text{ON}}/I_{\text{OFF}}$ ratio and results in the degradation of the delay and EDP.

IV. CONCLUSION

To improve the performance of SB-GNRFETs, the ambipolar behavior of these devices should be suppressed. We propose a device with an AG which covers only some part of the channel close to the source contact. The newly proposed design effectively suppresses the ambipolarity and reduces the I_{OFF} by 11×. A SPICE-compatible compact model of the proposed device is developed. Simulation results show significant improvement in device and circuit characteristics, which render AG SB-GNRFET as a potential candidate for next-generation high-performance low-power device. However, advanced fabrication techniques are required to remove the nonidealities faced by GNR fabrication.

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