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On the importance of electron–electron scattering for hot-carrier degradation

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Using our physics based model for hot-carrier degradation (HCD) we analyze the importance of the effect of electron–electron scattering (EES) on HCD in transistors with different channel lengths. The model is based on a thorough treatment of carrier transport and is implemented into the deterministic Boltzmann transport equation solver ViennaSHE. Two competing mechanism of Si–H bond-breakage are captured by the model: the one triggered by the multiple vibrational excitation of the bond and another which is due to excitation of one of the bonding electrons to an antibonding state by a solitary hot carrier. These processes are considered self-consistently as competing pathways of the same dissociation reaction. To analyze the importance of the EES process we use a series of nMOSFETs with identical architecture but different gate lengths. The gate length varies in the wide range of 44–300 nm to cover short-channel MOSFETs as well as their longer counterparts. According to previous findings, EES starts to become important at a channel length of 180 nm. This situation is captured in the targeted gate length interval. Our results show that the channel length alone is not a sufficient criterion on the importance of EES and that the applied bias conditions have to be taken into account as well.

1. Introduction

The rapid miniaturization of MOSFETs has led to operating voltages scaled below 1 V. As a result, hot-carrier degradation has evolved from a mode where the damage is produced primarily by solitary hot carriers to a regime in which a substantial contribution is provided by colder carriers.[1–4] In the first case a bond rupture event can be triggered by a highly energetic carrier. However, due to a large disparity between the electron and proton masses a bond-breakage portion of energy is unlikely to be transferred in a direct collision.[5] Rather, a hot carrier can excite one of the bonding electrons to an antibonding (AB) state, thereby initiating the AB-mechanism.[6,7] If operating/stress voltages are low, this process is unlikely. In scaled devices the carrier flux can be very high with low average carrier energies. Therefore, several colder carriers which collide with the Si–H bond can substantially excite it, thereby triggering the multiple vibrational excitation (MVE) of the bond.[1–4] When the bond is settled on the last bonded state the hydrogen atom can overcome the potential barrier which separates this state and the transport mode, thus leaving a dangling Si-bond, which is electrically active. This bond-breakage mode is termed "MVE-mechanism".

At the device level, the interplay of these competing mechanisms results in a change of the worst-case conditions when one switches from high-voltage transistors to their scaled counterparts.[3,4,8,9] As a consequence, HCD appears to be highly sensitive to the way carriers are distributed over energy because high and low energetical particles can trigger different bond dissociation mechanisms. This information is contained in the carrier energy distribution function (DF), which is very sensitive to scattering mechanisms.[6,10,11] One of these mechanisms playing a crucial role in ultra-scaled devices is electron–electron scattering which populates the high-energy tails of the DF far beyond energies available from the potential drop between the source and the drain.[12,13] Moreover, Rauch et al., have reported that this mechanism is responsible for severe HCD enhancement in transistors starting from the 180 nm node and beyond.[14,15] Quite to the contrary, the group of Bravaix suggested that in their devices the role of EES is substantially overestimated and instead a two-particle mixed mode process drives hot-carrier degradation.[16] Using our recently developed physics-based HCD model[6,7] we investigate the importance of EES in the context of HCD in short- and long-channel transistors.

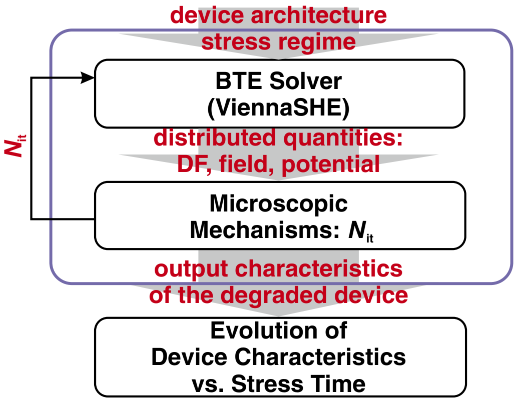

Fig. 1. (Color online) Our HCD model contains a carrier transport kernel, a module which describes the trap generation kinetics, and a degraded device characteristic simulator.

2. Modeling framework

Our approach covers and links three main aspects of HCD:[6,7,10] carrier transport, microscopic mechanisms of defect generation and modeling of the degraded devices (Fig. 1). The model is implemented into the deterministic Boltzmann transport equation solver ViennaSHE,[11,17,18] which is used for thorough carrier transport treatment. ViennaSHE simulates the carrier energy distribution functions in each point at the Si/insulator interface for a particular device structure and given operating/stress conditions. As the DF is very sensitive to the doping profiles, the MOSFET structures are obtained using the Sentaurus Process simulator calibrated and coupled to ViennaSHE to represent the characteristics of the fresh devices. Such important energy exchange mechanisms as surface scattering, scattering at ionized impurities, impact ionization as well as electron–

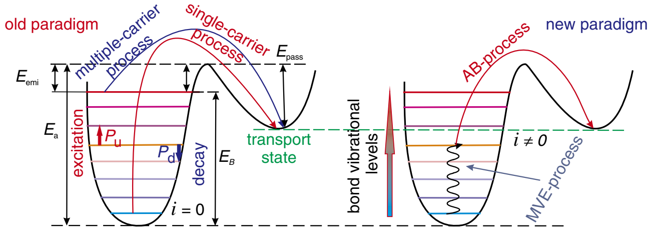

Fig. 2. (Color online) The sketch of the potential energy surface describing Si–H bond with a system of eigenstates in the potential well. Bond-breakage corresponds to hydrogen release from one of these bonded states to the transport mode. In the previous versions of our HCD model the single- and multiple-carrier processes of bond dissociation were assumed to be independent.[10,19] In the most recent version of the model these processes are considered self-consistently as competing pathways of the same bond-breakage reaction.[6,7]

phonon and electron–electron interactions are incorporated into ViennaSHE. The DFs are then used to calculate the carrier acceleration integral which is the key quantity in our model and describes the cumulative ability of the carrier packet to dissociate the bonds.[6,7,10] This quantity, hence, determines the rates of both AB- and MVE-mechanisms. As opposed to other approaches to HCD simulations,[2,15,20–28] our model incorporates all possible superpositions of these processes. In other words, first the bond can be excited by several colder carriers to an intermediate level (Fig. 2). The potential barrier which separates this level and the transport mode is now reduced. Thus, the bond-breakage portion of energy which needs to be transferred from a hot carrier to the bond is reduced as well, and hence the probability that the particle ensemble contains carriers with such an energy and above can be substantially high. Therefore, the bond can be dissociated by an AB-process triggered by a carrier with a substantially lower energy than the bond-breakage energy. Note that although the idea to consider all the possible combinations of the AB and MVE-processes was expressed previously by the Hess model,[2] in previous HCD models these mechanisms were considered independently for simplicity. Thus, in the previous version of our model the resulting interface state density was calculated as a superposition of AB- and MVE-induced contributions weighted with some probability coefficients.[10,19,29–31] In the most recent version of our model, however, the AB- and MVE-mechanisms are implemented self-consistently as competing pathways of the same reaction which converts pristine Si–H bonds into electrically active dangling Si bonds. We have already discussed that due to bond pre-heating by the MVE-process the potential barrier for hydrogen release is reduced when the bond is in an excited state. Another reason of the bond-breakage energy reduction is the interaction between the oxide electric field E_{ox} and the dipole moment of the bond d.[6,7,23,32] This reduction is modeled as a product $d \times E_{\text{ox}}$. An intimately related ingredient of the model stems from the structural disorder at the interface between crystalline Si and an amorphous dielectric. This disorder leads to statistical variations of the Si–H bonding energy which obeys a normal distribution with mean value and standard deviation equal to 1.5 and 0.15 eV, respectively.[33–35]

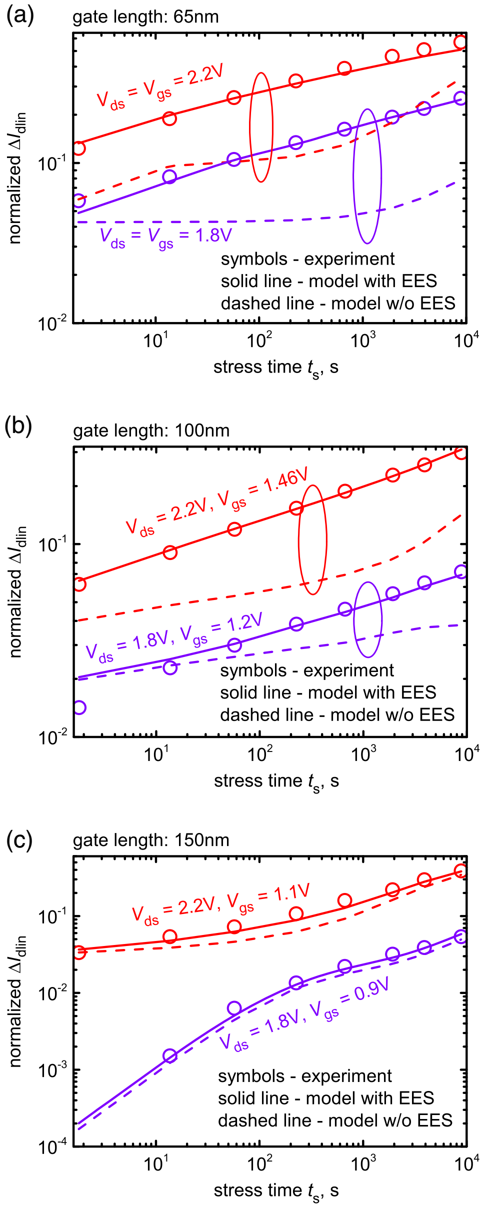

Fig. 3. (Color online) The normalized (i.e., divided by the drain current of the fresh device) linear drain current change $\Delta I_{\text{dlin}}(t)$ measured in three different nMOSFETs with gate lengths L_{G} of (a) 65, (b) 100, and (c) 150 nm. The devices were stressed at their corresponding HCD worst-case conditions at $V_{\text{ds}} = 1.8$ and 2.2 V. For comparison, we also plot $\Delta I_{\text{dlin}}(t)$ obtained without EES. In 65 and 100 nm transistors $\Delta I_{\text{dlin}}(t)$ is substantially underestimated if EES is ignored.

The model is capable of representing HCD in three different nMOSFETs with identical architecture (with a 2.5 nm SiON film) but with different gate lengths (65, 100, and 150 nm) stressed at different combinations of V_{ds} and V_{gs} for a period of 8 ks using a unique set of model parameters (see Fig. 3). Note that the devices have different dimensions, and thus worst-case conditions of HCD correspond to different combinations of V_{gs} and V_{ds}. For instance, the MOSFET with a gate length of 65 nm is considered to be a short-channel device and the worst-case scenario corresponds to $V_{\text{ds}} = V_{\text{gs}}$. The 150 nm transistor belongs to the long-channel devices, and therefore HCD is most severe when $V_{\text{gs}} = V_{\text{ds}}/2$. Also in this case the substrate current plotted as a function of V_{ds} and V_{gs} has a maximum at $V_{\text{gs}} = V_{\text{ds}}/2$. As for the 100 nm counterpart, the maximum substrate current was measured when $V_{\text{gs}} = 2/3\ V_{\text{ds}}$, and this device was

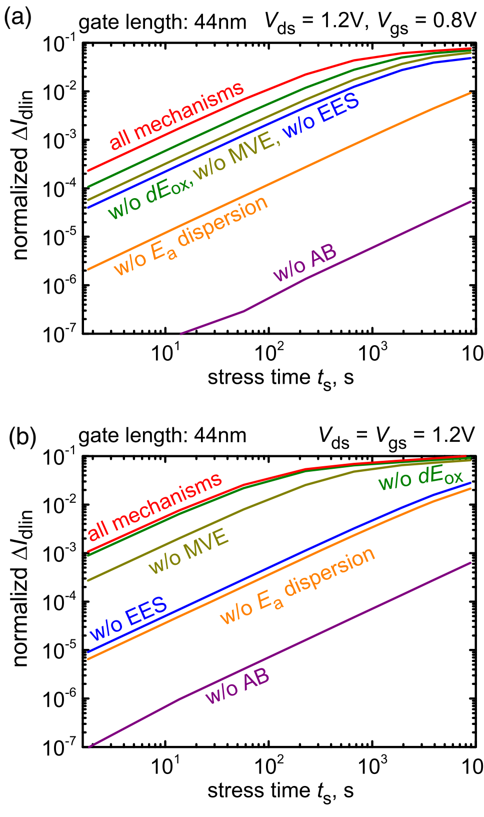

Fig. 4. (Color online) $\Delta I_{\mathrm{dlin}}(t)$ curves modeled in the nMOSFET with a gate length of 44 nm for (a) $V_{\mathrm{ds}} = 1.2$ V, $V_{\mathrm{gs}} = 0.8$ V and (b) $V_{\mathrm{ds}} = V_{\mathrm{gs}} = 1.2$ V considering and ignoring one of the model components, i.e., the AB- and MVE-mechanisms, EES, dipole-field interactions, and the bond-breakage energy dispersion.

subjected to hot-carrier stress using this interrelation between the voltages.

3. Results and discussion

Figure 3 summarizes the experimental change of the linear drain current ΔI_{dlin} as a function of time plotted vs the simulated $\Delta I_{\mathrm{dlin}}(t)$ curves. The $\Delta I_{\mathrm{dlin}}(t)$ data obtained neglecting EES fail to represent HCD in 65 and 100 nm devices for both combinations of voltages. Note that already in the case of the 100 nm MOSFET subjected to hot-carrier stress at lower voltages ($V_{\mathrm{gs}} = 1.2$ V, $V_{\mathrm{ds}} = 1.8$ V) the effect of EES is not so prominent. Furthermore, the discrepancy between $\Delta I_{\mathrm{dlin}}(t)$ curves simulated with and without EES increases with V_{ds}, V_{gs}. As for the MOSFET with a gate length of 150 nm the contribution of EES is weak and can be neglected.

It is important to emphasize that in previous paradigms of hot-carrier degradation only the channel/gate length was used to judge on the importance of EES for HCD.[14–16] Our findings suggest, however, that a superposition of the device geometry and applied voltages determines whether the effect of electron–electron scattering strong or not. In order to check this idea, a series of devices of similar architecture but with different gate lengths was virtually fabricated using Sentaurus process simulator. To cover a wide range of gate lengths we used MOSFETs with $L_{\mathrm{G}} = 44$, 200, and 300 nm.

Figure 4 presents the $\Delta I_{\mathrm{dlin}}(t)$ curves calculated with and without one of the model ingredients such as the AB- and MVE-mechanisms of bond dissociation, electron–electron scattering, interaction of the electric field with the dipole moment of the bond, and the dispersion of the bond rupture activation energy for the transistor with a gate length of 44 nm for two stress conditions, i.e., for $V_{\mathrm{ds}} = 1.2$ V, $V_{\mathrm{gs}} = 0.8$ V and $V_{\mathrm{ds}} = V_{\mathrm{gs}} = 1.2$ V. One can see that already at rather low voltages ignoring the EES mechanism leads to a severe underestimation of the linear drain current change for all stress times.

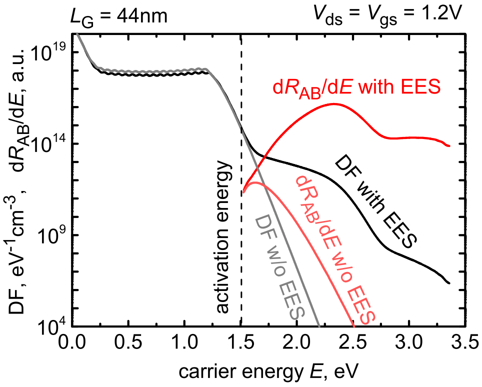

Fig. 5. (Color online) A schematic representation of the AB-process rate enhancement by EES for the case of the 44 nm device stressed at $V_{\mathrm{ds}} = V_{\mathrm{gs}} = 1.2$ V. A superposition of two competing functions, i.e., of the decaying with energy carrier DF and the increasing reaction cross section leads to a maximum of the integrand in Eq. (1). EES dramatically changes the DF shape by populating its high-energy tail. As a consequence, the derivative dR_{AB}/dE has a much more pronounced maximum, which in the case when EES is considered results in an AB-process rate several orders of magnitude higher than that obtained without EES.

Such a dramatic enhancement of HCD by the EES process can be explained by considering the functional structure of the expression which determines the AB-process rate:[6,7,25]

$$R_{\mathrm{AB}} = \int f(E)g(E)v(E)\sigma(E)\,dE, \tag{1}$$

where $f(E)g(E)$ is the carrier energy DF, $f(E)$ the occupation number, $g(E)$ the density-of-states, $v(E)$ the carrier group velocity, while $\sigma(E)$ is the Keldysh-like reaction cross section. The reaction cross section is determined as[2,6,7,22]

$$\sigma(E) = \begin{cases} \sigma_0(E - E_{\mathrm{th}})^{11} & \text{if } E \geq E_{\mathrm{th}} \\ 0 & \text{if } E < E_{\mathrm{th}} \end{cases}, \tag{2}$$

where E_{th} is the bond-breakage energy and σ_0 an attempt frequency. One can see that $\sigma(E)$ is a strongly increasing function of energy. The carrier DF simulated without EES has a plateau (due to a phonon cascade) followed by a thermal tail, i.e., in this section the DF values rapidly decrease with energy, Fig. 5. As a superposition of these two trends, the integrand in the expression for R_{AB} has a maximum at a certain energy (Fig. 5), see Refs. 25 and 26. If electron–electron scattering is considered, it leads to a hump visible in the DF at high energies, and thus to a maximum of $f(E)g(E)\sigma(E)$ which is observed at $E > E_{\mathrm{th}}$. This maximum is much higher than that related to R_{AB} evaluated without EES, and the bond-breakage rate in general is several orders of magnitude higher due to the EES process. Therefore, EES substantially populates the high energy fraction of the carrier ensemble, thereby making the AB-process dominant even at relatively low V_{ds} as 1.2 V, which is visible in Fig. 4.

It is worth to discuss also the effect of the interaction of the electric field with the dipole moment of the bond on the

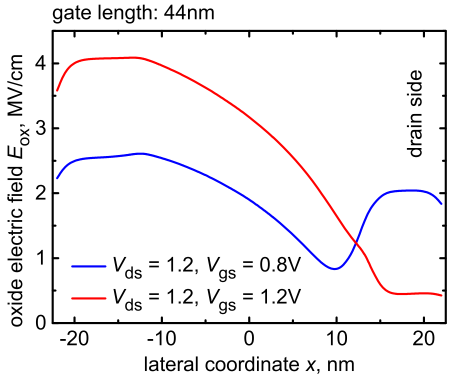

Fig. 6. (Color online) The dielectric electric field profiles at the SiON/Si interface simulated for the 44 nm device for $V_{ds} = 1.2$ V, $V_{gs} = 0.8$ V and $V_{ds} = V_{gs} = 1.2$ V.

$\Delta I_{dlin}(t)$ curves. This effect is stronger at $V_{ds} = 1.2$ V and $V_{gs} = 0.8$ V as compared to the case with $V_{ds} = V_{gs} = 1.2$ V. At a first glance, such a finding appears to contradict to our recent results, see Refs. 6 and 7. To understand this behavior we plot the electric field profiles at the SiON/Si interface for both combinations of V_{ds} and V_{gs} (Fig. 6) as well as the interface state density N_{it} as a function of the lateral coordinate x for two stress time steps of 14 and 700 s with and without the $d \times E_{ox}$ effect (Fig. 7). In the case of $V_{gs} = 0.8$ V the electric field is lower at the source side of the device and higher in the drain MOSFET area, as compared to that evaluated for $V_{gs} = 1.2$ V. As a result, the effect of the $d \times E_{ox}$ contribution has a stronger impact on the drain N_{it} peak (visible at $x \gtrsim 15$ nm) and has much less effect on the N_{it} values near the source when $V_{gs} = 0.8$ V. However, at these stress conditions and within the used stress time window, the I_{dlin} degradation is primarily determined by the drain N_{it} because the source and channel interface traps have a low density N_{it} and do not significantly disturb the transistor performance. Hence, the effect of the field-dipole interaction is stronger for $V_{gs} = 0.8$ V. Note finally that the source/channel interface states are responsible for HCD at longer stress times, see Refs. 6 and 7.

Further, in the case of longer devices, instead of calculating the linear drain current change with all the model ingredients and the same curves ignoring one of these ingredients (as it was in Fig. 3), we analyze relative contributions of different model components into $\Delta I_{dlin}(t)$. In other words, we reformulate the problem in terms of the ratio between $\Delta I_{dlin}(t)$ evaluated neglecting one of these components and that obtained with the "full" model.

Figure 8 presents these ratios plotted for the transistors with gate lengths of 200 and 300 nm stressed at the worst-case conditions of hot-carrier degradation for long-channel MOSFETs, i.e., at $V_{gs} = V_{ds}/2$ at three different values of V_{ds}, namely at 1.8, 2,2, and 2.8 V. If the $\{V_{ds}, V_{gs}\}$ values are fixed and the ratio obtained for two different channel lengths are compared, one can see that the effect of EES is more prominent in the shorter device. The contribution of electron–electron scattering also appears to be stronger when a gate length is fixed while the $\{V_{ds}, V_{gs}\}$ values increase. It is important to emphasize that even in such a long device as the 300 nm MOSFET the role of EES is substantial already at $V_{ds} = 2.2$ V and $V_{gs} = 1.1$ V, while at $V_{ds} = 2.8$ V and $V_{gs} = 1.4$ V the ΔI_{dlin} value can be underestimated by ~30%. As for the 200 nm transistor such an underestimation corresponds to substantially lower voltages, i.e., to $V_{ds} = 2.2$ V and $V_{gs} = 1.1$ V. Note also that in the case of $V_{ds} = 1.8$ V and $V_{gs} = 0.9$ V the contribution of electron–electron scattering can be neglected for all stress times and for both devices. Therefore, we conclude that the role of EES depends not exclusively on the gate length but also on the applied voltages, and this process can be negligible or crucial in the same long-channel MOSFET stressed using different $\{V_{ds}, V_{gs}\}$.

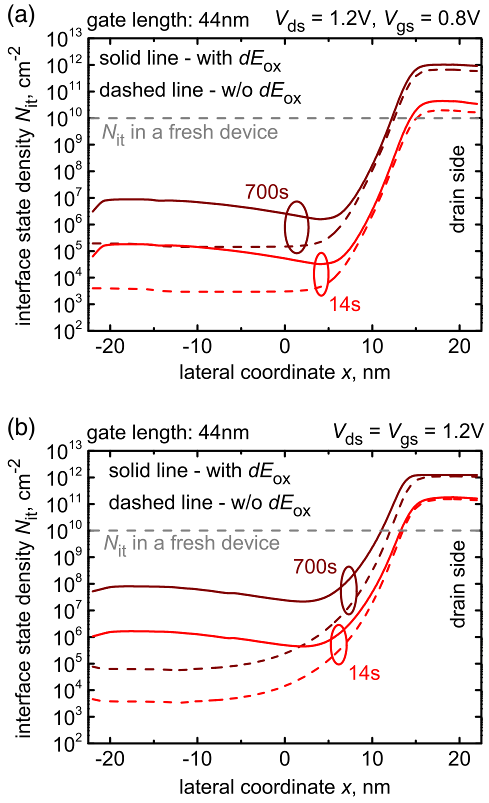

Fig. 7. (Color online) The interface state density $N_{it}(x)$ profiles simulated for the 44 nm device with and without the interaction of the electric field with the dipole moment of the bond for two combinations of stress voltages: (a) $V_{ds} = 1.2$ V, $V_{gs} = 0.8$ V and (b) $V_{ds} = V_{gs} = 1.2$ V. The curves for two stress time steps of 14 and 700 s are shown. As a reference we also indicate the N_{it} value typical for unstressed devices of ~10^{10} cm^{-2}. Those interface traps which are characterized with an interface state density below this value do not significantly contribute to the device performance degradation.

These trends are supported by Fig. 9 which shows the electron energy distribution functions calculated for the 200 and 300 nm devices. The left plot of Fig. 9 demonstrates that the DFs shift in the whole energy range when the applied voltages increase. For instance, high-energy tails appear to be more populated at higher $\{V_{ds}, V_{gs}\}$. These high-energy tails are formed primarily by the electron–electron scattering mechanism (and disappear if EES is switched off), which results in the DF humps pronounced at high energies (see Fig. 9). Thus, the EES role is enforced if the applied bias becomes higher.

The effect of the gate length on the contribution of the EES process is also evident: DFs calculated for the same combination of $\{V_{ds}, V_{gs}\}$ but for a longer device are characterized by lower values. Such a trend can be explained in the following manner. The high-energy tail of the carrier

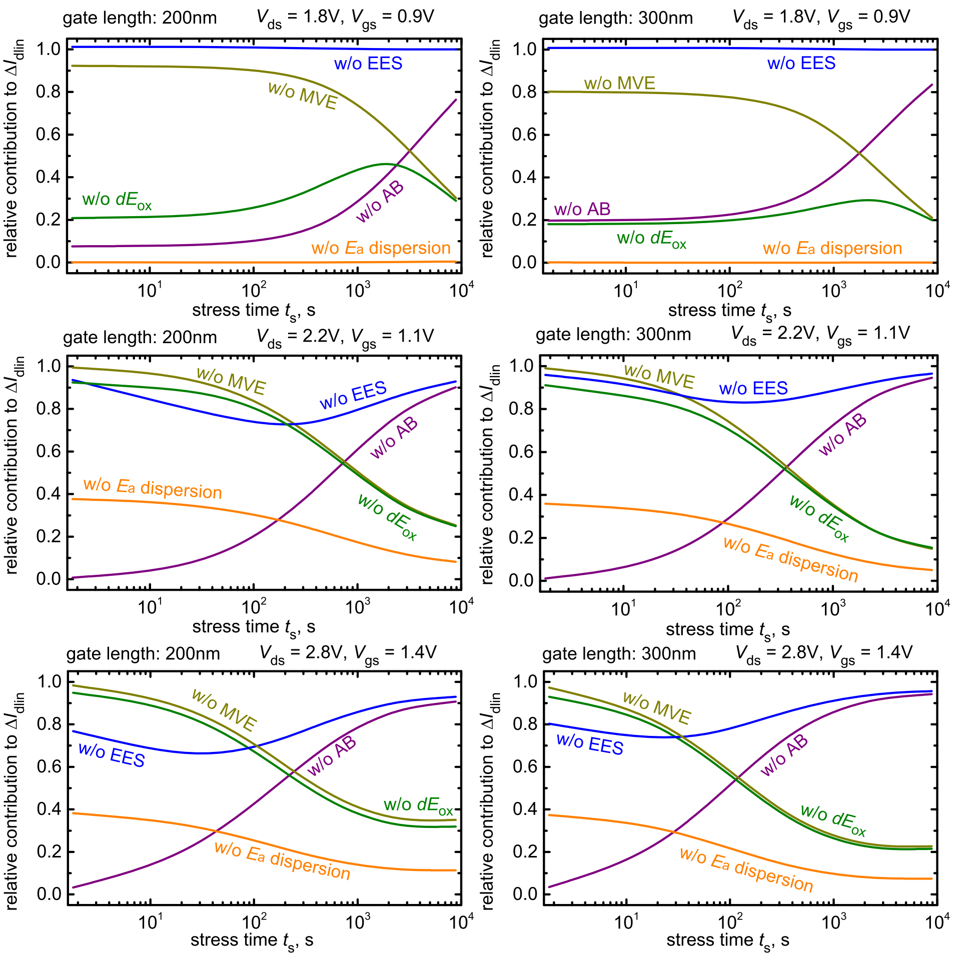

Fig. 8. (Color online) The ratio between $\Delta I_{dlin}(t)$ simulated neglecting one of the model components and that obtained with the full model. These ratios were calculated for two MOSFETs with gate lengths of 200 and 300 nm for the interrelations between V_{ds} and V_{gs} corresponding to the worst-case HCD conditions in long-channel transistors.

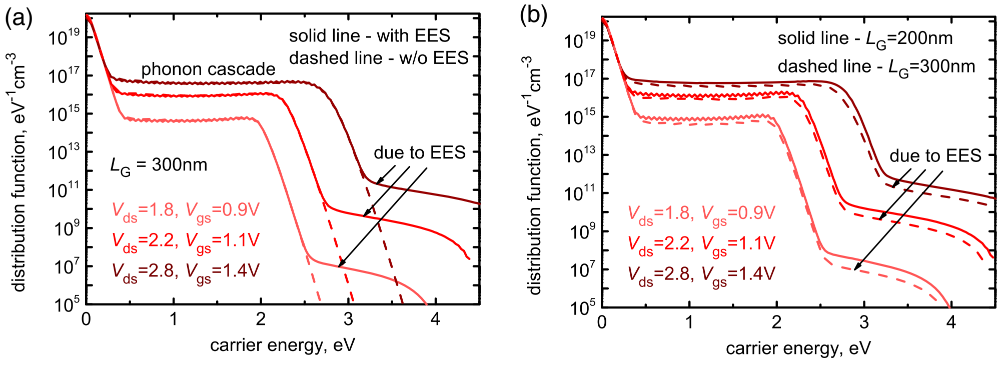

Fig. 9. (Color online) (a) Comparison of the carrier energy distribution functions simulated with and without EES for the 300 nm MOSFET near the drain. (b) Comparison of carrier DFs obtained for 200 and 300 nm MOSFETs near the drain for the same combinations of voltages. All the DFs are plotted for the same values of $\{V_{ds}, V_{gs}\}$, namely for $V_{gs} = 0.9$ V, $V_{ds} = 1.8$ V, $V_{gs} = 1.1$ V, $V_{ds} = 2.2$ V, and $V_{gs} = 1.4$ V, $V_{ds} = 2.8$ V.

DF is formed by the balance between scattering-out (electron–phonon interactions) and scattering-in (electron–electron interactions).[13,36] The phonon scattering rate is a weak function of energy, and thus the tail level of the DF is determined by the EES rate, see Ref. 37. In longer MOSFETs scattering-out is more efficient, and hence the balance between electron–phonon and electron–electron interactions is achieved at a higher value of the EES rate. This rate is energy dependent, and thus the onset of the typical hump formed by EES (pronounced in high-energy tails of the DFs) occurs at higher energies in longer devices, and thus the EES contribution to HCD is weaker. It is also worth to note that since two electrons are involved into EES the corresponding rate is proportional to the squared carrier concentration, which is also lower in longer devices.

Figure 8 also allows to analyze the role of other model ingredients. For instance, one concludes that the MVE-mechanism is important in both 200 and 300 nm MOSFETs stressed at all combinations of V_{ds} and V_{gs}. This result agrees with our previous finding[10,19,29] as well as with the results published by the Bravaix group,[38] where it was demonstrated that the MVE-mechanism can provide a substantial contribution even if a gate length as long as 2.0 µm. As for the AB-process, this mechanism provides the dominant contribution to hot-carrier degradation. This is consistent with the current HCD paradigm that in long-channel devices and/or at high stress voltages the hot-carrier damage is dominated by the single-carrier mechanism.[3,26] Note also that the sum of the relative contributions to ΔI_{dlin} simulated neglecting one of the AB-/MVE-mechanisms is not necessary equal to 1 (see Fig. 8). This is because these two bond-breakage modes are coupled, i.e., their rates cannot be considered independently. Such a situation corresponds to the bond rupture scenario when the multiple vibrational excitation of the bond heats this bond and then the single-carrier process induces hydrogen release. Therefore, the multiple-carrier excitation substantially increases the rate of the AB-mechanism. As a result, if the MVE-mode is ignored, the rate of the single-carrier process is also underestimated. In this case the sum of the corresponding contributions exceeds 1.

If the bond-breakage energy dispersion is omitted this leads to a substantial underestimation of ΔI_{dlin}. This tendency, however, becomes less pronounced if the stress voltages increase. This is because at high $\{V_{ds}, V_{gs}\}$ carriers are rather hot, thereby efficiently triggering a bond dissociation event. As a result, further reduction of the activation energy does not substantially affect the bond-breakage rates. The same is typical also for the energy reduction due to the interaction of the oxide electric field with the dipole moment of the bond, i.e., the $d \times E_{ox}$ contribution has a weaker impact on the bond dissociation kinetics at higher stress voltages.

4. Conclusions

Using our physics-based model for hot-carrier degradation we have analyzed the importance of electron–electron scattering in the context of HCD. For this purpose, MOSFETs of an identical geometry but with different gate lengths have been used. The gate length varied in a wide range. i.e., from 44 to 300 nm. We have demonstrated that even in the 300 nm MOSFET the contribution of electron–electron scattering can be substantial if the applied voltages are high enough. Thus, the linear drain current change calculated ignoring EES will be underestimated by more than 15% at $V_{ds} = 2.2$ V and $V_{ds} = 1.1$ V and by ~30% at $V_{ds} = 2.8$ V and $V_{ds} = 1.4$ V. As for the shortest transistor with a gate length of 44 nm, the effect of EES is important already at $V_{ds} = 1.2$ V and $V_{gs} = 0.8$ V. Therefore, the importance of EES is defined by both the device topology and the applied stress/operating voltages, i.e., not exclusively by the gate/channel length as in previous HCD paradigms.

Acknowledgments

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