Dominant Mechanisms of Hot-Carrier Degradation in Short- and Long-Channel Transistors

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***Abstract*—Using our physics-based model for hot-carrier degradation (HCD) we analyze the role of such important processes as the Si-H bond-breakage induced by a solitary hot carrier, bond dissociation triggered by the miltivibrational excitation of the bond, and electron-electron scattering. To check the roles of these mechanisms we use planar CMOS devices with gate lengths varying between 65 and 300 nm as well as a high-voltage nLDMOS transistor. We show that the current HCD paradigm needs to be revised because the aforementioned processes can be crucial even under stress conditions at which they are supposed to be weak.**

I. Introduction

It is commonly assumed that in scaled devices hot-carrier degradation is driven by the multiple-carrier process [1–3]. The argument is that in these devices the operating/stress voltages are low, and thus carriers with energies above the threshold for triggering a single-carrier bond-breakage even of ∼1.5 eV [4, 5] are unlikely. Thus, in scaled devices the only probable way to dissociate the Si-H bond is by the multiple vibrational excitation (MVE) of this bond [6–8], i.e. by the MVE-process. According to this scenario, dissociation is triggered by a series of carriers with relatively low energies which subsequently bombard the bond, thereby heating it. When the bond is situated in an excited state the bond-breakage energy is reduced and electrons with much lower energies then 1.5 eV can induce hydrogen release from a bonded state to the transport mode. Since in modern MOSFETs the operating voltages are scaled below 1.5 V the particles in the ensemble are predominately cold and the MVE process is suggested to be dominant.

In our recent works [9, 10], however, we have shown that even in nano-scale devices Si-H bond-breakage can be efficiently triggered by a solitary hot carrier. The situation is made even more complicated because it was independently shown by the Bravaix group as well as in our recent findings that the MVE-process is an essential contributor to HCD also in long-channel devices with a gate length as long as 2 μm subjected to hot-carrier stress at drain voltages of up to V_{ds} = 7.25 V [11–13].

Another important mechanism which is claimed to be responsible for HCD enhancement in scaled MOSFETs is electron-electron scattering (EES) [3, 9, 10, 14, 15]. This process was shown to populate the carrier ensemble fraction which is characterized by energies higher than that obtained by the electric field [16, 17]. As a result, EES substantially enforces hot-carrier degradation in the devices fabricated according to the 180 nm process node and in shorter counterparts [14, 15]. This enhancement is due to the hot carriers generated by the EES process which can contribute to both single- and multiple-carrier mechanisms of bond dissociation. However, the group of Bravaix has expressed the idea that the role of EES is dramatically overestimated and instead a two-particle mixed mode process is responsible for HCD in short-channel MOSFETs [18].

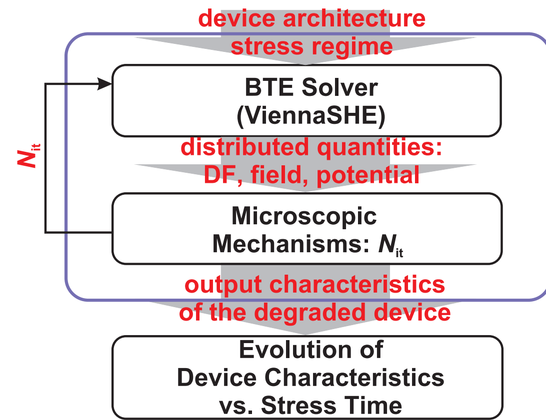

Fig. 1. The structure of our HCD model. The deterministic Boltzmann transport equation solver computes the carrier energy distribution functions for a particular device geometry and applied voltages. These distribution functions are then used to calculate the rate of the bond dissociation reaction and then obtain the interface state density as a function of time and the lateral coordinate along the interface. This interface state density table is then used to evaluate the linear drain current change for each stress time step.

We apply our physics-based HCD model to analyze the limits of importance of such mechanisms as EES and single- /multiple-carrier processes of bond dissociation. For this, we employ CMOS MOSFETs with gate lengths varying from 65 to 300 nm as well as an nLDMOS transistor with a length of the Si/SiO_2 interface of ∼ 2.5 μm.

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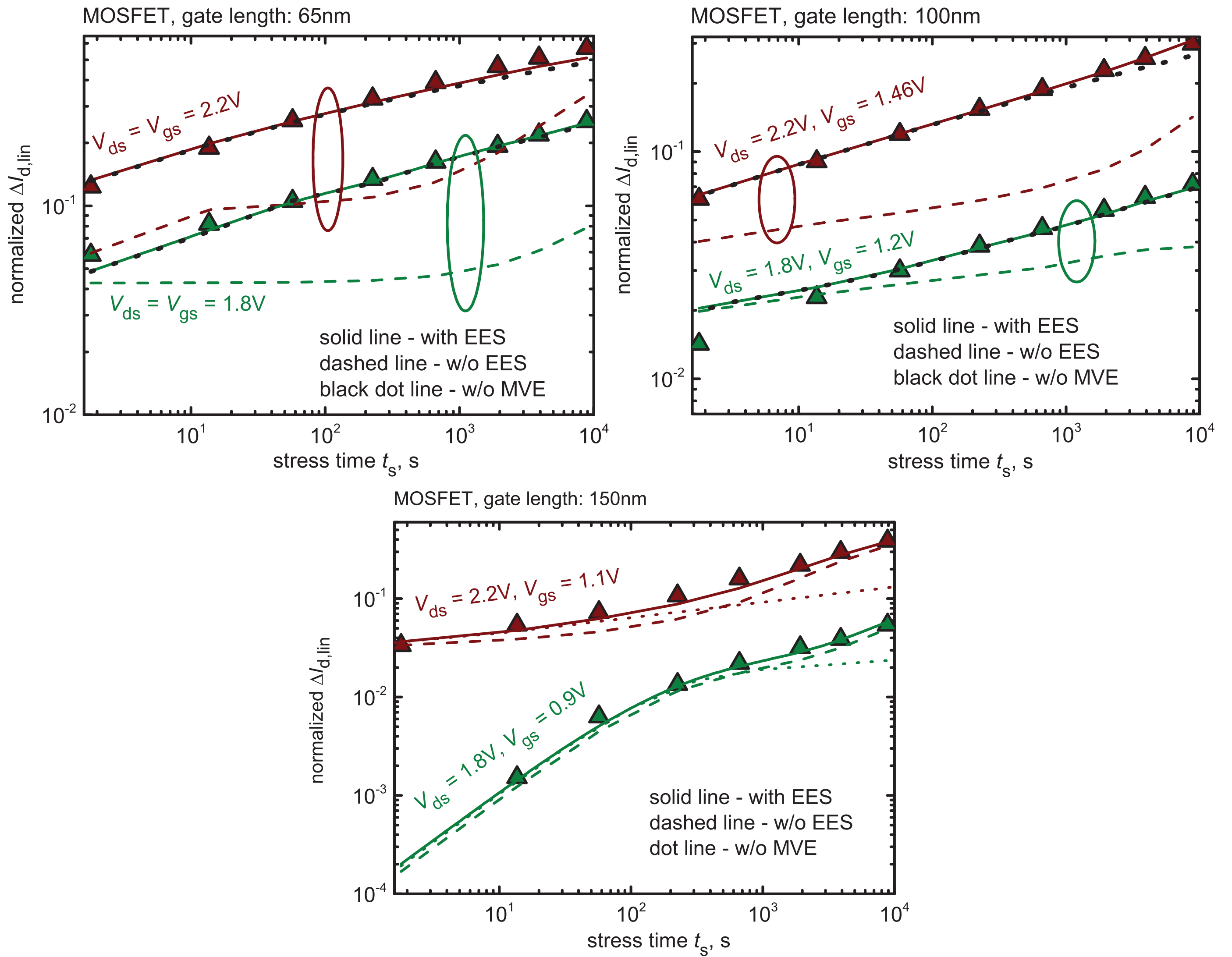

Fig. 2. The normalized change of the linear drain current $\Delta I_{\mathrm{dlin}}(t)$ as a function of stress time: experiment (symbols) vs. simulations (lines). The $\Delta I_{\mathrm{dlin}}(t)$ data were obtained in n-MOSFETs with gate lengths of 65, 100, and 150 nm stressed under various combinations of V_{ds}, V_{gs}. To analyze the importance of EES we have also plotted $\Delta I_{\mathrm{dlin}}(t)$ curves obtained neglecting EES and the MVE-mechanism.

II. Simulation Framework:

Our HCD model covers and links three main aspects of hot-carrier degradation: carrier transport, modeling of defect generation kinetics, and the simulation of the degraded devices [9, 10]. For proper carrier transport treatment we use the deterministic Boltzmann transport equation solver ViennaSHE, which is employed to simulate the carrier energy distribution functions (DFs) for a certain device structure and applied voltages. Obtained DFs are then used to evaluate the carrier acceleration integral, which describes the cumulative ability of the carrier ensemble to dissociate the bonds, and thus determines the rates of both bond rupture mechanisms [9–11]. A solitary highly energetic carrier can trigger a bond dissociation event in a single collision by exciting one of the bonding electrons to an antibonding (AB) state, and thus this process is called the AB-mechanism. If the carrier ensemble does not contain a substantial number of these hot carriers, bond-breakage is triggered by several colder carriers, which induce the MVE-process terminated by hydrogen release. We consider all possible combinations of the AB- and MVE-mechanisms self-consistently. In other words, first the bond can be excited to an intermediate state by a series of carriers with low energies and then dissociated by a solitary hotter carrier. Note that in this case a hot carrier needs to transfer an energy lower than the dissociation energy of the bond in its ground state [10, 11].

The potential barrier which separates the bonded state and the transport mode can also be reduced by the interaction of the electric field E_{ox} with the dipole moment d. The corresponding reduction of the bond-breakage energy is modeled as $d \times E_{\mathrm{ox}}$ [19, 20]. Additionally, the activation energy of bond dissociation E_{a} varies stochastically due to the structural disorder at the Si/insulator interface. As a result, in the model we assume that E_{a} obeys a Gaussian distribution

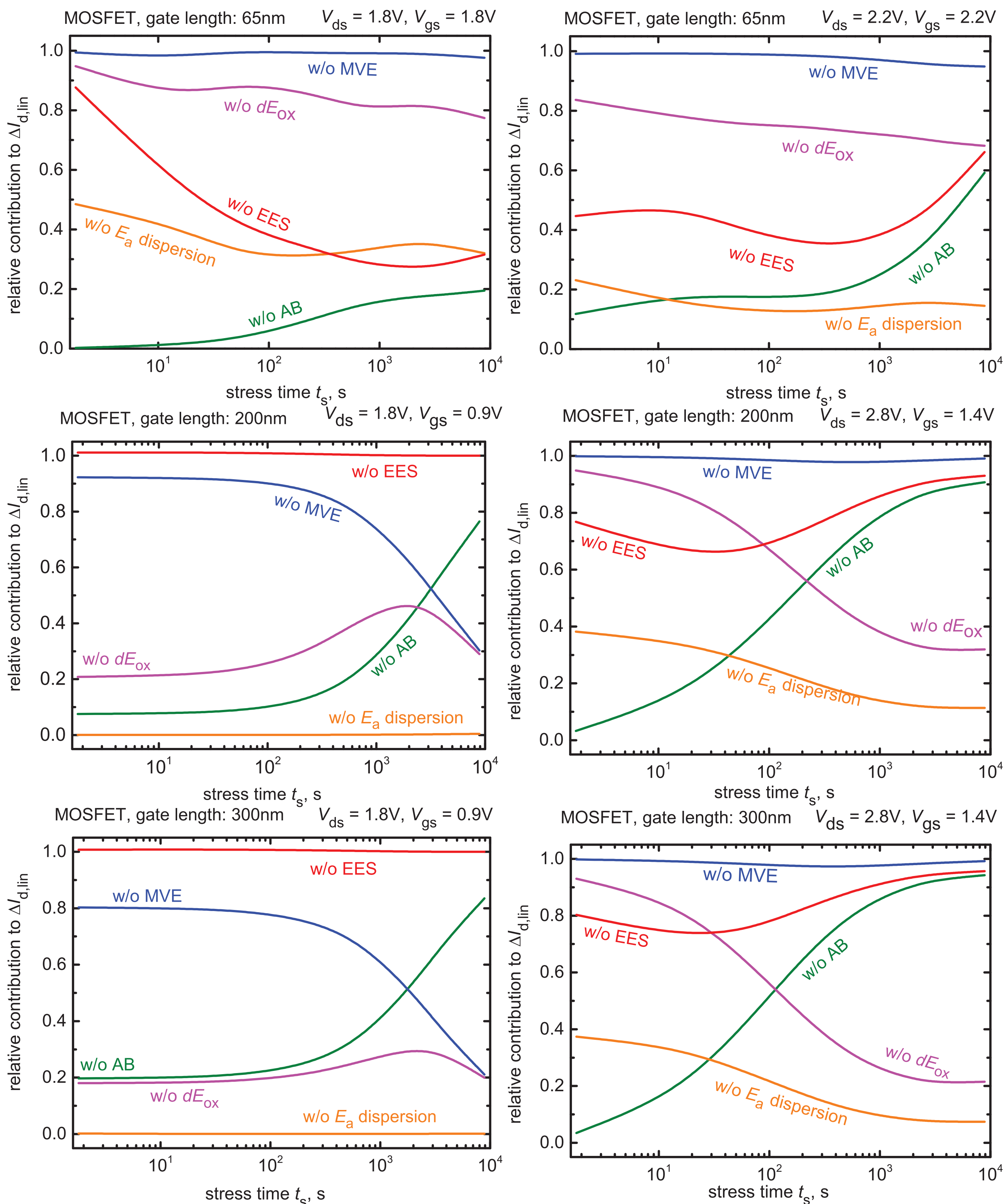

Fig. 3. The ratio between the linear drain current change calculated disregarding one of the model components to that obtained with the full HCD model for CMOS MOSFETs with three different gate lengths: 65, 200, and 300 nm. The calculations are carried out for two different values of V_{ds} = 1.8, 2.2 V while V_{gs} were chosen corresponding to the worst-case conditions of HCD typical for these transistors.

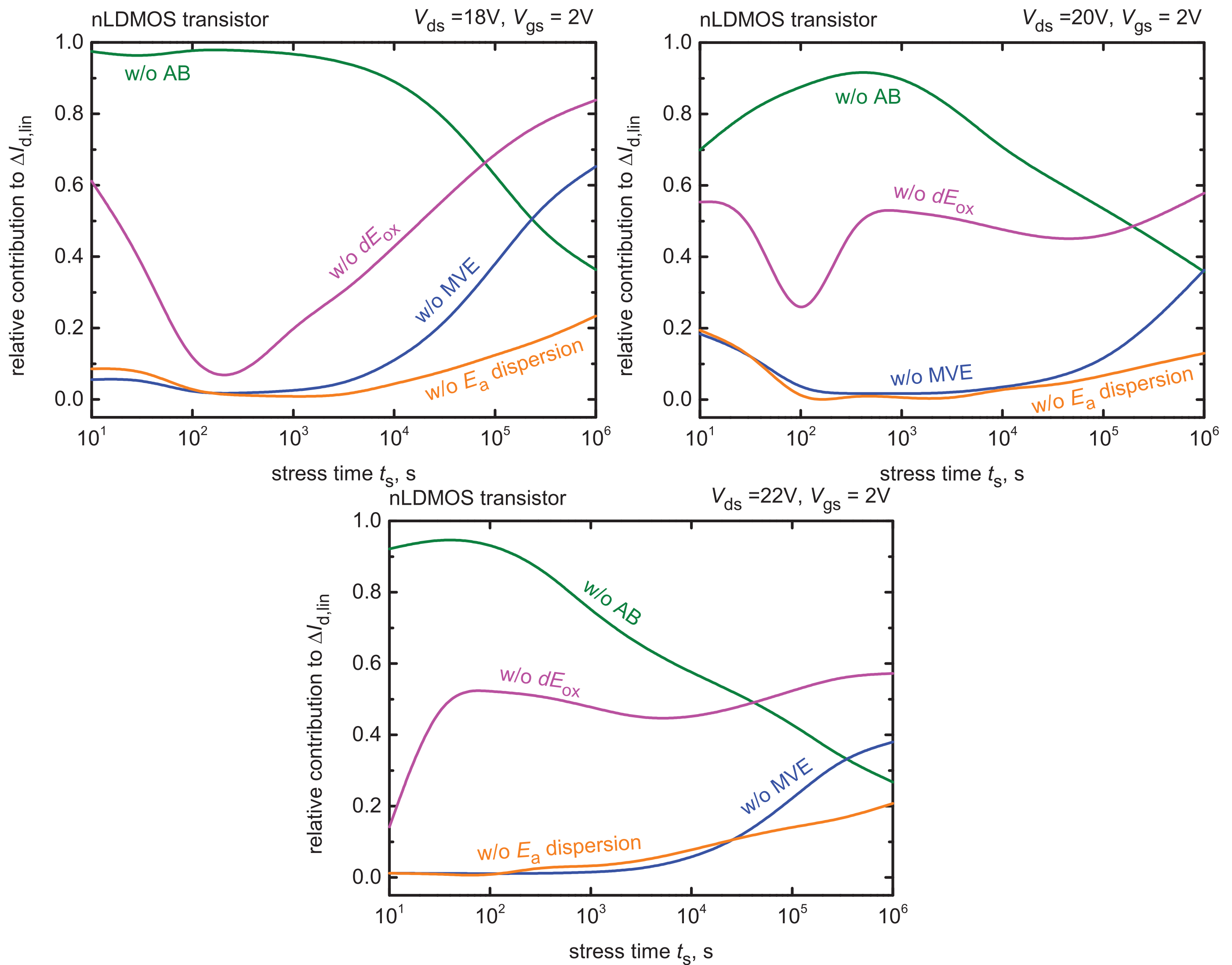

Fig. 4. The same as in Fig. 3 but calculated for the nLDMOS stressed under the fixed gate voltage of V_{gs} = 2 V and three different values of V_{ds} = 18, 20, and 22 V.

with the mean value and the standard deviation equal to 1.5 eV and 0.15 eV correspondingly. These values are in good agreement with the experimentally observed ones [5, 21]. All these ingredients are consolidated in the latest model [9, 10]. The model was calibrated in a fashion to represent the linear drain current degradation $\Delta I_{\mathrm{dlin}}(t)$ measured in nMOSFETs of a similar topology and with different gate lengths (65, 100, and 150 nm) which were subjected to hot-carrier stress using different voltages, see Fig. 2. Note that two values of the drain voltage V_{ds} were used, namely 1.8 and 2.2 V. The gate voltage V_{gs} was adjusted to satisfy the worst-case conditions of hot-carrier degradation for each particular device. Fig. 2 shows quite good agreement between the experimental and simulated data. It is worth to emphasize that our simulation approach uses a unique set of the parameters for modeling of HCD in different devices stressed under different V_{ds}, V_{gs}.

III. Results and Discussion:

To study the effect of EES on HCD we have also evaluated the $\Delta I_{\mathrm{dlin}}(t)$ curves neglecting electron-electron scattering, Fig. 2. One can see that if EES is ignored, $\Delta I_{\mathrm{dlin}}(t)$ is massively underestimated for the case of the 65 nm MOSFET for both device stress conditions and in the 100 nm transistor subjected to HCD at V_{gs} = 1.1 V and V_{ds} = 2.2 V. At the same time, the EES effect on HCD is weak in the longest MOSFET at both combinations of V_{gs} and V_{ds}. Note that in the 100 nm transistor the impact of EES is pronounced at high stress voltages (V_{ds} = 2.2 V) but much weaker when the drain voltage is lower (V_{ds} = 1.8 V). More intriguingly, the contribution of the MVE-process is very weak or even negligible in 65 and 100 nm MOSFETs. At a first glance, this finding contradicts the idea that in scaled devices HCD is dominated by the MVE-mechanism. This behavior suggests that rather than the device length exclusively a superposition of the transistor geometry and applied voltages needs to be considered.

To analyze the importance of the EES effect on HCD, the $\Delta I_{\mathrm{dlin}}(t)$ curves have also been modeled for the MOSFETs with gate lengths of 200 and 300 nm fabricated in the same architecture. These devices were "virtually grown" using the Sentaurus process simulator [22] and a quite similar process flow as for those MOSFETs which were used for the model validation and the data presented in Fig. 2.

Fig. 3 summarizes the ratios between the $\Delta I_{\mathrm{dlin}}(t)$ values calculated neglecting one of the model components (AB- and MVE-mechanisms, EES, $d \times E_{\mathrm{ox}}$ activation energy reduction, and its dispersion) to those computed with the "full" model. The curves are obtained for 65, 200, and 300 nm devices for two different values of V_{ds} = 1.8 and 2.2 V. The gate voltages were chosen according to the worst-case conditions of HCD, i.e. $V_{\mathrm{gs}} = V_{\mathrm{ds}}$ for the 65 nm device and $V_{\mathrm{gs}} = V_{\mathrm{ds}}/2$ for 200 and 300 nm counterparts [23, 24]. One can see that the role of EES can also be substantial even in the 300 nm MOSFET if the applied V_{ds} is high (higher than 2.2 V). For instance, in the case of the 200 nm transistor subjected to hot-carrier stress at V_{ds} = 2.8 V and V_{gs} = 1.8 V the ΔI_{dlin} change calculated without the EES effect is underestimated by more than 25% for stress times within the interval of 10-100 s. As for the device with a gate length of 300 nm stressed at the same voltages the discrepancy is a bit less, i.e. ∼20%, but is still substantial. Therefore, one concludes that the role of electron-electron scattering increases with the gate length.

Another important Si-H bond-breakage mechanism is the MVE-process which is suggested to be responsible for HCD in short-channel devices [1, 2, 8]. The contribution of the MVE-process can be important at long stress times in 200 and 300 nm MOSFETs if they are stressed at V_{ds} = 1.8 V being rather weak at V_{ds} = 2.8 V, see Fig. 3. This is because under high V_{ds}, V_{gs} voltages HCD is driven primarily by the single-carrier mechanism. Due to the same reason, the role of the energy reduction by the interaction of the electric field with the dipole moment of the bond is less important under higher voltages. In fact, if V_{ds} is high enough carriers are rather hot, hence can efficiently trigger bond dissociation events, and this process is not very sensitive to an activation energy reduction. If the $\{V_{\mathrm{ds}}, V_{\mathrm{gs}}\}$ pair is fixed and we analyze the role of the AB-mechanism in devices with different gate lengths, the AB-process contribution becomes less pronounced in longer devices. As a result, the relative role of the $d \times E_{\mathrm{ox}}$ reduction tends to increase. The same behavior is typical to the effect of the activation energy dispersion. Another important conclusion which can be drawn from Fig. 3 is that the AB-mechanism can be dominant also in the scaled devices if the drain voltages are high enough.

Recently we have applied our hot-carrier degradation model to represent the linear drain current change in an nLDMOS transistor [25]. Fig. 4 shows the same ratios as Fig. 3 but plotted for the nLDMOS device stressed at a fixed V_{gs} = 2 V and three different V_{ds} = 18, 20, 22 V. Due to the complex structure of the nLDMOS transistor and additional computational costs related to EES we neglect this mechanism. One can see that although the drain voltage is high, under all combinations of the stress voltages $\{V_{\mathrm{ds}}, V_{\mathrm{gs}}\}$, the MVE-process still plays an important role, especially at short stress times. As we demonstrate in [25], this is because the interface state density peak located in the transistor channel is formed by the contribution of the MVE-mechanism and this peak determines short-term HCD. This result is consistent with our previous findings where we showed that the MVE-process is important in the context of HCD in MOSFETs with channel lengths up to 2 μm stressed at $V_{\mathrm{ds}} \geqslant 6$ V [11, 12]. The same findings were independently published by the group of Bravaix [13].

IV. Conclusion

We have demonstrated that even in long-channel transistors with a channel length of 300 nm electron-electron scattering can play a significant role. For instance, ignoring EES while modeling HCD in 200 and 300 nm MOSFETs stressed at V_{ds} = 2.8 V and V_{gs} = 1.4 V leads to ΔI_{dlin} underestimation of more than 25% and ∼ 20%, respectively. As opposed to the previous HCD understandings, the contribution of the MVE-process can be pronounced also in long-channel CMOS transistors as well as in high-voltage nLDMOS devices subjected to hot-carrier stress at $V_{\mathrm{ds}} \geq 18$ V. Further, the AB-process was shown to be important even in deep submicron MOSFETs with a gate length of 65 nm subjected to high voltages, i.e. to $V_{\mathrm{ds}} = V_{\mathrm{gs}}$ = 1.8 V, while in this situation the MVE-process makes only a small contribution to the damage. Our analysis shows that the prevalent hot-carrier degradation paradigm, which suggests that HCD in long-channel devices is controlled by the multiple-carrier process and that HCD is dominated by the multiple-carrier mechanism in scaled MOSFETs, needs to be revised. The importance of each of these mechanisms is determined by the superposition of the device geometry and applied voltages, not exclusively by one of these factors.

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