3D Coupled Electro-Thermal FinFET Simulations Including the Fin Shape Dependence of the Thermal Conductivity

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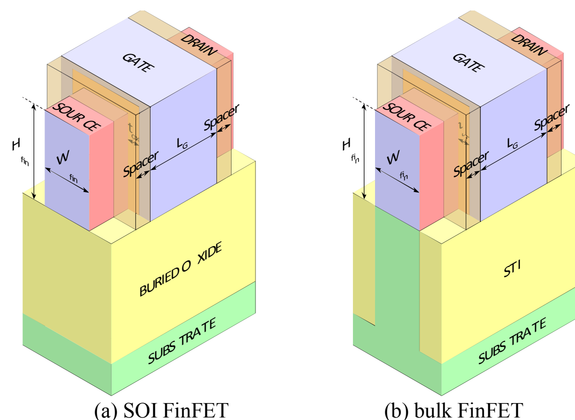
***Abstract*— A thermal simulation module, based on the solution of the coupled Heat Flow, Poisson, and Current Continuity Equations, has been developed and implemented in the 'atomistic' simulator GARAND to investigate the impact of self heating on FinFET DC operation. A progressive study of coupled electro-thermal simulation for FinFETs is presented. A new approximate formula for the reduced thermal conductivity due to phonon-boundary scattering in the fin is presented which considers both the fin height and the fin width, and is both position and temperature dependent. Simulation results for a SOI FinFET and a bulk FinFET example are compared and analysed.**

Keywords—FinFET; thermal effects; self-heating effects; thermal conductivity

I. INTRODUCTION

With the continuous scaling of semiconductor devices into the nanometer regime, the thermal density inside transistors is increasing and self-heating effects have become a crucial issue [1-3]. Now that the traditional planar MOSFET is approaching the end of its useful life, novel architectures such as FinFETs and fully depleted (FD) SOI transistors, have been introduced in order to enable technology scaling at the 22nm CMOS technology generation and beyond. Because of the 3D architecture of the FinFET (schematics of SOI and bulk FinFETs are shown in Fig. 1), thermal reliability imposes greater challenges, therefore analyzing and modeling self-heating in FinFETs has attracted significant interest [4-5].

In this paper, we present a study of coupled electro-thermal simulation for FinFETs. In section II, the model and formulae of the coupled electron-thermal simulation, including the new approximate formula for the calculation of the thermal conductivity in the fin region, are presented. In Section III, the simulation results for two FinFET structures – a SOI FinFET and a bulk FinFET – are analysed, investigating the lattice temperature profile and the corresponding Id-Vg characteristics. The cases without and with external thermal resistances were considered, and the effect of the much lower thermal conductivity of the fin due to phonon-boundary scattering with the use of the new approximate formula is taken into account.



(a) SOI FinFET (b) bulk FinFET

Fig. 1. Schematics of SOI and bulk FinFETs.

II. COUPLED ELECTRO-THERMAL SIMULATION

Within the framework of the GSS statistical-variability-aware device simulator GARAND [6], we have developed a thermal simulation module to investigate the impact of self heating on FinFET DC operation. This module is based on the solution of the coupled Heat Flow, Poisson, and Current Continuity Equations.

The heat flow equation, which assumes the electrons and holes are in thermal equilibrium with the host lattice, is:

$$\rho c \frac{\partial T_L}{\partial t} = H + \nabla(\kappa \nabla T_L) \quad (1)$$

where T_L is the temperature of the lattice, ρ is the mass density, c is the specific heat of the material, κ is the thermal conductivity, and H is the heat generation term. If Joule heat is considered, the heat generation term can be written as:

$$H = J_n \cdot E_n + H_U \quad (2)$$

where J_n is the electron current densities, E_n is the electric field, H_U is the lattice heating due to carrier recombination/generation. Here we focus on the self-consistent solution of the steady-state (i.e. not time-dependent) heat-flow equation.

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The current densities under the influence of temperature gradient are:

$$J_n = qn\mu_n E_n + k\mu_n T_L \nabla n + +k\mu_n n \nabla T_L \quad (3)$$

where n is the electron density, μ_n is the electron mobility, k is Boltzmann constant.

The unipolar current continuity equation is:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot J_n - U_n \quad (4)$$

where U_n is the net electron recombination rate. In Eq.(2)~(4), only electrons are currently considered and equations for holes can be formulated in a similar way..

Poisson's equation is:

$$\nabla \cdot \varepsilon \nabla(\psi - \theta) = -q(p - n + N_D^+ - N_A^-) \quad (5)$$

accounting for the case when the lattice temperature is not spatially constant. Here N_D^+ and N_A^- are ionized donor and acceptor impurity concentration, θ is the band structure parameter for the material:

$$\theta = \chi + \frac{E_g}{2q} + \frac{kT_L}{2q}\ln\left(\frac{N_c}{N_v}\right) \quad (6)$$

where χ is the electron affinity of the material, E_g is the bandgap energy, N_c and N_v are the effective conduction and valence band density of states.

The current continuity equation has been discretized using the standard Scharfetter-Gummel scheme and Bernoulli functions which take the temperature gradient into account. Temperature dependence has been considered in both mobility models and the thermal conductivity.

Usually, the electrical characteristics of the device are calculated in a restricted device simulation domain in order to maximize computational efficiency. However, heat is dissipated in a much larger domain, including the active region of the transistor, its neighbors, the substrate, the interconnect layers, the case, and eventually the heat sink. Therefore, realistic thermal boundary conditions rely on thermal resistances, employed to account for heat dissipation into interconnects, the wafer, the case etc. For given values of thermal resistances, GARAND calculates the temperature differences using an iterative scheme according to the temperature gradient until convergence is achieved.

Since the thickness and width of the fin is less than 100 nm, the thermal conductivity can be significantly reduced compared to bulk Si, due to phonon-boundary scattering. We employ a new approximate formula for the calculation of the thermal conductivity in the fin region, which extends the previous 1D formula [1] to 2D. Consider a fin of height h and width w. Assuming that the z-axis is along the direction of fin height with the top and bottom surfaces of the fin being at z=0 and z=h, and the y-axis is along the direction of fin width with the surfaces of the fin being at y=-w/2 and y=w/2, the thermal conductivity of the fin by

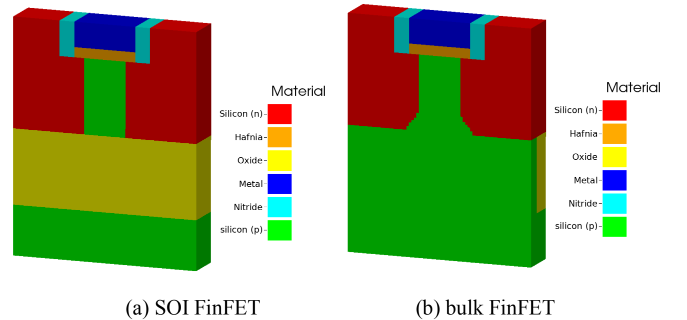
$$\kappa(y,z) = \kappa_0(T)\int_0^{\pi/2} \sin^3\theta \left\{1 - \exp\left(-\frac{h}{2\lambda(T)\cos\theta}\right)\cosh\left(\frac{h-2z}{2\lambda(T)\cos\theta}\right)\right\} d\theta$$
$$\int_0^{\pi/2} \sin^3\theta \left\{1 - \exp\left(-\frac{w}{2\lambda(T)\cos\theta}\right)\cosh\left(\frac{-2y}{2\lambda(T)\cos\theta}\right)\right\} d\theta \quad (7)$$

This new formula considers both the fin height and the fin width, and is position dependent as well as temperature dependent. Using this new calculation method, the thermal conductivity is predicted to be 1~2 orders of magnitude lower than conventional values for bulk Si.

III. RESULTS FOR FINFET EXAMPLES

The material and structure of the SOI and bulk FinFET devices used in this study are shown in Fig. 2. For both devices [7], the channel length is L_G = 25 nm, and the fin width is 12nm, while the fin height is 30nm. Spacers of 6nm are introduced on both sides of the gate. The source and drain regions are highly doped with peak concentration of 1 $\times 10^{20}$ cm^{-3} and the channel doping is 1 $\times 10^{15}$ cm^{-3}. For the bulk FinFET, a 5 $\times 10^{18}$ cm^{-3} channel stop doping is introduced below the channel. The high-k gate dielectric has an Equivalent Oxide Thickness (EOT) of 0.8nm. For the SOI FinFET, the depth of the Buried Oxide (BOX) is 30nm and in the bulk FinFET, the depth of the Shallow Trench Isolation (STI) is 30nm. The supply voltage is 0.9 Volts.

The resulting lattice temperature profile for an SOI FinFET and a bulk FinFET without external thermal resistances are shown in Fig. 3(a) and 4(a), where the ambient temperature 300K is fixed at the bottom of the solution domain and at the contacts, and a temperature dependent thermal conductivity for bulk silicon is used. The resulting electrical characteristics are shown in Fig. 3(b) and 4(b). If external thermal resistances are taken into account this modifies the resulting lattice temperature and Id-Vg characteristics for both devices as shown in Fig. 5 and 6 respectively. For the SOI FinFET, the peak lattice temperature increases from 323.1K to 350.8K, while for the bulk FinFET, the peak temperature increases from 315.7K to 341.4K.



(a) SOI FinFET (b) bulk FinFET

Fig. 2. Materials and structures of the FinFETs' electrical simulation domain, showing a cross section.

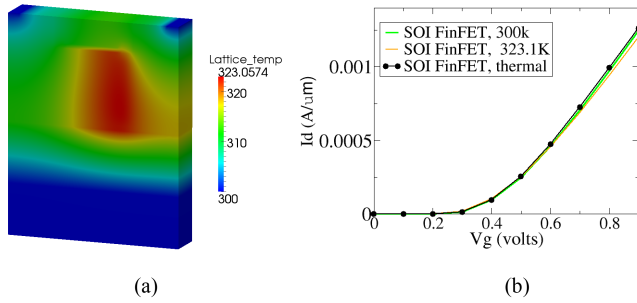


Fig. 3. Lattice temperature profile (a) and Id-Vg characteristics (b) in a SOI FinFET example, without external thermal resistances.

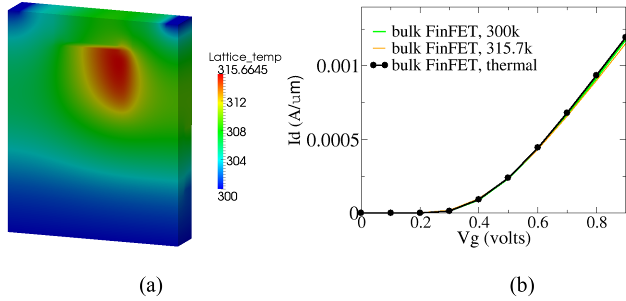


Fig. 4. Lattice temperature profile (a) and Id-Vg characteristics (b) in a bulk FinFET example, without external thermal resistances.

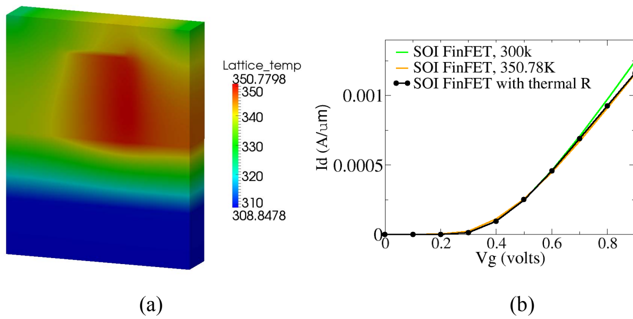


Fig. 5. Lattice temperature profile (a) and Id-Vg characteristics (b) in a SOI FinFET example, with external thermal resistances.

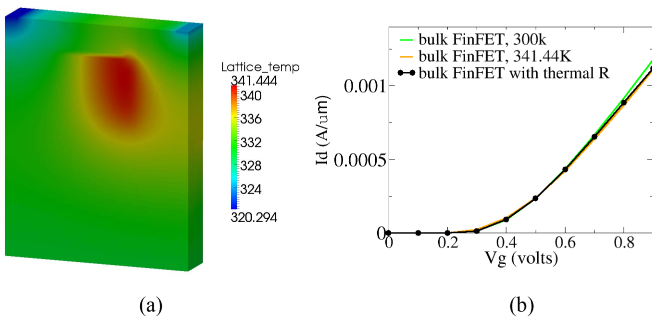


Fig. 6. Lattice temperature profile (a) and Id-Vg characteristics (b) in a bulk FinFET example, with external thermal resistances.

We now proceed to 3D electro-thermal simulations using new formula for thermal conductivity for the fin region, as up to this point the thermal conductivity of bulk Si has been used. Simulated lattice temperature distribution, Joule heat, and potential distribution, and Id-Vg characteristics at high drain voltage (0.9V) for the SOI FinFET and the bulk FinFET, using the updated thermal conductivity for the fin region and with external thermal resistances, are shown in Fig. 7 and Fig. 8 respectively. Due to the much lower thermal conductivity of the fin, a significant hot spot is produced near the drain, with peak lattice temperature reaching 457K in the SOI FinFET example while reaching 433K in the bulk FinFET example. This also indicates strong temperature gradients in the region.

In Table 1, simulation results of peak lattice temperature and on current for the SOI FinFET and bulk FinFET structures are summarised. A comparison of the simulation results of on current for the SOI FinFET and bulk FinFET structures from the coupled electro-thermal simulations with results of uniform temperature simulations is given in Table 2. Comparing to the bulk FinFET structure, the self-heating effect in the SOI FinFET structure is undoubtedly more severe due to the thermal isolation of the BOX, however the on current is comparable (7.5% reduction vs. 5.2% reduction in the bulk FinFET example).

For both FinFETs, the on current has been reduced because of self-heating effects, however, the device drive current is not only affected by the peak lattice temperature, but also by its gradient. As shown in Fig.7(d) and Fig.8(d), simulations performed with a uniform maximum lattice temperature without solving Heat Flow Equation, i.e. that does not take the temperature gradient into account, will overestimate the reduction of on current.

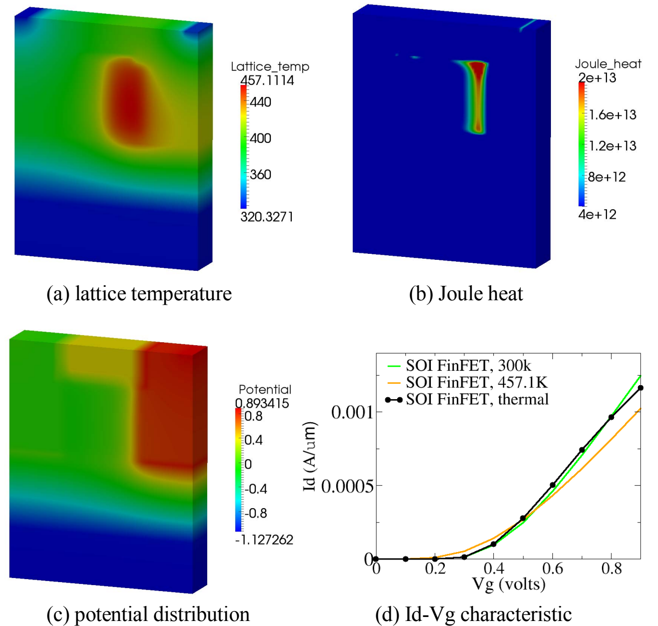


Fig. 7. Simulation results for a SOI FinFET example, using new formula for thermal conductivity for fin region and with external thermal resistances taken into account.

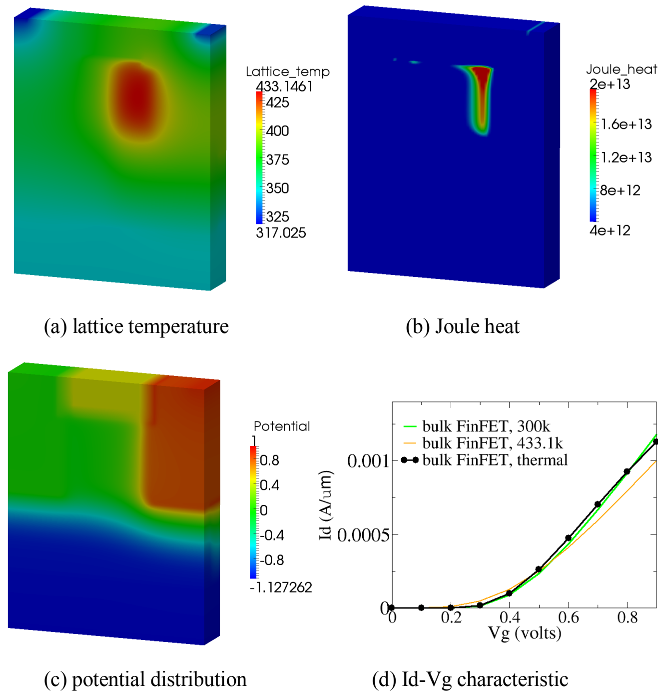


Fig. 8. Simulation results for a bulk FinFET example, using new formula for thermal conductivity for fin region and with external thermal resistances taken into account.

TABLE I. SIMULATION RESULTS OF PEAK LATTICE TEMPERATURE AND ON CURRENT FOR THE SOI FINFET AND BULK FINFET EXAMPLES

	SOI FinFET example		**Bulk FinFET example**	
	***Peak lattice temperature* (K)**	***On current* (mA/µm)**	***Peak lattice temperature* (K)**	***On current* (mA/µm)**
without external thermal resistances.	323.1	1.261	315.7	1.195
with external thermal resistances.	350.8	1.161	341.4	1.117
using new formula for thermal conductivity for fin region and with external thermal resistances.	457.1	1.163	433.1	1.129

TABLE II. COMPARISON OF SIMULATION RESULTS OF ON CURRENT FOR THE SOI FINFET AND BULK FINFET EXAMPLES FROM THE COUPLED ELECTRO-THERMAL SIMULATIONS WITH RESULTS OF UNIFORM TEMPERATURE SIMULATIONS

	SOI FinFET (mA/ µm)	**Bulk FinFET (mA/ µm)**
Uniform 300K	1.257	1.191
Electro-thermal simulations	1.163	1.129
Uniform peak temperature	1.022	0.999

a. In the electro-thermal simulations, new formula for thermal conductivity for fin region is used and external thermal resistances are included.

IV. CONCLUSIONS

A 3D thermal simulation module implemented in atomistic simulator GARAND, based on the solution of the coupled Heat Flow, Poisson, and Current Continuity Equations, has been demonstrated, in which a new approximate formula for the reduced thermal conductivity due to phonon-boundary scattering for the fin is employed. The lattice temperature profile and the corresponding Id-Vg characteristics of a SOI FinFET and a bulk FinFET have been simulated. The results show a significant hot spot generated near the drain because of the much lower thermal conductivity of the fin. Comparing to the bulk FinFET, the self-heating effect in the SOI FinFET is more severe due to the thermal isolation of BOX, however the reduction of the on current is comparable. The coupled electro-thermal simulation clearly shows that the device drive current is not only affected by the peak lattice temperature, but also by its gradient. The simulations performed with a uniform maximum lattice temperature without solving Heat Flow Equation, will overestimate the reduction of the on current.

This work lays the foundation for further electro-thermal coupling with statistical variability device simulations.

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