BTB Tunneling In InAs/Si Heterojunctions

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***Abstract*—This works presents a study of the location of 3D band-to-band tunneling barriers in order to create improved tunneling devices. Specifically, the i-Si / n-InAs junction is considered. The large lattice mismatch in this material system causes dislocations in the interface and traps in the bandgap. Alternative device configurations are considered that move the tunneling away from the physical interface, therefore reducing the the effects of lattice mismatch on tunneling current.**

I. Introduction

Tunneling devices have shown clear promise in providing a steep subthreshold slope, garnering much interest for ultra low power switching applications. Due to the indirect nature of the energy band gap (Fig. 1), tunneling in Si devices requires the assistance of phonons (Fig. 2a). This, in turn, decreases the tunneling probability. Consequently, direct materials are considered for construction of Si/III-V heterojunctions for tunneling devices. This material system has a direct bandgap (Fig. 2b) and band-to-band (BTB) tunneling occurs at the Γ point, (Fig. 1). While promising, these materials do not come together without challenges. InAs/Si create highly lattice mismatched junctions, resulting in dislocations in the interface [1], giving rise to traps in the bandgap.

In this work, we consider the possibility of designing the InAs/Si heterojunction in such a way to decrease the effect of the dislocations in tunneling current. It has been suggested that this could be achieved by ensuring that BTB tunneling occurs farther from the heterojunction interface, [1]. We present simulation studies and improvements to the InAs/Si junction in a TFET device by performing 3D band-to-band tunneling simulations for varied junction configurations. We will consider the effects of gate overlap and insertion of an i-InAs segment in order to shift the tunneling barrier.

II. Band-to-Band Tunneling

Recently, we presented a 3D approach for computation of BTB tunneling in direct semiconductors [2]. The developed method consists of two parts: computation of an effective tunneling barrier and propagating wave function computation.

The effective tunneling barrier is extracted from valence and conduction bands. These are obtained using a self-consistent Schrödinger-Poisson model that is part of the Vienna Schrödinger-Poisson (VSP) solver framework [3]. The effective barrier exhibits valence band properties in some parts of the device, and conduction band properties in others. The locations of the transitions are calculated for a specific energy E by comparing the momenta of valence and conduction bands:

$$M_{\mathrm{v}}^2 = m_{\mathrm{v}}\,(E - E_{\mathrm{v}}) \quad \text{and} \quad M_{\mathrm{c}}^2 = m_{\mathrm{c}}\,(E_{\mathrm{c}} - E)\,. \tag{1}$$

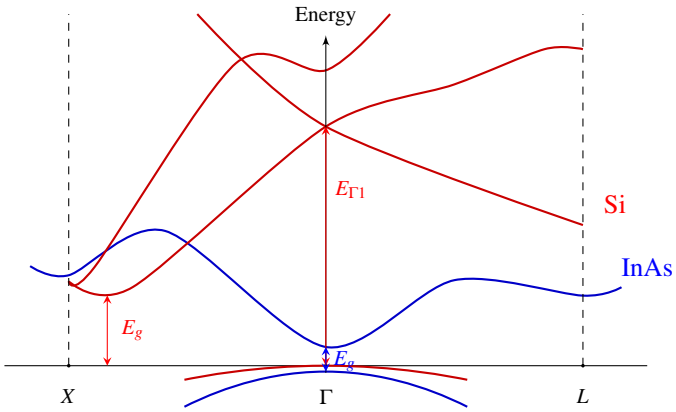

Fig. 1: Band structure of InAs and Si. E_g is the bandgap of InAs (blue) and Si (red)

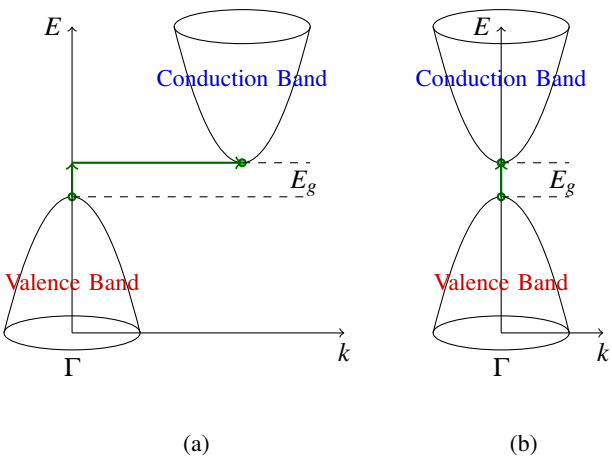

Fig. 2: (a) Phonon assisted tunneling in an indirect band gap (b) Direct band gap transition

The effective barrier potential is then obtained,

$$E_{\mathrm{eff}} = \begin{cases} 2E - E_{\mathrm{v}}, \\ E_{\mathrm{c}}, \end{cases} \quad m_{\mathrm{eff}} = \begin{cases} m_{\mathrm{v}}, & M_{\mathrm{v}} \le M_{\mathrm{c}} \\ m_{\mathrm{c}}, & M_{\mathrm{v}} > M_{\mathrm{c}}. \end{cases} \tag{2}$$

The extracted BTB tunneling barrier responds naturally to changes in device geometry, material parameters and applied bias (Fig. 3).

Once the effective tunneling barrier is extracted, injection eigenmodes are computed in the contacts by solving the closed boundary effective mass Schrödinger equation (Fig. 4a). Once the wave functions in the contacts are found, the propagating

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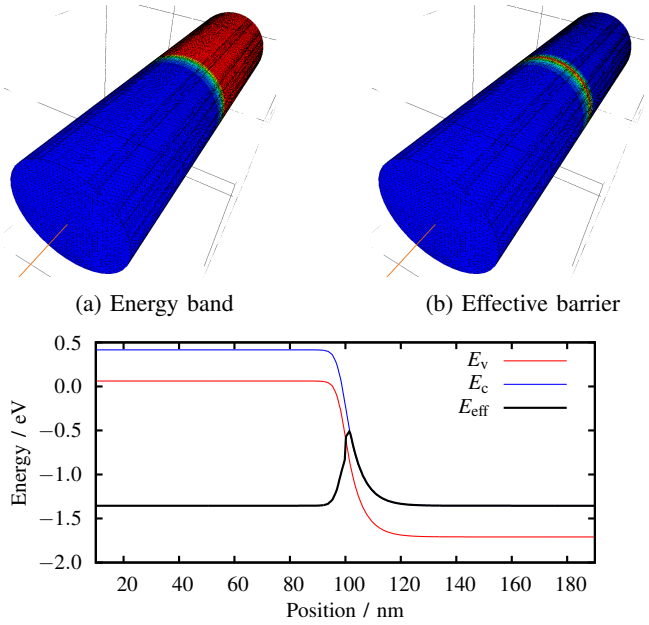
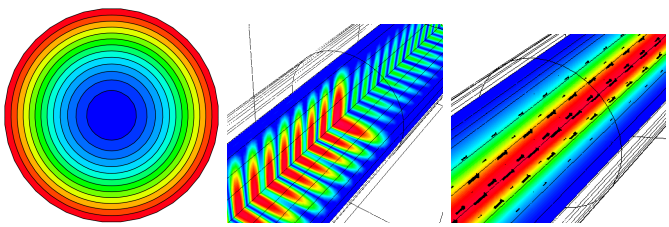


(a) Energy band (b) Effective barrier

(c) 1D Effective barrier

Fig. 3: (a) Self-consistently calculated energy bands of a nanowire p-n junction; (b) Effective tunneling potential barrier from (a); (c) 1D cut through (a) and (b)



(a) Contact mode (b) Wave function (c) Current

Fig. 4: Sample mode propagation through a barrier

waves through the 3D device can be calculated for each mode by solving the QTBM-like Schrödinger equation:

$$\left[\frac{-\hbar^2}{2m_{\text{eff}}}\nabla^2 + V + E\right]\Psi_{\text{E}} = \Psi_{\text{n}}, \tag{3}$$

where V contains the self-consistent Hartree potential and the extracted effective potential barrier E_{eff}. Ψ_{n} is an eigenmode wave function injected from a contact, and Ψ_{E} is the resulting wave function in the device (Fig. 4b).

The tunneling current is then computed through the effective barrier by combining eigenmode contributions,

$$J_{v\to c} = \int_{E_{\text{min}}}^{E_{\text{max}}} \sum_{n=0}^{N_m} J_n(E)\,dE, \tag{4}$$

where N_m denotes the number of injection modes, and $J_n(E)$ is the tunneling current due to injection mode n at a tunneling energy E.

In order to gain a better understanding of the tunneling barrier location over all the tunneling energies a combined

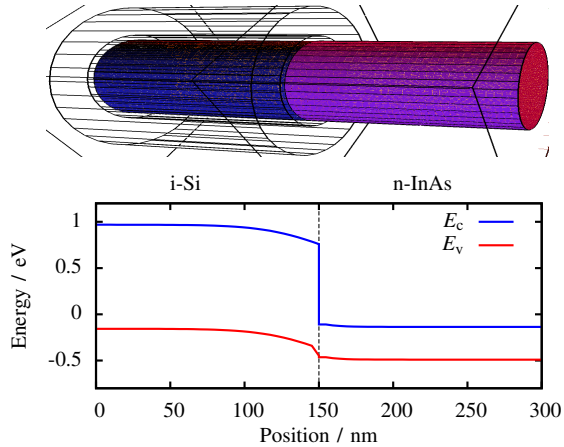


Fig. 5: i-Si / n-InAs tunneling barrier simulation 3D: device structure and 1D energy bands

effective barrier is computed:

$$E_{\text{combined}} = \sum_{E_{\text{min}}}^{E_{\text{max}}} E_{\text{eff}}(E)\,T(E) \tag{5}$$

where E_{min} and E_{max} are the limits of tunneling integration from Eq. (4), T is the transmission coefficient and E_{eff} is the effective barrier from Eq. (2). Definition in Eq. (5) gives most significance to the tunneling barrier where most tunneling would occur, while still providing an overall tunneling barrier location for the device.

III. Simulation Results

In this work, simulations are performed for the i-Si / n-InAs interface in a gate-all-around (GAA) TFET device. The i-Si portion of the NW is gated, whereas the n-InAs section is doped (N_{D}=$1\times10^{18}\,\text{cm}^{-3}$), resulting in the band structure in Fig. 5. In order to study the location of BTB tunneling at all energies, a combined effective barrier is computed, Eq. (5).

From a few bias conditions, it is observed that the tunneling barrier is clearly located at the physical interface between Si and InAs, Fig. 6. Performing the BTB tunneling simulations in 3D allows us to visualize the effective barrier, Fig. 6b, Fig. 6c. Cylindrical shape of the device has resulted in a curvature of the tunneling barrier. The barrier shows widening at the center of the device. This results in tunneling wave propagation most likely occurring closer to the surface. The effect of bias on the tunneling barrier is also visualized. Higher applied bias results in a narrower barrier with a smaller curvature in the center. The tunneling current is shown in Fig. 9. Comparing this to experimentally obtained results from [4] shows that the simulation highly overestimates the tunneling current. This is expected, since simulation assumes a simple bandgap tunneling problem. Due to the lattice mismatch of the Si/InAs interface, tunneling occurs at the physical interface and is plagued by traps and bandgap states.

In order to move the tunneling location from this interface, we consider the simple modification of gate position. An

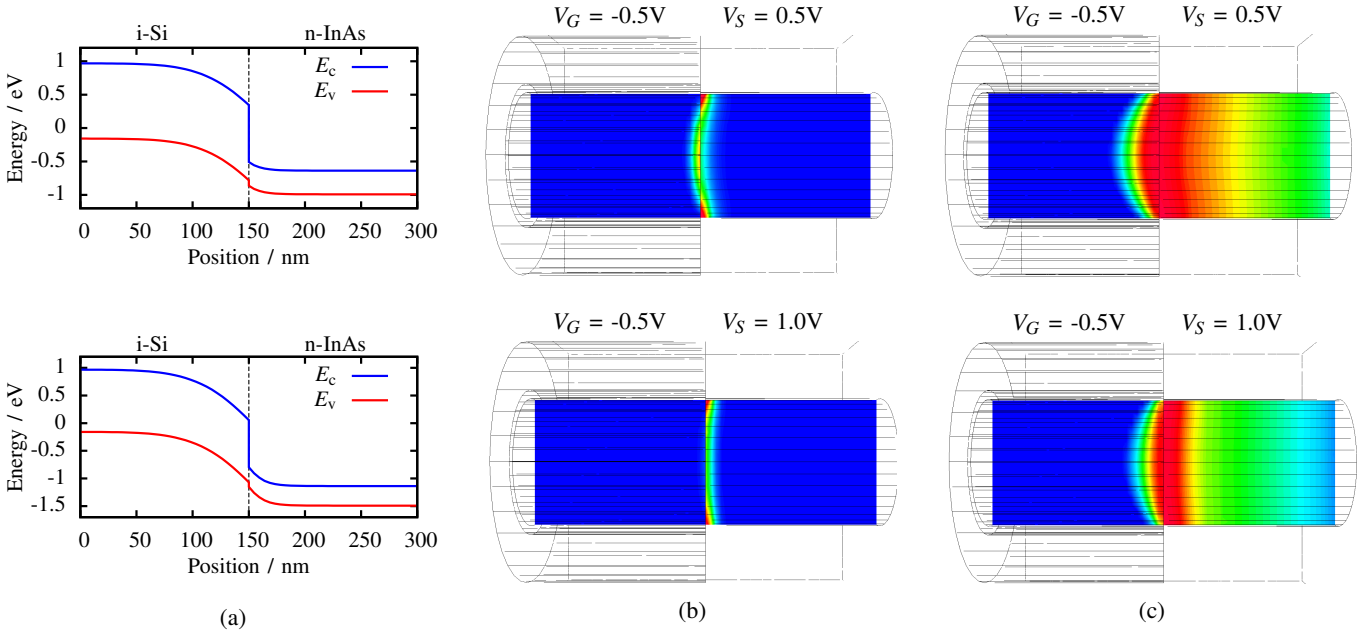


Fig. 6: i-Si / n-InAs 1D energy bands (b) Effective tunneling barrier (c) Log-scaled effective tunneling barrier

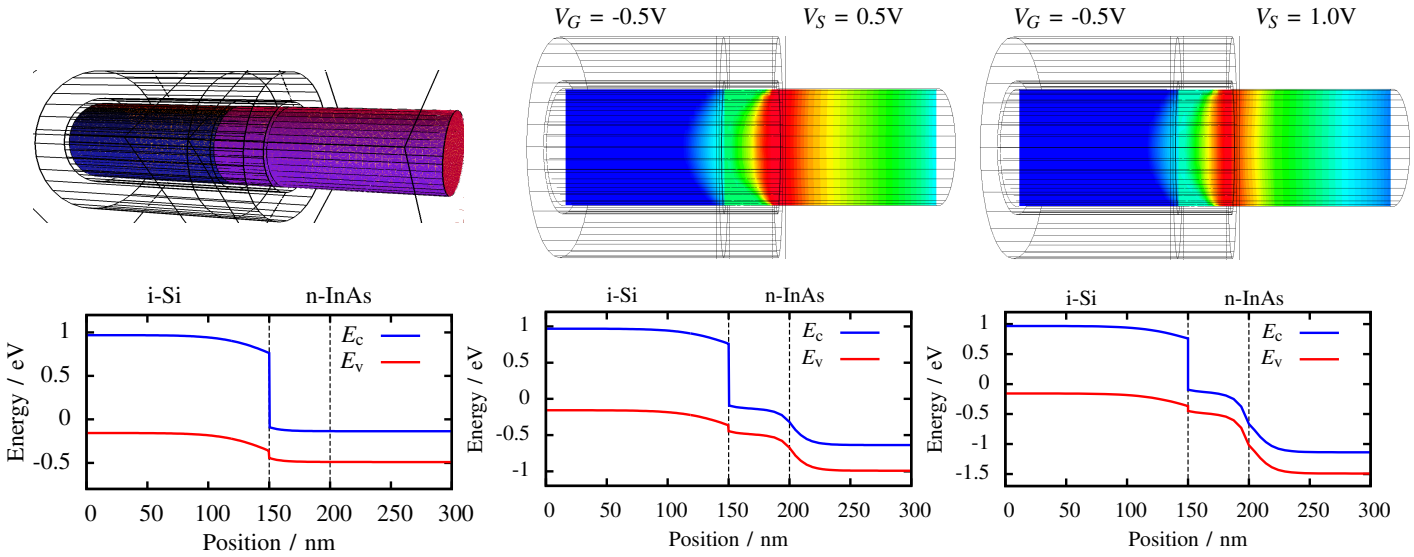


Fig. 7: i-Si / n-InAs with 50nm gate overlap, tunneling barrier simulation

effective tunneling barrier location was simulated for a gate overlapped structure (Fig. 7). In this configuration, tunneling occurs inside the n-InAs portion of the junction, moving the effective tunneling barrier away from the physical material interface. As with the previous simulations, we observe the geometry effects on the tunneling barrier. The widest barrier is in the center, and the tunneling, once again, is most likely to occur closer to the surface. The gate overlap has resulted in an overall narrowing of the tunneling barrier compared to the previously studied device (Fig. 6). Location of this tunneling barrier strongly relies on the length of the gate-overlap. Since we are relying on the gate overlap to open the tunneling inside the n-doped region, the total tunneling current is significantly decreased, as shown in Fig. 9.

To study further alternatives to TFET design, an investigation of Si TFET improvement was performed. It was found that many approaches consider inserting differently doped material segments to improve the tunneling conditions [5], [6]. Similarly, we have created this in the i-Si / n-InAs junction, by insert an undoped InAs layer to create an i-Si / i-InAs / n-InAs structure, (Fig. 8). The insertion of a gated i-InAs layer moves the tunneling boundary into InAs and away from the heterojunction. This device configuration results in a narrower barrier, compared to both of the previous structures.

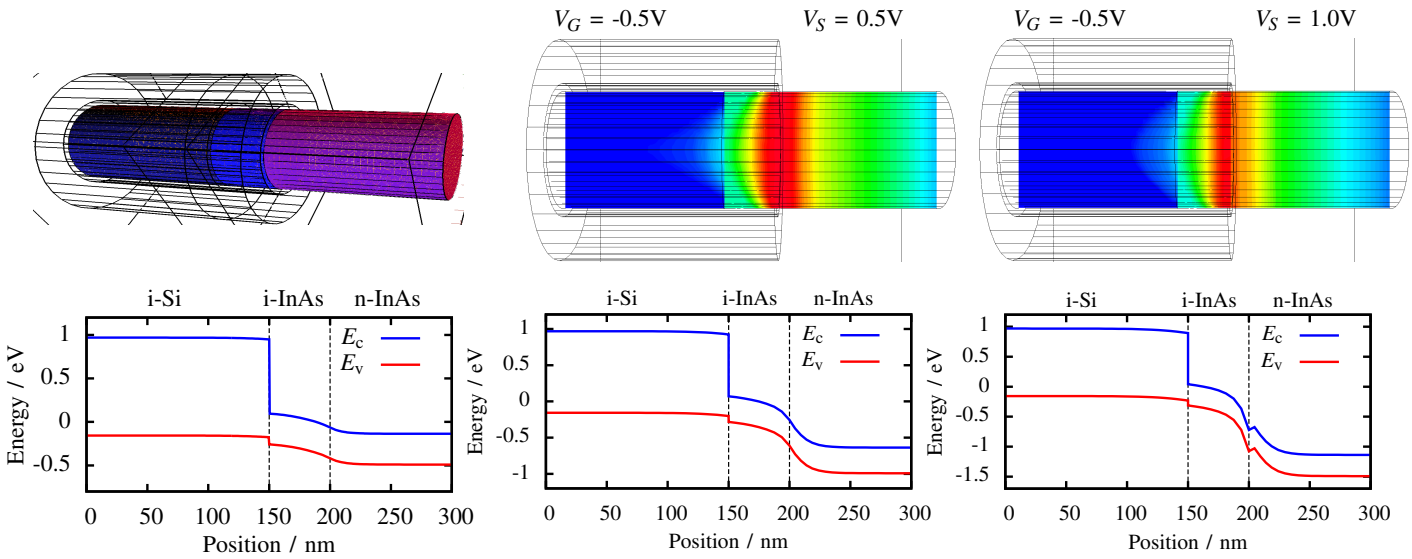


Fig. 8: i-Si / i-InAs / n-InAs tunneling barrier simulation

IV. Discussion

Silicon is an indirect bandgap material, and as such, requires phonon interaction to assist the tunneling process. Alternatively, Si / III-V junctions are investigated for tunneling applications. These, achieve a direct bandgap and do not require phonons.

In this work, a 3D direct band-to-band tunneling method is used for the study of the i-Si / n-InAs heterojunction. In order to decrease the effects of dislocations in the heterojunction, we simulate various device configurations that would move the tunneling location away from the physical interface.

By adding gate overlap (Fig. 7) and inserting an undoped InAs segment, (Fig. 8), we have demonstrated that the tunneling barrier can be designed away from the physical interface. The simulated devices are compared with a fabricated device [4] by comparing the tunneling current, (Fig. 9). As expected, the initial device (Fig. 6) results in an overestimation of tunneling current, as the ideal direct tunneling is only considered. Gate overlap moves the tunneling barrier away from the physical interface, and it decreases the tunneling current. The alternative device configuration of i-Si / i-InAs / n-InAs, moves the tunneling barrier while resulting in a larger tunneling current.

This study demonstrates the value of 3D simulations of tunneling devices in order to study various segment configurations. The computed 3D tunneling barrier responds naturally to changes in device geometry, material parameters and applied bias. The flexibility of this approach could further be exploited to minimize the challenges faced by the novel devices and material combinations.

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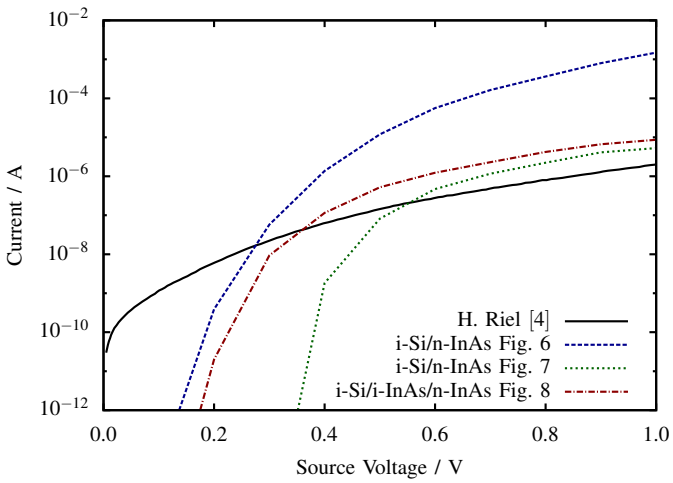

Fig. 9: Current computation, V_G = -0.5V

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