Abstract #1341, 227th ECS Meeting, © 2014 The Electrochemical Society

(Invited) Spin-Based Silicon and CMOS-Compatible Devices

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With CMOS feature size rapidly approaching ultimate scaling limits the electron spin attracts much attention as an alternative degree of freedom for low-power non-volatile applications [1]. Silicon, the main material of microelectronics, is perfectly suited for spin-driven applications, because it is mostly composed of nuclei without spin and is characterized by weak spin-orbit interaction [2]. Both factors favor a long electron spin lifetime in silicon.

However, even a weak spin-orbit interaction causes the electron spin lifetime to decrease. The Elliot-Yafet spin relaxation due to phonons' mediated scattering between the valleys along different crystallographic axes is the main spin relaxation mechanism in bulk silicon at room temperature [3,4]. This inter-valley scattering can be effectively eliminated by partially lifting the valley degeneracy either by stress or by confining an electron system. In strained silicon the spin lifetime can indeed be increased by a factor of two. In contrast, in silicon-on-insulator structures the spin lifetime is reduced; and methods to increase the spin lifetime are needed.

Uniaxial stress dramatically reduces the spin relaxation and boosts the spin lifetime by an order of magnitude in thin silicon films [5]. The physical reason for the spin lifetime enhancement lies in the capability to lift completely the degeneracy between the two valleys in a confined electron systems by shear strain [6]. This degeneracy was a long-standing problem in silicon spintronics [7]; indeed, apart from causing a strong spin decoherence and relaxation, the degeneracy between the valleys introduces an unwanted competition between the quantum numbers of the valleys and electron spin, thus potentially threatening spin-based device operation. Therefore, lifting the valley degeneracy completely in a controllable way by means of standard stress techniques represents a major breakthrough in future silicon spin-driven applications.

Despite impressive progress in spin injection in silicon at room temperature [2,8], the larger than predicted amplitude of the signal [2] is heavily debated prompting alternative explanations [9]. In addition, low efficiency of spin injection from ferromagnetic metal leads in silicon and the absence of a viable concept of electron spin manipulation in the channel by purely electrical means makes a practical realization of a device working on a principal similar to a MOSFET difficult. An experimental demonstration of the Datta-Das Spin FET [10] is pending for 25 years now. This motivates researchers to look into MOSFET and CMOS compatible spin-driven devices and applications.

Commercially available CMOS compatible spin-transfer torque magnetic random access memory (MRAM) built on magnetic tunnel junctions (MTJs) possesses all properties characteristic to universal memory: fast operation, high density, and non-volatility. The reduction the critical current for magnetization switching is the main challenge. Perpendicular MTJs allow circumventing the problem at the expense of thermal stability [11]. The thermal stability is considerably increased in structures with a free layer composed of two vertically sandwiched layers [11]. An alternative path is to consider in-plane structures with composite free magnetic layers [12]. A substantial reduction of the critical current density is achieved, when the free layer is composed of two similar parts in the same plane next to each other [13]. The critical current reduction and/or switching is caused by the fact that the magnetization of the free layer remains in plane.

MRAM can be used to build non-volatile logic-in-memory architectures with non-volatile storage elements on the top of logic circuits. Non-volatility and reduction of interconnects guarantee low-power consumption [14]. MRAM-CMOS hybrid ternary content-addressable memory and lock-up table circuits were demonstrated [14]. An alternative concept for non-volatile logic-in-memory circuits utilizes the same MRAM cells to store and process information simultaneously [15].

The work is supported by the European Research Council through the grant #247056 MOSILSPIN.

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