Spin-Based Devices for Future Microelectronics

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***Abstract*—With CMOS technology rapidly approaching its scaling limits, the electron spin attracts much attention as an alternative degree of freedom for low-power applications. Silicon is suited for spin-driven applications because of its long spin lifetime. In confined electron systems the spin lifetime can be increased significantly by uniaxial stress. However, despite the many achievements, an experimental demonstration of a spin-based field effect transistor (SpinFET) is pending due to low spin injection efficiency and difficulties to manipulate spins electrically. This motivates researchers to look into CMOS-compatible spin-driven devices. Spin-transfer torque MRAM is fast, compact, and non-volatile; however, the high current for magnetization switching is a challenge. For in-plane magnetization a substantial reduction of the current is achieved, when the free layer is composed of two parts. In addition to information storing, the same MRAM cells can also be used for information processing, paving a path towards non-volatile logic-in-memory architectures.**

I. Introduction

The tremendous increase in performance, speed, and density of modern integrated circuits is determined and stipulated by a sucsessful continuous miniaturization of CMOS devices. There are good indications that device miniaturization with some technological adaptations will continue its pace down to 10nm feature size and beyond. In order to continue with scaling further, a possible modification of channel material with improved characteristics is foreseen [1]. The introduction of new materials with higher mobility, combined with a multi-gate three-dimensional architecture for improved electrostatic control, will potentially allow to proceed with scaling below 7nm; however, growing critical technological challenges and soaring costs will gradually bring CMOS scaling to a saturation.

The principle of MOSFET operation is fundamentally based on the charge degree of freedom of an electron. Another intrinsic electron feature, the electron spin, attracts at present much attention as a possible candidate for complementing or even replacing the charge degree of freedom in future electron devices [2], [3]. The electron spin state is characterized by one of the two of its possible projections on a given axis and could be potentially used in digital information processing. In addition, it takes an amazingly small amount of energy to invert the spin orientation, which is necessary for low power applications.

Silicon predominantly consists of ^{28}Si nuclei with zero magnetic moment, with only a few percent admixture of magnetic ^{29}Si nuclei, and is characterized by weak spin-orbit interaction in the conduction band. Because of these properties electron spin states of conduction electrons in silicon should show long lifetime, which makes silicon a perfect candidate for spin-driven device applications. Next we briefly describe a spin field-effect transistor [4] and outline some of the challenges that prevented it from being realized so far.

II. Spin field-effect transistor

A spin field-effect transistor (SpinFET) is a future semiconductor spintronic device promising a performance superior to what can be achieved by present transistor technology [4]. SpinFETs are composed of two ferromagnetic contacts (source and drain), linked by a non-magnetic semiconductor channel region. The current modulation is achieved by tuning the strength of the spin-orbit interaction in the semiconductor region, which depends on the effective electric field and can be controlled by purely electrical means applying a gate voltage.

A. *Spin injection*

Spin injection in silicon and other semiconductors by purely electrical means from a ferromagnetic metal electrode was not very successful until recently. The fundamental reason has been identified as an impedance mismatch problem [5]. One solution to overcome this problem is the use of hot electron injection [6]; however, the efficiency of spin injection and detection is very limited.

Another solution to the impedance mismatch problem is the introduction of a potential barrier between the metal ferromagnet and the semiconductor [7]. Room temperature spin injection into n- and p-doped silicon was first demonstrated in 2009 [8], [9].

One of the unsolved issues is a several orders of magnitude discrepancy between the signal measured in a three-terminal spin accumulation measuring scheme and the theoretical value. The reasons for these discrepancies are heavily debated [10], [11], [12] and it is apparent that more research is needed.

B. *Spin propagation*

The injected excess spin is not a conserved quantity: while diffusing, it gradually relaxes to its equilibrium value which is zero in a non-magnetic semiconductor. The spin lifetime in undoped silicon at room temperature is about 10ns [13], [14], which corresponds to a spin diffusion length of 2μm. The spin lifetime is determined by the spin-flip processes. Several important spin relaxation mechanisms are identified [2], [3]. The Elliot-Yafet spin relaxation due to phonons mediated scattering between the valleys along different crystallographic axes is the main spin relaxation mechanism in bulk silicon at room temperature [14], [15]. This relaxation can be effectively eliminated by partially lifting the valley degeneracy either by stress or by confining an electron system. In strained silicon the spin lifetime can indeed be increased by a factor of two

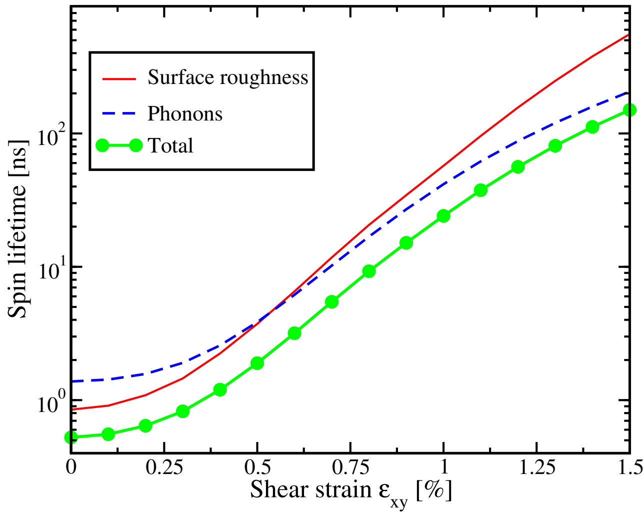

Fig. 1. Dependence of spin lifetime on shear strain for T=300K and film thickness 2.1nm (cf. [19]).

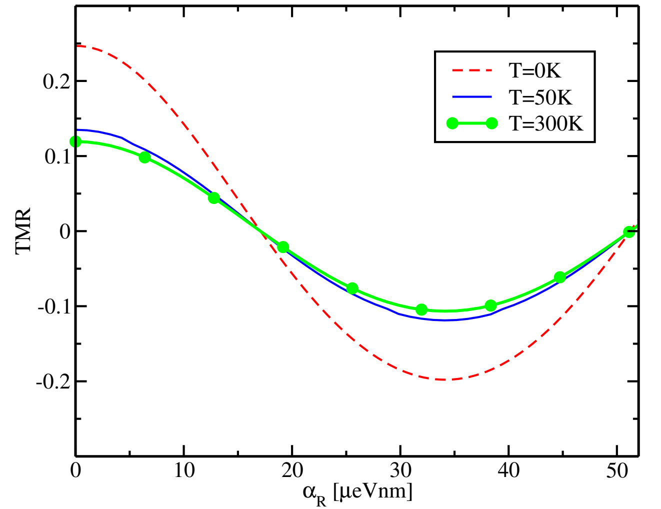

Fig. 2. TMR dependence on the value of the spin-orbit coupling α_R for several values of temerature (cf. [26]).

to three depending on the spin injection direction. In contrast, in silicon-on-insulator structures the spin lifetime is reduced, and methods to increase the spin lifetime are needed.

C. Spin lifetime in thin films and surface layers

In size-confined electron systems of (001)-oriented inversion layers the degeneracy between the six valleys is partly lifted, which leads to the suppression of f-phonons mediated spin-flip processes and should result in an enhancement of the spin lifetime. However, the relatively large spin relaxation experimentally observed in electrically-gated lateral-channel silicon structures [16], [17] indicates that the extrinsic interface induced spin relaxation mechanism becomes important. This may pose an obstacle in realizing spin-driven CMOS compatible devices, and a deeper understanding of fundamental spin relaxation mechanisms in silicon inversion layers, thin films, and fins is needed.

Uniaxial stress dramatically reduces the spin relaxation and boosts the spin lifetime by orders of magnitude in thin silicon films [18]. A strong increase of the spin lifetime is demonstrated in Fig.1 [19]. The increase is less pronounced, if the term responsible for the valley splitting in relaxed films is taken into account; however, even in this case the spin lifetime is boosted by almost two orders of magnitude.

The physical reason for the spin lifetime enhancement lies in the capability to lift completely the degeneracy between the two valleys in a confined electron systems by shear strain [20]. This degeneracy was a long-standing problem in silicon spintronics [21]. Indeed, apart from causing a strong spin decoherence and relaxation, the degeneracy between the valleys introduces an unwanted competition between the quantum numbers of the valleys and the electron spin, thus potentially threatening spin-based device operation. Therefore, lifting the valley degeneracy completely in a controllable way by means of standard stress techniques represents a major breakthrough for future silicon spin-driven applications.

D. Electric spin manipulation

In a SpinFET [4], the total current through the device depends on the relative angle between the magnetization direction of the drain contact and the electron spin polarization at the end of the semiconductor channel. Current modulation is achieved by tuning the strength of the spin-orbit coupling in the semiconductor region. The spin-orbit coupling is usually taken in the Rashba form [22], [23] with the effective electric field-dependent strength α_R of the spin-orbit coupling. The spin precession angle $\Delta\theta$ defined as the difference between the orientation of the spin of the electron at the end and at the beginning of the semiconductor region is [24]

$$\Delta\theta = \frac{2\alpha_R m^*}{\hbar^2} L, \qquad (1)$$

where m^* is the effective mass of the electron, and L is the length of the semiconductor channel. The effective mass depends on the quantization direction and the channel orientation. Due to the non-parabolicity of the conduction band [25] the effective mass also depends on the thickness of the silicon channel [18]. The effective length of the channel required to achieve a substantial spin precession and magnetoresistance (TMR) modulation is inversely proportional to the effective mass m^*. Therefore, channels with larger effective mass are prefered.

TMR modulation as a function of the spin-orbit interaction strength is achieved even at elevated temperatures (Fig.2) if the spin is injected through the tunnel barriers. This opens a practical possibility to modulate the TMR even at room temperature. Unfortunately, because the spin-orbit interaction in silicon is weak, the channel length required to achieve a proper TMR modulation is much larger than the length of the channel of modern transistors. Even in the best case scenario of a [001] oriented fin [26] the channel length required to modulate the TMR is about a micron. For shorter channels, the only option to realize a SpinFET is to exploit the relative magnetic orientation of the source and drain ferromagnetic contacts [24]. This adds a possibility to reprogram MOSFETs and to obtain a different current under the same drain and

gate voltage by changing the drain magnetization orientation. It is important that, once modified, the magnetization remains the same infinitely long without any extra power applied. This property is used in emerging magnetic non-volatile memories.

III. Spin-transfer torque magnetic RAM

The prediction [27], [28] of purely electrical switching of the magnetization in magnetic tunnel junctions by means of the spin-transfer torque (STT) makes STT magnetic random access memory (MRAM) a promising candidate for future universal memory. Indeed, STT-MRAM is characterized by small cell size ($4F^2$) and high density inherent to DRAM, fast access time (less than $10ns$) intrinsic to SRAM, non-volatility and long retention time subject to flash, and high endurance (10^{14}). The basic element of the STT-MRAM is a magnetic tunnel junction (MTJ). The three-layer MTJ represents a sandwich of two magnetic layers separated by a thin spacer which forms a tunnel barrier. While the magnetization of the pinned layer is fixed, the magnetization orientation of the free layer can be switched between the two stable states parallel and anti-parallel to the fixed magnetization direction. Switching between the two states is induced by spin-polarized current flowing through the MTJ. Because the spin-polarized current is only a fraction of the total charge current passing through the cell, fairly high currents are required to switch the magnetization direction of the free layer. The reduction of the current required for switching and the increase of the switching speed are the most important challenges in STT-MRAM developments [29].

Depending on the orientation of the layer magnetizations, the magnetic elements are characterized by perpendicular with out-of-plane magnetization and in-plane with the magnetization lying in the plane of the magnetic layers. The problem of a relatively high switching current in in-plane structures lies in the specificity of the switching dynamics: the magnetization must get out of plane during the switching, which results in an additional penalty contribution to the switching barrier. The switching barrier is higher as the thermal barrier separating the two stable magnetization states. The latter is due to the magnetic layer shape anisotropy.

The solution of the problem of higher switching barrier is to resort to perpendicular MTJs. In these MTJs the switching path is the same as the path for magnetization reversal due to thermal agitations. Therefore, the switching barrier is equal to the thermal barrier. However, the reduction of the Hilbert damping and thus the switching current density [30] and the increase of thermal stability in perpendicular structures [31], [32] are substantial challenges for the known materials and prompts effortful search for new materials with superior characteristics.

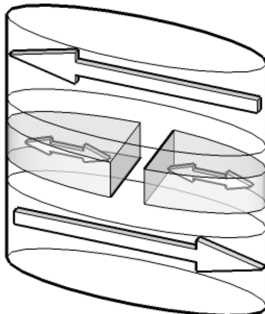

Fig. 3. MRAM cell with a composite free layer.

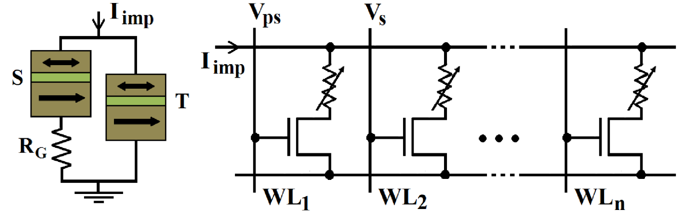

Fig. 4. MTJ- and MRAM-based implication logic architecture.

Another option is to use an in-plane structure with a composite free magnetic layer made of two half-elliptic parts separated by a narrow gap [33]. A structure with an elliptical cross-section and the following layer sequence CoFeB(5nm)/MgO(1nm)/CoFeB(2nm)/MgO(1nm) /CoFeB(5nm) was considered. The central 2.5nm stripe is removed from the middle CoFeB layer (Fig.3). The switching processes of the left and right parts of the composite free layer occur in opposite senses to each other. Most importantly, the magnetization of each half stays almost in-plane. The switching energy barrier is almost equal to the thermal stability barrier, which results in a three-fold reduction of the switching time [33].

IV. Logic-in-memory

The introduction of non-volatile logic could help to reduce significantly heat generation, especially at stand-by, booting, and resuming stages. It is extremely attractive to use the same elements as memory and latches, which reduces the time delay and energy waist while transferring data between CPU and memory blocks in conventional computer architectures. STT-MTJ-based memory has all the characteristics of a universal memory [34]. Furthermore, the MTJ technology is attractive for building logic configurations which combine non-volatile memory cells and logic circuits (so-called logic-in-memory architecture) to overcome the leakage power issue [35], [36], [37]. Recently, the realization of MTJ-based non-volatile logic gates has been demonstrated, for which the MTJ devices are used simultaneously as non-volatile memory cells and main computing elements [38], [39], [40]. The MTJ-based logic gates reported in [40] are designed on an implication circuit topology (Fig.4).

The logic operation (N)IMP is realized based on a conditional switching in the target (T) MTJ [40] depending on the initial resistance states of the source (S) and the target MTJs.

Due to the easy integration of MTJs on top of a CMOS circuit, the MTJ-based logic gates could be implemented within STT-MRAM arrays without the need of extra hardware and generalized to large-scale non-volatile circuits (Fig.4), where the same elements are used for information storage and processing.

V. Summary and Conclusion

Spin-based devices are promising for future low-power electronics. Regardless recent experimental and theoretical breakthroughs in understanding spin properties in silicon, more research is needed to enhance spin injection and spin lifetime to bring them to applications. It is demonstrated that a standard mechanical stress technique routinely applied to enhance the electron mobility can also be used to boost the spin lifetime significantly. An efficient coupling between the electrical and the magnetic degrees of freedom makes STT-MRAM a viable candidate for future universal memory, which is fast, non-volatile, and CMOS compatible. Building implication logic gates from STT-MRAM cells opens the road towards intrinsic logic-in-memory architecture, where the same elements are employed to store and to process information.

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