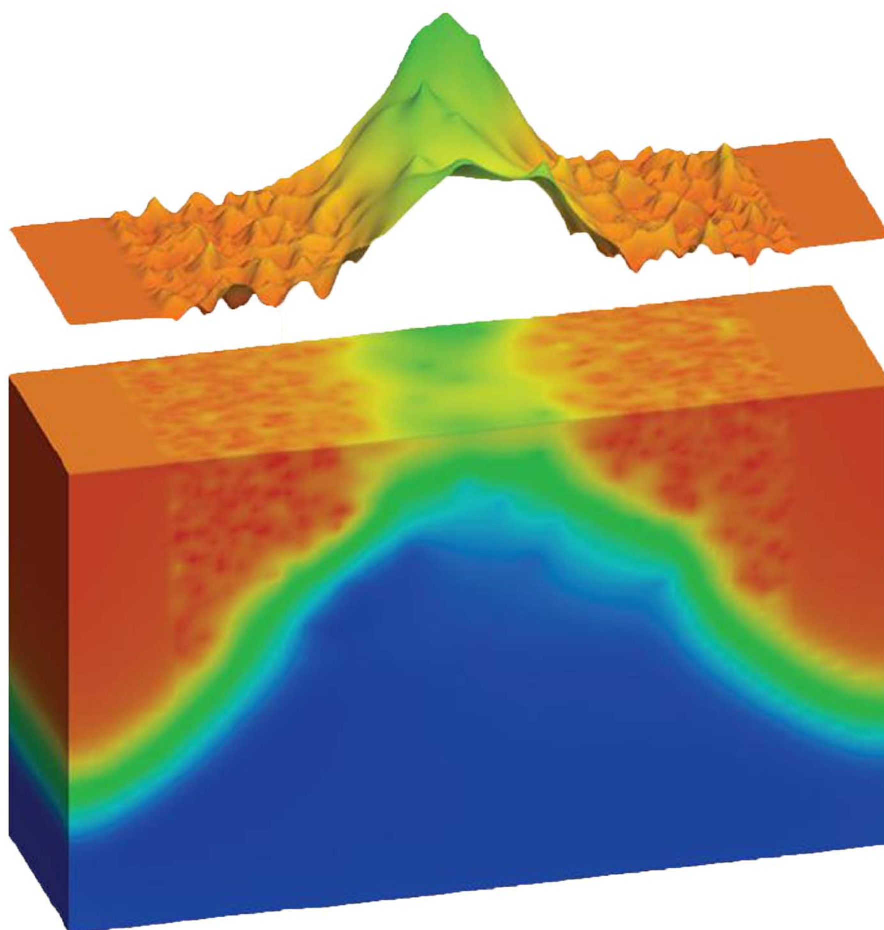
IEEE TRANSACTIONS ON

ELECTRON DEVICES

A PUBLICATION OF THE IEEE ELECTRON DEVICES SOCIETY

AUGUST 2011 VOLUME 58 NUMBER 8 IETDAI (ISSN 0018-9383)

SPECIAL ISSUE ON CHARACTERIZATION OF NANO CMOS VARIABILITY BY SIMULATION AND MEASUREMENTS



The electron density distribution in a 35 nm device, simulated with RDD, LER, and MGG as sources of variability. The surface indicates the potential landscape.

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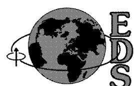

AUGUST 2011 VOLUME 58 NUMBER 8 IETDAI (ISSN 0018-9383)

SPECIAL ISSUE ON CHARACTERIZATION OF NANO CMOS VARIABILITY BY SIMULATION AND MEASUREMENTS

FOREWORD

Special Issue on Characterization of Nano CMOS Variability by Simulation and Measurements . . . . . . *E. Sangiorgi, A. Asenov, H. S. Bennett, R. W. Dutton, D. Esseni, M. D. Giles, M. Hane, K. Nishi, J. Ranaweera, and S. Selberherr* 2190

SPECIAL ISSUE PAPERS

Process Technology Variation . . . .
K. J. Kuhn, M. D. Giles, D. Becher, P. Kolar, A. Kornfeld, R. Kotlyar, S. T. Ma, A. Maheshwari, and S. Mudanai 2197

Quantum-Transport Study on the Impact of Channel Length and Cross Sections on Variability Induced by Random Discrete Dopants in Narrow Gate-All-Around Silicon Nanowire Transistors . . . .
. . . . *A. Martinez, M. Aldegunde, N. Seoane, A. R. Brown, J. R. Barker, and A. Asenov* 2209

Hierarchical Simulation of Process Variations and Their Impact on Circuits and Systems: Methodology . . . .
. . . . *J. K. Lorenz, E. Bär, T. Clees, R. Jancke, C. P. J. Salzig, and S. Selberherr* 2218

Hierarchical Simulation of Process Variations and Their Impact on Circuits and Systems: Results . . . .
J. K. Lorenz, E. Bär, T. Clees, P. Evanschitzky, R. Jancke, C. Kampen, U. Paschen, C. P. J. Salzig, and S. Selberherr 2227

Characterization and Modeling of Transistor Variability in Advanced CMOS Technologies . . . .
. . . . *C. M. Mezzomo, A. Bajolet, A. Cathignol, R. Di Frenza, and G. Ghibaudo* 2235

Direct Measurement of Correlation Between SRAM Noise Margin and Individual Cell Transistor Variability by Using Device Matrix Array . . . . *T. Hiramoto, M. Suzuki, X. Song, K. Shimizu, T. Saraya, A. Nishida, T. Tsunomura, S. Kamohara, K. Takeuchi, and T. Mogami* 2249

Statistical Enhancement of the Evaluation of Combined RDD- and LER-Induced V_T Variability: Lessons From 10^5 Sample Simulations . . . . *D. Reid, C. Millar, S. Roy, and A. Asenov* 2257

An Approach Based on Sensitivity Analysis for the Evaluation of Process Variability in Nanoscale MOSFETs . . . . .
. . . . *V. Bonfiglio and G. Iannaccone* 2266

(Contents Continued on Page 2186)

(Contents Continued from Page 2185)

A Comparative Study of Surface-Roughness-Induced Variability in Silicon Nanowire and Double-Gate FETs . . . . . . *A. Cresti, M. G. Pala, S. Poli, M. Mouis, and G. Ghibaudo* 2274
Grain-Orientation Induced Quantum Confinement Variation in FinFETs and Multi-Gate Ultra-Thin Body CMOS Devices and Implications for Digital Design . . . . *S. Hadi Rasouli, K. Endo, J. F. Chen, N. Singh, and K. Banerjee* 2282
Statistical Threshold-Voltage Variability in Scaled Decananometer Bulk HKMG MOSFETs: A Full-Scale 3-D Simulation Scaling Study . . . . *X. Wang, A. R. Brown, N. Idris, S. Markov, G. Roy, and A. Asenov* 2293
Compact Modeling of Variability Effects in Nanoscale NAND Flash Memories . . . . . . *A. Spessot, C. M. Compagnoni, F. Farina, A. Calderoni, A. S. Spinelli, and P. Fantini* 2302
Low-Frequency Noise Investigation and Noise Variability Analysis in High-k/Metal Gate 32-nm CMOS Transistors . . . . *D. Lopez, S. Haendler, C. Leyris, G. Bidal, and G. Ghibaudo* 2310
Investigation on Variability in Metal-Gate Si Nanowire MOSFETs: Analysis of Variation Sources and Experimental Characterization . . . . *R. Wang, J. Zhuge, R. Huang, T. Yu, J. Zou, D.-W. Kim, D. Park, and Y. Wang* 2317
On the Variability in Planar FDSOI Technology: From MOSFETs to SRAM Cells . . . . . . *J. Mazurier, O. Weber, F. Andrieu, A. Toffoli, O. Rozeau, T. Poiroux, F. Allain, P. Perreau, C. Fenouillet-Beranger, O. Thomas, M. Belleville, and O. Faynot* 2326
A Three-Dimensional Physical Model for $V_{\rm th}$ Variations Considering the Combined Effect of NBTI and RDF . . . . . *G. D. Panagopoulos and K. Roy* 2337
Impact of Hot Carriers on nMOSFET Variability in 45- and 65-nm CMOS Technologies . . . . . . *P. Magnone, F. Crupi, N. Wils, R. Jain, H. Tuinhout, P. Andricciola, G. Giusi, and C. Fiegna* 2347

Silicon and Column IV Semiconductor Devices

Reduction of Fixed-Position Noise in Position-Sensitive Single-Photon Avalanche Diodes . . . . . . *M. W. Fishburn, Y. Maruyama, and E. Charbon* 2354
Impact of Ge Content and Recess Depth on the Leakage Current in Strained $Si_{1-x}Ge_x/Si$ Heterojunctions . . . . . . *A. Luque Rodríguez, M. Bargallo Gonzalez, G. Eneman, C. Claeys, D. Kobayashi, E. Simoen, and J. A. Jiménez Tejada* 2362
Novel Capacitorless 1T-DRAM Cell for 22-nm Node Compatible With Bulk and SOI Substrates. . . . . . *N. Rodriguez, S. Cristoloveanu, and F. Gamiz* 2371
Performance Assessment of Nanoscale Field-Effect Diodes . . . . . . *N. Manavizadeh, F. Raissi, E. A. Soleimani, M. Pourfath, and S. Selberherr* 2378
Drain Current Collapse in Nanoscaled Bulk MOSFETs Due to Random Dopant Compensation in the Source/Drain Extensions. . . . . . *S. Markov, X. Wang, N. Moezi, and A. Asenov* 2385
Optimization of Germanium (Ge) n^+/p and p^+/n Junction Diodes and Sub 380 °C Ge CMOS Technology for Monolithic Three-Dimensional Integration . . . . . . *J.-H. Park, D. Kuzum, H.-Y. Yu, and K. C. Saraswat* 2394
Modeling and Design of Ferroelectric MOSFETs . . . . . . *H.-P. Chen, V. C. Lee, A. Ohoka, J. Xiang, and Y. Taur* 2401
Threshold-Voltage Instability Due to Damage Recovery in Nanoscale NAND Flash Memories . . . . . . *C. Miccoli, C. Monzio Compagnoni, S. Beltrami, A. S. Spinelli, and A. Visconti* 2406
A Quantitative Error Analysis of the Mobility Extraction According to the Matthiessen Rule in Advanced MOS Transistors . . . . . . *D. Esseni and F. Driussi* 2415
Thermionic Field Emission Explanation for Nonlinear Richardson Plots . . . . . . *C. Kenney, K. C. Saraswat, B. Taylor, and P. Majhi* 2423
Technology Assessment Methodology for Complementary Logic Applications Based on Energy–Delay Optimization . . . . . . *L. Wei, S. Oh, and H.-S. P. Wong* 2430
Degradation Model of Self-Heating Effects in Silicon-on-Glass TFTs . . . . . . *M. Mativenga, M. H. Choi, J. Jang, R. Mruthyunjaya, T. J. Tredwell, E. Mozdy, and C. Kosik-Williams* 2440
Electrical Degradation and Recovery of Low-Temperature Polycrystalline Silicon Thin-Film Transistors in Polycrystalline Silicon Plasma Process . . . . . . *J.-J. Chang, K.-S. Chang-Liao, T.-K. Wang, Y.-C. Wu, K.-C. Lin, C.-Y. Chen, Y.-M. Chen, J.-P. Tseng, and M.-F. Hung* 2448
Noniterative Compact Modeling for Intrinsic Carbon-Nanotube FETs: Quantum Capacitance and Ballistic Transport . . . . . . *L. Wei, D. J. Frank, L. Chang, and H.-S. P. Wong* 2456
Three-Dimensional $4F^2$ ReRAM with Vertical BJT Driver by CMOS Logic Compatible Process . . . . . . *C.-H. Wang, Y.-H. Tsai, K.-C. Lin, M.-F. Chang, Y.-C. King, C. J. Lin, S.-S. Sheu, Y.-S. Chen, H.-Y. Lee, F. T. Chen, and M.-J. Tsai* 2466
Multi-V_T UTBB FDSOI Device Architectures for Low-Power CMOS Circuit . . . . . . *J.-P. Noel, O. Thomas, M.-A. Jaud, O. Weber, T. Poiroux, C. Fenouillet-Beranger, P. Rivallin, P. Scheiblin, F. Andrieu, M. Vinet, O. Rozeau, F. Boeuf, O. Faynot, and A. Amara* 2473

(Contents Continued on Page 2187)

(Contents Continued from Page 2186)

Explanation of the Charge-Trapping Properties of Silicon Nitride Storage Layers for NVM Devices Part I: Experimental Evidences From Physical and Electrical Characterizations . . . . *E. Vianello, F. Driussi, L. Perniola, G. Molas, J.-P. Colonna, B. De Salvo, and L. Selmi* 2483
Explanation of the Charge Trapping Properties of Silicon Nitride Storage Layers for NVMs—Part II: Atomistic and Electrical Modeling . . . . . . *E. Vianello, F. Driussi, P. Blaise, P. Palestri, D. Esseni, L. Perniola, G. Molas, B. De Salvo, and L. Selmi* 2490
High-Density 3-D Interconnect of Cu–Cu Contacts With Enhanced Contact Resistance by Self-Assembled Monolayer (SAM) Passivation . . . . *L. Peng, H. Li, D. F. Lim, S. Gao, and C. S. Tan* 2500
Simulation of the Electron Transport in a Mott Diode by the Monte Carlo Method . . . . *S. V. Obolensky, A. V. Murel, N. V. Vostokov, and V. I. Shashkin* 2507
Junctionless Multiple-Gate Transistors for Analog Applications . . . . *R. T. Doria, M. A. Pavanello, R. D. Trevisoli, M. de Souza, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, A. Kranti, and J.-P. Colinge* 2511
Implicit Continuous Current–Voltage Model for Surrounding-Gate Metal–Oxide–Semiconductor Field-Effect Transistors Including Interface Traps . . . . *Y. S. Yu, N. Cho, S. W. Hwang, and D. Ahn* 2520
Device Simulation for Evaluating Effects of Inplane Biaxial Mechanical Stress on n-Type Silicon Semiconductor Devices . . . . *M. Koganemaru, K. Yoshida, T. Ikeda, N. Miyazaki, and H. Tomokage* 2525
Electroforming of Amorphous Silicon Nitride Heterojunction *pin* Visible Light Emitter . . . . *M. Anutgan, T. Anutgan, I. Atilgan, and B. Katircioglu* 2537
Layout Scaling of $Si_{1-x}Ge_x$-Channel pFETs . . . . *G. Eneman, S. Yamaguchi, C. Ortolland, S. Takeoka, M. Kobayashi, L. Witters, A. Hikavyy, J. Mitard, R. Loo, T. Hoffmann* 2544

Compound Semiconductor Devices

Peculiarities of Surface Breakdown in GaAs Bipolar Junction Structures . . . . *G. Duan, S. N. Vainshtein, and J. T. Kostamovaara* 2551
Optimal Filling of the Intermediate Band in Idealized Intermediate-Band Solar Cells . . . . *R. Strandberg and T. Worren Reenaas* 2559
Trends in Submicrometer InP-Based HBT Architecture Targeting Thermal Management . . . . *B. Grandchamp, V. Nodjiadjim, M. Zaknoune, G. A. Koné, C. Hainaut, J. Godin, M. Riet, T. Zimmer, and C. Maneux* 2566
An Investigation of DC and RF Safe Operating Area of n-p-n + p-n-p SiGe HBTs on SOI . . . . *P. Cheng, S. Seth, J. D. Cressler, G. Cestra, T. Krakowski, J. A. Babcock, and A. Buchholz* 2573
Influence of a Barrier Layer on the Formation of AuBe Ohmic Contact With the p-GaAs Bases of Heterojunction Bipolar Transistors . . . . *Q. Xu and L.-W. Yang* 2582
Transport Studies of AlGaN/GaN Heterostructures of Different Al Mole Fractions With Variable SiN_x Passivation Stress . . . *T. B. Fehlberg, J. S. Milne, G. A. Umana-Membreno, S. Keller, U. K. Mishra, B. D. Nener, and G. Parish* 2589
Experimental Study of $\langle 110 \rangle$ Uniaxial Stress Effects on p-Channel GaAs Quantum-Well FETs . . . . *L. Xia, V. Tokranov, S. R. Oktyabrsky, and J. A. del Alamo* 2597
InP DHBT-Based IC Technology for 100-Gb/s Ethernet . . . . *R. Driad, J. Rosenzweig, R. E. Makon, R. Lösch, V. Hurm, H. Walcher, and M. Schlechtweg* 2604

Thin Film Devices

Transport Physics and Device Modeling of Zinc Oxide Thin-Film Transistors Part I: Long-Channel Devices . . . . *F. Torricelli, J. R. Meijboom, E. Smits, A. K. Tripathi, M. Ferroni, S. Federici, G. H. Gelinck, L. Colalongo, Z. M. Kovacs-Vajna, D. de Leeuw, and E. Cantatore* 2610
Integration of Solar Cells on Top of CMOS Chips—Part II: CIGS Solar Cells . . . . *J. Lu, W. Liu, A. Y. Kovalgin, Y. Sun, and J. Schmitz* 2620
Charge-Based Modeling of Junctionless Double-Gate Field-Effect Transistors . . . . *J.-M. Sallese, N. Chevillon, C. Lallement, B. Iñiguez, and F. Prégaldiny* 2628
Protrusions of Super Grains Formed by Ultrashort Xe Flash-Lamp Annealing of Amorphous Silicon and Its Effect on the Performances of Thin-Film Transistors . . . . *S. Saxena and J. Jang* 2638
Inclusion of the Accumulation Region in the Compact Models of Bulk and SOI FinFETs . . . . *G. Dessai and G. Gildenblat* 2644

Optoelectronics, Displays, and Imaging

Lifetime Amelioration for an AMOLED Pixel Circuit by Using a Novel AC Driving Scheme . . . . *C.-L. Lin, K.-W. Chou, C.-C. Hung, and C.-D. Tu* 2652
Evaluation of a Surface-Channel CCD Manufactured in a Pinned Active-Pixel-Sensor CMOS Process . . . . *J. Borg and J. Johansson* 2660

(Contents Continued on Page 2188)

(Contents Continued from Page 2187)

Solid-State Power and High Voltage Devices

High-Voltage (2.8 kV) Implantation-Free 4H-SiC BJTs With Long-Term Stability of the Current Gain . . . . *R. Ghandi, B. Buono, M. Domeij, C.-M. Zetterling, and M. Östling* 2665

Modeling and Evaluation of Carbon-Nanotube-Based Integrated Power Inductor for On-Chip Switching Power Converters . . . . . . *O. F. Mousa and J. A. Abu Qahouq* 2670

Materials, Processing, and Packaging

Polyimide-Enhanced Stretchable Interconnects: Design, Fabrication, and Characterization . . . . . . *Y.-Y. Hsu, M. Gonzalez, F. Bossuyt, J. Vanfleteren, and I. De Wolf* 2680

Carbon Nanotube Vias: Does Ballistic Electron-Phonon Transport Imply Improved Performance and Reliability? . . . *H. Li, N. Srivastava, J.-F. Mao, W.-Y. Yin, and K. Banerjee* 2689

Carbon Nanotubes Bundled Interconnects: Design Hints Based on Frequency- and Time-Domain Crosstalk Analyses . . *A. Giustiniani, V. Tucci, and W. Zamboni* 2702

Estimation of Time Delay and Repeater Insertion in Multiwall Carbon Nanotube Interconnects . . . . . . *F. Liang, G. Wang, and W. Ding* 2712

Solid-State Device Phenomena

The Relation Between Degradation Under DC and RF Stress Conditions . . . . . . *A. J. Scholten, D. Stephens, G. D.J. Smit, G. T. Sasse, and J. Bisschop* 2721

An Electronic Synapse Device Based on Metal Oxide Resistive Switching Memory for Neuromorphic Computation . . . *S. Yu, Y. Wu, R. Jeyasingh, D. Kuzum, and H.-S. P. Wong* 2729

Impact of ZnO Polarization on the Characteristics of Metal–Ferroelectric–ZnO Field Effect Transistor . . . . . . *Q. Tan, J. Wang, X. Zhong, Y. Zhou, Q. Wang, Y. Zhang, X. Zhang, and S. Huang* 2738

Statistical Model for MOSFET Bias Temperature Instability Component Due to Charge Trapping . . . . . . *G. I. Wirth, R. da Silva, and B. Kaczer* 2743

Characterization of Border Trap Density With the Multifrequency Charge Pumping Technique in Dual-Layer Gate Oxide . . . . . . *Y. Son, S. Park, T. Kang, B. Oh, and H. Shin* 2752

Molecular and Organic Devices

Series-Connection Designs for Dye Solar Cell Modules . . . . . . *F. Giordano, E. Petrolati, T. M. Brown, A. Reale, and A. Di Carlo* 2759

Complementary Ring Oscillator Exclusively Prepared by Means of Gravure and Flexographic Printing . . . . . . *H. Kempa, M. Hambsch, K. Reuter, M. Stanel, G. C. Schmidt, B. Meier, and A. C. Hübler* 2765

Sensors and Actuators

Transduction of High-Frequency Micromechanical Resonators Using Depletion Forces in p-n Diodes . . . . . . *E. Hwang and S. A. Bhave* 2770

Vacuum Electron Devices

Operation of a Continuously Frequency-Tunable Second-Harmonic CW 330-GHz Gyrotron for Dynamic Nuclear Polarization . . . . . . *A. C. Torrezan, M. A. Shapiro, J. R. Sirigiri, R. J. Temkin, and R. G. Griffin* 2777

Thermal Analysis of a Strapped Magnetron . . . . . . *M. A. Sattorov, A. Bera, A. Sharma, W.-J. Kang, O.-J. Kwon, S.-S. Jung, D.-H. Kim, K. W. Lee, J.-H. Won, C. H. Kook, and G.-S. Park* 2784

Development of an S-band 22-kW-Average-Power-Klystron With 7.14% Relative Bandwidth . . . . . . *Z. Zhang, B. Shen, X. Yu, F. Zhu, Y. Han, Y. Huang, and F. Zhang* 2789

BRIEFS

Empirical Modeling and Extraction of Parasitic Resistance in Amorphous Indium–Gallium–Zinc Oxide Thin-Film Transistors . . . . . . *J.-H. Park, H.-K. Jung, S. Kim, S. Lee, D. M. Kim, D. H. Kim* 2796

Total Ionizing Dose (TID) Effects on TaO_x-Based Resistance Change Memory . . . . . . *L. Zhang, R. Huang, D. Gao, P. Yue, P. Tang, F. Tan, Y. Cai, and Y. Wang* 2800

Anomalous Dependence of Threshold Voltage Mismatch of Short-Channel Transistors . . . . . . *T. B. Hook, J. B. Johnson, and J. Shah* 2805

Supply-Voltage Scaling Close to the Fundamental Limit Under Process Variations in Nanometer Technologies . . . . . . *M.-E. Hwang* 2808

A Novel Sensing Scheme for Reliable Read Operation of Ultrathin-Body Vertical NAND Flash Memory Devices . . . . . . *S. Cho and B.-G. Park* 2814

(Contents Continued on Page 2189)

(Contents Continued from Page 2188)

CORRESPONDENCE

Erratum: Analytic Model for the Surface Potential and Drain Current in Negative Capacitance Field-Effect Transistors . . . . *D. Jiménez, E. Miranda, and A. Godoy* 2818

ANNOUNCEMENTS

Call for Papers—Special Issue of IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY on Materials, Processing, and Reliability of 3D Interconnects 2819
Announcing EDS Early Career Award 2820

About the Cover: Figure on the cover represents the electron density distribution in 35 nm device, simulated with random discrete dopants (RDD), line edge roughness (LER), and metal gate granularity (MGG) as sources of variability. The blue and red colors correspond to the electron densities of 10^5 cm^{-3} and 10^{20} cm^{-3}, respectively. The different sources of variability result in several order of magnitudes electron concentration variation in the channel region. The surface indicates the potential landscape with the evidence of variability effects. The figure with more details appears in the paper by Wang *et al*. that begins on page 2293 of this Special Issue.

Foreword
Special Issue on Characterization of Nano CMOS Variability by Simulation and Measurements

THIS Special Issue presents significant results from recent research studies on the "Characterization of Nano CMOS Variability by Simulation and Measurements." Due to the continuous scaling of the transistor dimensions and the rapid introduction of the 32-nm and 22-nm technology nodes, the variability of transistor characteristics has become a major concern associated with the further scaling and integration of CMOS. Variability already critically affects SRAM scaling and introduces leakage and timing issues in digital logic circuits. Variability is the main factor restricting scaling of the supply voltage, which for the last four technology generations has remained virtually constant and thereby has added to the power crisis. In addition to this increasing variability, the looming challenges that arise from the statistical aspects of reliability threaten to dramatically reduce the life span of integrated circuits and systems in the near future. The physical and compact modeling of variability and the statistical aspects of reliability, together with their requirements for comprehensive characterization, have been highlighted in the 2008 and 2010 updates of the International Technology Roadmap for Semiconductors and in the 2008 European Nanoelectronics Initiative Advisory Council (ENIAC) Joint Technology Initiative (JTI) Multi-annual Strategic Plan. These topics have also received particular attention in the recent European FP7 Cooperation Project named "Silicon-based nanostructures and nanodevices for long-term nanoelectronics applications" (NANOSIL FP7 IST-216171) that is cited by several papers in this Special Issue.

The simulation and characterization of variability have become extremely important in terms of understanding the current variability mechanisms and sources. They are also used for predicting the levels of variability in future technology generations involving conventional and novel nanoscale CMOS devices such as biosensors and other devices used in more than Moore applications of nanoelectronics. Many semiconductor industry stakeholders now accept that variability and statistical reliability requirements will transform the way circuits and systems are designed in the future. In addition, reliable statistical compact models based on predictive physical simulations will be critical for designing these systems.

In view of the increasing importance of this area that involves new materials, devices, circuits, modeling tools, characterization techniques, and associated international standards, the aim of this Special Issue is to bring together recent advances in the "Characterization of Nano CMOS Variability by Simulation and Measurements" and present them to the device- and design-oriented academic and industrial communities, as represented by the readers of the IEEE TRANSACTIONS ON ELECTRON DEVICES.

This Special Issue consists of 16 carefully selected papers, i.e., 5 invited papers (one of which has two parts) and 11 contributed papers, that discuss topics such as process variation, device variability, hierarchical modeling tools, and address challenges such as device mismatch and SRAM noise margin variability. The Special Issue starts with the five invited papers.

Highlights from the 5 invited papers:

1) In "Process Technology Variation," Kuhn *et al.* discuss the importance of process variation in modern CMOS transistor technology, review front-end variation sources, present device and circuit variation measurement techniques, and compare recent intrinsic transistor variation performance reported in the literature.
2) In "Quantum transport study on the Impact of Channel Length and Cross-section on Variability Induced by Random Discrete Dopants in Narrow Gate-all-around Silicon Nanowire Transistors," Martinez *et al.* review and extend recent work on the effect of random discrete dopants on the statistical variability in gate-all-around silicon nanowire transistors. The authors use the nonequilibrium Green's function formalism and full 3-D real-space and coupled-mode-space representations.
3) In "Hierarchical Simulation of Process Variations and their Impact on Circuits and Systems: Methodology (Part I) and Results (Part II)," Lorenz *et al.* discuss in Part I the sources of process variations and the state-of-the-art related simulation tools with their hierarchical structure. In Part II, they present examples of hierarchical simulation results obtained with the methodology described in Part I.
4) In "Characterization and Modeling of Transistor Variability in Advanced CMOS Technologies," Mezzomo *et al.* review their results on the characterization and modeling of transistor mismatch in advanced CMOS technologies. They begin with a review of the theoretical background and modeling approaches for analyzing and interpreting the mismatch results. Next, they discuss the experimental procedures and methodologies for characterizing transistor matching. Finally, they present typical matching results obtained on modern CMOS technologies with the main variability (mismatch) sources.
5) In "Direct Measurement of Correlation between SRAM Noise Margin and Individual Cell Transistors Variability by Using Device-Matrix-Array," Hiramoto *et al.* present direct measurements of noise margin, characteristics of

Digital Object Identifier 10.1109/TED.2011.2160884

0018-9383/$26.00 © 2011 IEEE

six individual cell transistors, and their variability in SRAM cells using a special device-matrix-array test element group of 16-Kbit SRAM cells. Their results indicate that the circuit simulation with only the threshold variability taken into account will not predict SRAM stability precisely at low supply voltage.

We arranged the 11 contributed papers into two groups as follows: 1) New Model Developments and 2) Characterization and Reliability Aspects of Variability.

Group 1: New Model Developments

This group of six papers covers new model developments, including process, device, and compact models, devoted to variability.

1) In "Statistical Enhancement of the Evaluation of Combined RDD and LER-Induced V_T Variability: Lessons from 10^5 Sample Simulations," Reid *et al.*, report on the statistical threshold voltage variability in a state-of-the-art n-Channel MOSFET. They are the first to include the combined effect of random discrete dopants and line-edge roughness and demonstrate that the resulting distribution is nonnormal. They are able to analyze up to 100 000 devices by deploying computationally efficient statistical enhancement techniques.
2) In "An approach based on sensitivity analysis for the evaluation of process variability in nanoscale MOSFETs," Bonfiglio *et al.* propose an interesting approach to evaluate the effects of line-edge roughness, surface roughness, and random dopant distribution on the threshold voltage dispersion in nanoscale MOSFETs. They use parameter sensitivity analyses performed by means of a limited number of technology computer-aided design simulations or analytical modeling.
3) In "A comparative study of surface-roughness-induced variability in silicon nanowire and double-gate FETs," Pala *et al.*, present a full quantum analysis based on the 3-D self-consistent solution of the Poisson–Schrödinger equation within the nonequilibrium Green's function formalism and solved with a coupled-mode-space approach. They use this approach to calculate the effect of surface roughness at the Si/SiO2 interfaces on transport properties of quasi-1-D- and quasi-2-D-silicon nanodevices by comparing the electrical performances of nanowire and double-gate FETs.
4) In "Grain-Orientation Induced Quantum Confinement Variation in Multi-Gate Ultra-Thin Body CMOS Devices and Implications for Digital Circuit Design," Rasouli *et al.* identify a new source of random threshold voltage variation, i.e., "grain-orientation induced quantum confinement" in emerging ultrathin body metal-gate CMOS devices. These effects arise from the dependence of the work function of the metal gates on the grain orientations and cause different parts of the gate in multigate CMOS devices to feature different work-function values.
5) In "Statistical Threshold-Voltage Variability in Scaled Deca-Nanometer Bulk HKMG MOSFETs: a Fully Scaled 3D Simulation Scaling Study," Wang *et al.* present a comprehensive fully scaled 3-D simulation scaling study of the statistical threshold voltage variability in bulk high-κ/metal-gate (HKMG) MOSFETs with gate lengths down to 13 nm. They include metal-gate granularity and the corresponding work-function-induced threshold voltage variability, which have become important sources of statistical variability in bulk HKMG MOSFETs.
6) In "Compact Modeling of Variability Effects in Nanoscale NAND Flash Memories, " Spessot *et al.* present a thorough investigation of the main variability effects in nanoscale NAND Flash memory devices and consider their impact on device operation by means of a statistical compact model for the memory array.

Group 2: Characterization and Reliability Aspects of Variability

The final five papers cover several characterization and reliability aspects of variability.

1) In "Low Frequency Noise Investigation and Noise Variability Analysis in High-κ Metal Gate 32nm CMOS Transistors," Lopez *et al.* report on the low-frequency noise (LFN) of high-κ/metal stack n- and p-MOS transistors. Their results obtained on the 32-nm CMOS technology, including LFN spectra, indicate that carrier number fluctuation is the main noise source for both n- and p-MOS devices.
2) In "Investigation on Variability in Metal-Gate Si Nanowire MOSFETs: Analysis of Variation Sources and Experimental Characterization," Wang *et al.* study the characteristic variability in gate-all-around Si nanowire (NW) MOSFETs and include detailed discussions on specific sources of NW cross-sectional shape variation, random dopant fluctuation in NW source/drain extension regions, and NW line-edge roughness.
3) In "On the Variability in Planar FDSOI Technology: From MOSFETs to SRAMs," Mazurier *et al.* report a variability analysis of MOSFET threshold voltage (Vth) on static random access memory devices noise margin in fully depleted silicon-on-insulator technology and demonstrate a very low Vth variability.
4) In "A 3-D Physical Model for Vth Variations Considering the Combined Effect of NBTI and RDF," Panagopoulos *et al.* use the stochastic differential equation to investigate the combined effects of random dopant fluctuation and negative bias temperature instability due to hot carriers on Vth.
5) In "Impact of Hot Carriers on n-MOSFET variability in 45 nm and 65 nm CMOS Technologies," Magnone *et al.* examine the impact of hot carriers (HCs) on n-channel metal–oxide–semiconductor (MOS) field-effect transistor mismatch across the 45-nm and 65-nm complementary MOS technology generations. Their reported statistical analysis is based on a large overall sample population of about 1000 transistors. They find that HC stress becomes a source of variability in device electrical parameters due to the randomly generated charge traps in the gate dielectric or at the substrate/dielectric interface.

Acknowledgment

The members of the IEEE Electron Devices Society (EDS) Technology Computer-Aided Design Technical Committee and guest editors for this Special Issue would like to thank the

authors for their work in submitting and revising their manuscripts. We would also wish to express our deepest gratitude to our reviewers for their efforts and dedication. This issue would not have been possible without their expert advice. The supporting and patient work from J. A. Marsh of the EDS Office is also deeply appreciated.

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Mr. Sangiorgi is a Fellow of the IEEE, Distinguished Lecturer of the Electron Device Society, Chairman of the Electron Device Society Technology Computer-Aided Design Technical Committee. From 1994 to 2009, he was an Editor of IEEE ELECTRON DEVICE LETTERS. He has been a Guest Editor of several special issues on major scientific journals such as IEEE TRANSACTIONS ON ELECTRON DEVICES and SOLID-STATE ELECTRONICS. He has been a member of the Technical Committees of several International Conferences on Electron Devices: International Electron Devices Meeting ('91–96; '04–'06), European Solid-State Device Research Conference ('99-present), INFOS ('95-03), ULIS ('00–'08), etc. He has been involved in several European Projects of the 5, 6, and now 7 FP with management responsibilities, and he has acted as a Project Reviewer for the European Commission.

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Dr. Dutton has published more than 200 journal articles and has been able to teach more than four dozen doctorate students and made them graduate. He was an Editor of the IEEE CAD Journal (1984–1986). He was elected to the National Academy of Engineering in 1991. He was a recipient of the 1987 IEEE J. J. Ebers and the 1996 Jack Morton Awards, the 1988 Guggenheim Fellowship to study in Japan, the C&C Prize (Japan) in 2000, the Career Achievement Award (2005) from the Semiconductor Industry Association (SIA) for sustained contributions in support of research that is critical to SIA needs, the Phil Kaufman Award in 2006, and the IEEE Education Award in 2008.

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