Circuit simulation of workload-dependent RTN and BTI based on trap kinetics

V.V.A. Camargo [a], B. Kaczer [b], T. Grasser [c], G. Wirth [a],*

[a] Universidade Federal do Rio Grande do Sul—UFRGS, Porto Alegre 90035-190, Brazil
[b] IMEC, Leuven B-3001, Belgium
[c] TU Wien, Vienna A-1040, Austria

ABSTRACT

A simulation methodology is presented capable of evaluating the transient impact of trap kinetics in transistors at the circuit level and thus the effects caused by them, particularly Random Telegraph Noise (RTN) and Bias Temperature Instability (BTI). The downscaling of channel area leads to transistors with a smaller number of traps, but each trap causing a larger impact on the transistor's electrical parameters, increasing its importance in circuit reliability. Despite the increasing impact of these effects on circuit reliability there are still no Computer-Aided Design (CAD) tools capable of analyzing the trapping kinetics and the methodologies presented in the literature suffer from either lack of computational efficiency or accuracy. This paper presents a comprehensive trap simulation methodology relying on both theoretical evaluations and experimental device characterization. The developed simulation framework performs a transient SPICE simulation on an arbitrary design considering the trap activity in situ, allowing accurate simulations of both RTN and BTI effects, at DC, AC or arbitrarily changing bias conditions. In order to perform statistical simulations, the simulation framework may be run inside a Monte Carlo loop. Case studies on a SRAM and on a ring oscillator are performed considering the workload dependence and the BTI effect during the simulation.

© 2014 Elsevier Ltd. All rights reserved.

1. Introduction

Charge trapping and de-trapping at localized states at the interface or in the gate dielectric is a significant reliability issue in state of the art CMOS applications. It is known to be a source of low-frequency noise, and also considerably contributes to the Bias Temperature Instability (BTI) [1–7]. These localized states are known as traps. Trapping and de-trapping are stochastic events, and a trap may be either populated or empty. A trap becomes populated when capturing a charge carrier and becomes empty after emitting it. These capture and emission events dynamically impact the electrical parameters of the transistor, generating time dependent reliability issues at the circuit level.

According to the characteristics of each trap it may impact the MOS transistor in a different way [1]. If a trap is more likely to capture a carrier than to emit it, this trap will tend to remain occupied, producing an aging effect. BTI is an aging phenomenon attributed to this trap activity effect [2]. On the other hand, a trap which is equally likely to capture and to emit carriers will likely change its state frequently generating a noise effect. This effect is known as Random Telegraph Signal (RTS) or Random Telegraph Noise (RTN).

To first order, the impact of a trapped carrier at the Si/SiO$_2$ interface or in the oxide on the electrical behavior of the transistor is inversely proportional to the channel area [3]. The miniaturization of the transistor's channel, hence, leads to an increase of the relevance of charge trapping and de-trapping phenomena. Furthermore, Random Dopant Fluctuations (RDF) will induce percolation paths, further increasing the impact of a single trap and leading to variability issues in circuit electrical response [22]. Another trend is the increase of the nominal threshold voltage and/or the decrease of the operation voltage, aiming to reduce the power consumption. When combining these effects, the increase of the impact of trap activity on transistor variability becomes evident, leading to serious circuit reliability issues. Atomistic (TCAD) simulation results show that the impact of a single trap on a 45 nm channel length transistor might cause an increase as high as 16% on the device threshold voltage [4], these kind of simulation, however, cannot be used to study the traps impact in circuits with more than a couple of transistor due to its computational cost.

As RTN has become a critical effect for circuit reliability, its impact on circuits has been widely investigated. Traditionally RTN was evaluated only in the frequency domain, therefore the circuit analysis techniques to evaluate the RTN impact on circuits were developed based on frequency domain analysis [5]. For digital and low power applications, however, it is of most interest to make studies in the time-domain [6], but to the moment there are still no commercial Spice tools available that allows this kind of simulation.

Recently many authors presented simulation methodologies capable to simulate RTN effect on transient Spice analysis thus allowing the investigation of its impact on circuit level. A cyclo-stationary simulation method for RTN was first presented by Van Der Wel in 2003 [8] and further developed by Kolhatkar [9] and Wirth et al. [10,11]. Other simulation methodologies were developed at the electrical level (Spice level). These methodologies are based on (i) equivalent electrical models for each trap [6,12], where trap behavior is modeled by equivalent circuits or (ii) in evaluating the trap activity outside the electrical simulation tool in a single simulation as in [13] and in MUSTARD [14], or in multiple simulations as in SAMURAI [14] aiming to consider the bias dependency.

The goal of this kind of simulation is to obtain a reliable result for circuit simulations considering the trap activity on transient simulations. A cyclo-stationary simulator can be used to perform case studies on specific circuits that might give insights to designers in order to develop newer, more reliable design techniques, and also to evaluate the traps impact on small critical blocks widely used on designs such as SRAM cells, ring oscillators and analog blocks. Another possible use of this kind of simulations is to provide a golden simulation result for the developing of more computing efficient CAD tools that would be used during the design of large real circuits, such SSTA tools.

So far, the methodologies presented in the literature are either not accurate enough because they do not support models which depends on the bias conditions or are not computationally efficient, becoming unviable to run Monte Carlo simulations on realistic circuits under usual switching conditions. The existing methodologies also were focused on considering just RTN neglecting other effects caused by the trap activity, such as BTI.

This manuscript presents in depth a circuit simulation methodology capable of performing workload dependent trap simulations in the time-domain on arbitrary circuit designs under arbitrary bias conditions. It is thus capable to evaluate the effects caused by the traps, such as BTI and RTN, at the circuit level. As many studies on the trap kinetics and its impact on transistors are still being made, many new models and enhancements to previous models, which may be more suitable for different technology nodes, are still being developed. On this kind of simulation, the complexity of the model is tightly attached to the computational cost of the simulation. The methodology presented in this manuscript was developed so that the model used by the simulation tool can be easily changed, thus allowing the user to choose the model that best fits their needs.

This work first presents the model of trap kinetics which is used in the case studies, then the simulation tool developed is presented and case studies on an inverter, on a ring oscillator and on a SRAM cell are presented and discussed. Finally a conclusion section is presented summarizing the main contributions of this work.

2. Trap kinetics model

Oxide and interface traps capture and emit charge carriers responsible for the drain current of the MOSFET. When a trap captures a charge carrier, the drain current is affected due to the electrostatic effect, which leads to reduction in number of carriers in the channel and also affects mobility. This is here modeled as a V_T fluctuation.

For a constant bias condition i.e., in a steady state condition, the traps whose energy level is close to the Fermi level will present larger activity. By changing the transistor's bias point, the difference between the trap's energy level and the Fermi level is also changed, thus changing the occupation probability of the trap [15]. Responding to this change, the traps tend to change their states, adapting to the new occupation probability. However this change is not instantaneous but a function of the time constants of each trap. The same model can be used to describe the charge trapping activity, both for steady state (DC) condition as well as for arbitrary bias conditions [16].

Capture and emission of a charge carrier by a trap is modeled as a Poisson processes with rates τ_c and τ_e. State 1 stands for the populated trap, while state 0 stands for the empty trap. τ_c and τ_e are then the average residence times in states 0 and 1 in a steady state condition, respectively [17].

Eqs. (1) and (2) shown the probability of a particular trap to change its state after an elapsed time Δt [16].

$$P_{01}(\Delta t) = \left[1 - \exp\left(\frac{-\Delta t}{\tau_{eq}}\right)\right] \cdot \frac{\tau_e}{(\tau_c + \tau_e)} \tag{1}$$

$$P_{10}(\Delta t) = \left[1 - \exp\left(\frac{-\Delta t}{\tau_{eq}}\right)\right] \cdot \frac{\tau_c}{(\tau_c + \tau_e)} \tag{2}$$

where $1/\tau_{eq} = 1/\tau_c + 1/\tau_e$.

Eqs. (1) and (2) can be summarized into Eq. (3). The bias point condition and the process are included in the time constant parameter. For our circuit simulation in the time domain, the Δt in Eq. (3) is defined as the time step of the simulation, 'p' is the process, either capture ('c') or emission ('e'), 'v' is the bias condition on that given instant of time and τ is the trap time constant. The bar indicates the complementary process.

$$P_{p,v} = \frac{\tau_{\bar{p},v}}{\tau_{e,v} + \tau_{c,v}} \left\{1 - \exp\left[-\left(\frac{1}{\tau_{e,v}} + \frac{1}{\tau_{c,v}}\right)\Delta t\right]\right\} \tag{3}$$

These equations apply to any bias condition. However, as depicted by Fig. 13 in [18], the time constants are a function of the bias point. This dependency is included in the model by a numerical fitting algorithm which aims at finding the correct value of the time constants for a given bias point from known time constants defined for a known bias point.

For the emission time, the simulator is fed with two parameters, $\tau_{e;min}^{1'}$ and $\tau_{e;min}^{2'}$, which are defined in [18]. The emission time used during the simulations is given by Eq. (4). For the capture time, the simulator is fed with the capture time for two different gate voltages in the range of operation of the device. Using a linear approximation on the log-scale, the capture time of this given trap is calculated for the other gate voltages. The linear approximation presented to be satisfactory for electric fields in the range of 1–6MV/cm as shown in Fig. 13 in [18]. For a more accurate, but more computing cost simulation, the voltage dependency model can be changed to follow the model presented in [18].

$$\tau_e = \begin{cases} \tau_{e;min}^{1'} & V_g \leqslant V_T \\ \tau_{e;min}^{2'} & V_g > V_T \end{cases} \tag{4}$$

3. Simulation framework

This section presents the simulator framework developed and used in this study. Because not only the charge trapping kinetics are a stochastic phenomenon but also the number of traps and their properties are described as random variables, the simulation framework is decomposed into two different levels. One level

evaluates the trap activity during the electrical simulation and the other one controls the simulation flow externally.

In order to include the impact of the trap activity into the electrical simulator, the transistor model used in the simulations was enhanced by adding the trap kinetics equations presented in Section 2. This enhancement was performed by creating a Verilog-A component which contains the BSIM4 description [19]. The Verilog-A standard provides a flexible way to model devices and integrate new models into electrical simulations [20].

All the information regarding the trap properties for a given technology are included in a configuration file. This file also contains the information about the running options, such as the number of runs on a Monte Carlo Simulation, and analysis options, such as if time zero variability is to be considered in the analysis.

The input parameters for each instance of the Verilog-A component are: (i) number of traps for each transistor in the circuit; (ii) the time constants for each trap; (iii) the impact of each trap on the threshold voltage (when populated); (iv) the parameters that define the dependence of capture and emission probability on temperature and bias point, for each trap; and (v) the initial state of each trap. All these parameters are defined by the control script based on the configuration file information. The values of the parameters are defined for each instance prior to each electrical simulation.

Once that every instance has all of its parameters defined, the electrical simulation is performed. At each time step of the transient simulation, Eq. (3) is used to evaluate the probability of the trap to change its state. Based on this information the trap's next state is randomly defined. For each populated trap, its impact on V_T is added to the threshold voltage parameter of the transistor model.

The impact on V_T caused by each trap is considered to be a constant value independent of bias and temperature. Even though recent studies show that the trap's impact on V_T can have dependency on bias [21], this is not a strong one and has a negligible impact during the on-state conditions. There is still no conclusive study detailing this dependency nor models capable of describing it. The methodology is capable of considering this dependency by adding models in the Verilog-A model (as done to include the bias dependency of time constants).

The time constants used in Eq. (3), however, are a function of environmental variables such as the electrical field at the Si/SiO$_2$ interface as discussed for instance in [18]. To include these dependencies, during each step, prior to evaluate the next state of the trap the time constants are adjusted numerically, as presented in Section 2, based on the environmental parameters of each device and the conditions at which the trap was characterized. For a more precise consideration of these dependencies, one might also use the Eqs. (15) and (16) presented in [18]. A summary of this flow is presented in Fig. 1(a).

By performing an electrical simulation using the Verilog-A component, it is possible to simulate a given circuit with pre-defined traps considering the trap activity during the transient simulation. Aiming to improve the simulation process, a control script was written. Based on a configuration file that contains the information about the probability density functions of the trap related parameters and on the netlist of the studied circuit, this control script writes a new netlist changing the MOSFETs devices by the Verilog-A component and adding, to each instance of this component, its parameters (number of traps, time constants, and so on).

The control script starts by reading the configuration file and the netlist of the circuit of interest. For each Monte Carlo run, the control script defines the number of traps for each Verilog-A component in the circuit. For each MOSFET, the number of traps is randomly chosen according to a Poisson distribution as shown in [23]. The parameters of this distribution are defined in the configuration file and are adjusted based on the design parameters of each given component, such as its channel area [11]. During this stage the control script also writes the experimental characterization information related to the traps, which is also found in the configuration file, into every instance of the Verilog-A component.

Once the number of traps on each MOSFET is defined, the control script defines the impact of the trap on the threshold voltage (ΔV_{th}) and the time constants (τ_c and τ_e). Both parameters are random variables where the first is shown to be described by an exponential distribution with average η where η scales with the device properties as presented in [3]. For simplicity the time constants are described by uniform distributions in a logarithmic scale. In general, a more accurate bi-variate Gaussian distribution can be used [24]. Studies show that there is no correlation between the step-height and the time constants of each trap [3]. The definitions of these parameters for each trap are randomly chosen according to the statistical distribution of each random variable. The distributions and their properties are defined in the configuration file and are adjusted for each transistor based on its design dependent parameters, such as the channel area.

After all trap related information of each device in the design is defined, it is possible to run an electrical simulation which will consider the trap kinetics. Since all the equations were added to the transistor models and not to the simulation tool, any commercial tool that supports the Verilog-A standard is able to perform the simulation. Post simulation scripts aiming to analyze the results may be added after the electrical simulation to avoid losing information as other electrical simulations run in the same Monte Carlo loop.

The same trap kinetics mechanisms can be used to simulate BTI effects. Because BTI is an aging effect we are interested in evaluating its impact after a given time of operation, that may be in the range of years, and no longer in short time as we did for RTN. It is, however, impracticable to run transient electrical simulations in the range of years.

Aiming to allow users to simulate BTI effects, we implemented an analytical function capable of predicting the trap state after a certain period of time under a predefined stress condition. This way the user may describe the stress signal by its voltage, frequency and duty cycle, and define the duration of this stress condition. This function will, thus, evaluate the state of each trap for the stress condition defined and will feed the electrical simulator which will use these as its initial condition. The analytical solution is based on the trap kinetics equations presented in Section 2. A method of predicting the trap state after an arbitrary stress time under known conditions is presented in [25].

In contrast to the method that evaluates the trap activity on a transient Spice simulation, the analytical method presented in [25] is not capable to consider the impact that degraded devices have on the other devices surrounding it. A circuit with degraded devices produces slightly different waveforms which will be the stress signals for other circuits, for the case of a logic gate the rise and fall times will change, also changing how the next stage is stressed. A comparison between the two methods was performed, validating the methodology of [25] for long stress times where the BTI phenomena dominates, for short periods of time, where RTN dominates, the correlation between the impact of traps is more significant and thus the enhanced Spice simulation considering the trap kinetics should be used.

4. Case studies

Aiming to better illustrate the behavior of the simulation tool and its capabilities as to study circuits of interest for designers, some case studies were performed and are presented here. For
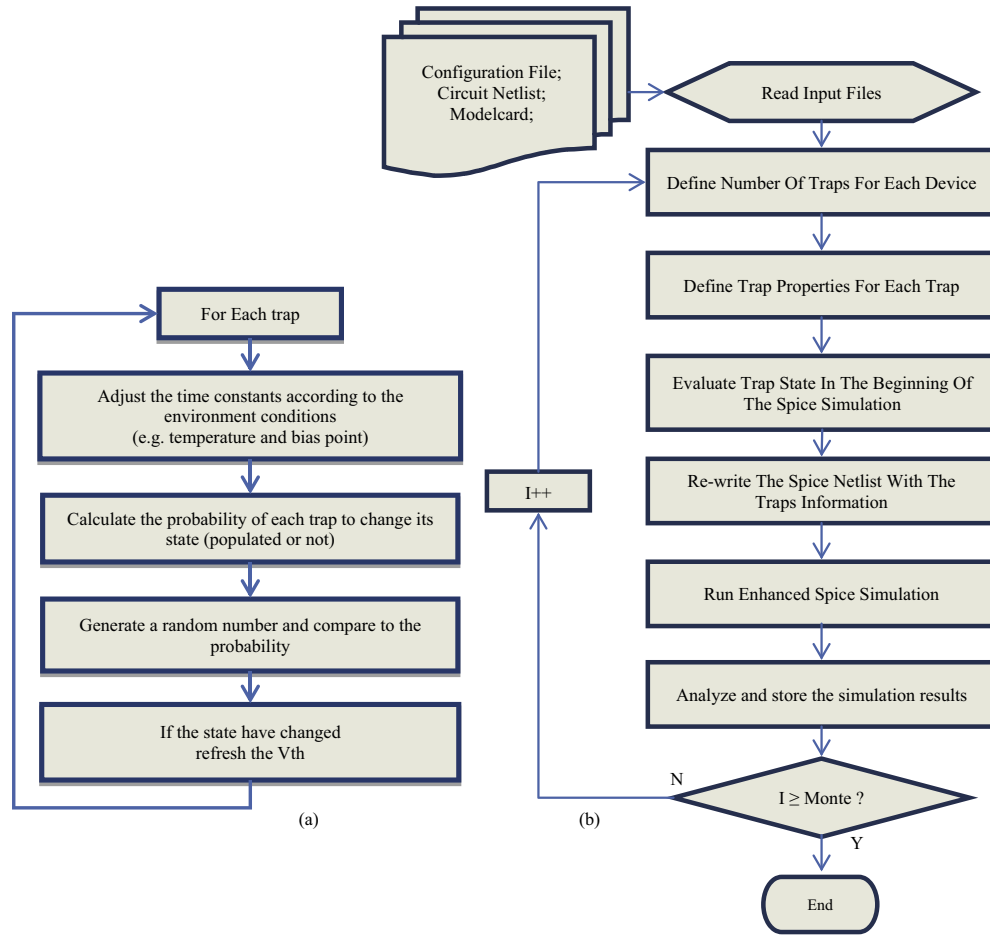
Fig. 1. (a) Trap kinetics on Verilog-A component. (b) High level simulation framework.

all case studies the test circuit was designed on a 45 nm CMOS technology. A PTM 45 nm modelcard for high-performance applications was used for the Spice simulation [26]. The trap properties used in the simulation are described in detail in [27]. Since trap related properties (as for instance number of traps on each device) are random variables, a statistical analysis method is mandatory.

In the first case study a transient simulation was run and the V_T of a PMOS transistor was measured right after the transistor started to be stressed. The result is plotted in Fig. 2. In this figure the trap activity and its impact on V_T are clearly seem. As each trap causes a particular impact on V_T it is possible to identify each trap and when it changed its state. The increase of V_T in time is caused by the BTI effect. In this figure it is possible to identify four traps responsible for causing the BTI effect. It is also possible to see one trap responsible for the RTN effect as it suffers both capture and emission events three times on this simulation.

For the second case study we performed a simulation on an inverter chain. The inverters used were sized with $w_p = 135$ nm
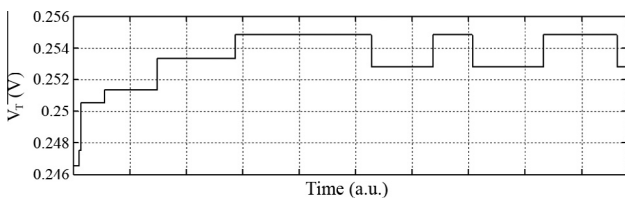
and $w_n = 90$ nm and $l = 50$ nm. A Monte Carlo simulation with 10,000 samples was then run and the delay of a given inverter in the center of the chain was analyzed. For this case study we considered not only the trap activity but also the time zero variability. The time zero variability in the transistors occurs due to effects such as Random Dopant Fluctuation (RDF) and Line Edge Roughness (LER) and, in this work, was modeled as a normal distribution of the threshold voltage with the standard deviation equal to 10% of the mean [28].

Fig. 3 shows the results obtained from these simulations. In (a) the delay of the inverter only considering the time zero variability is shown, while (b) shows the delay considering also the trap activity in the simulation. Comparing both figures we see not only the increase of the delay of the test inverters due to BTI but also that the right side tail obtained in the simulation considering the trap activity decreases much more smoothly. It is important to notice that the tail of the delay distribution is of high importance since it is in that region where circuits that fail to meet the constraints are located.

Ring oscillators are simple digital structures traditionally used as the base structure for voltage controlled oscillators and for test structures aiming at the extraction of basic parameters of the technology. Hence ring oscillators were chosen as the third case study. The inverters used in the ring oscillator simulated were sized with $w_p = 135$ nm and $w_n = 90$ nm and $l = 50$ nm.

The ring oscillator was submitted to a series of Monte Carlo analyses under different conditions. In each of these 1000 transient simulations were performed, using the enhanced electrical simulator presented in Section 3. On each simulation, the period of the

Fig. 2. Trap activity impact on the threshold voltage of a PMOS transistor in time.
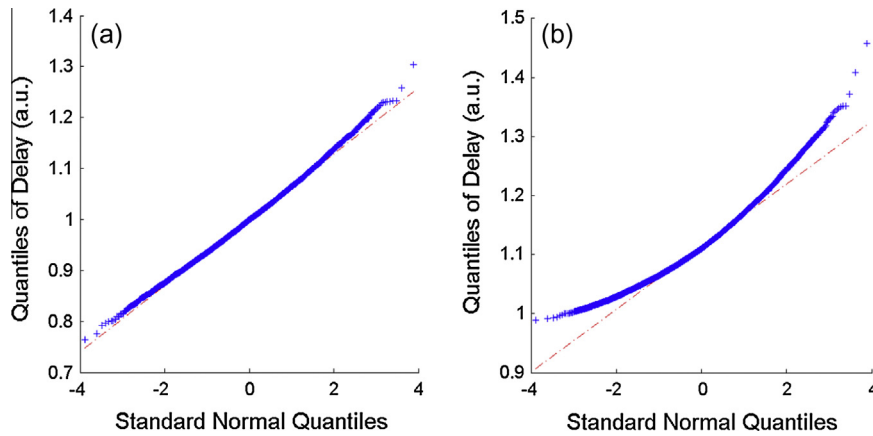
Fig. 3. (a) QQ-plot of the delay of an inverter considering the time zero variability and (b) considering also the trap activity after 1000 s of stress on nominal operating voltage (0.8 V) and duty factor of 0.5.

Table 1
Summary of the 7 stage RO analysis.

	Vdd	Time (s)	Avg. period (ns)	Avg. jitter (ps)
No time zero variability	0.8	0	0.37360	4.6665
	0.8	10^4	0.40492	5.6084
	0.83	10^4	0.37692	4.6822
Time zero variability	0.8	0	0.37608	5.0754
	0.8	10^4	0.40767	6.0284
	0.83	10^4	0.37797	4.8370

first 100 cycles was measured. The standard deviation of the period on each simulation was considered to be the signal cycle to cycle jitter, or just jitter.

First, we evaluated the impact RTN on the ring oscillator's jitter through a comparison between the initial impact of the RTN traps, and the impact of the RTN traps after 10^4 s of activity. These simulations were performed both with and without considering the time zero variability. It was then performed a new set of simulations increasing the operation voltage (Vdd) in order to adjust the oscillation period. All the simulations were performed under the conditions described above. The results are summarized at Table 1.

The results presented on Table 1 show that the jitter caused by the traps cannot be neglected with its average reaching a variation larger than 1.25% of the period of the signal. When including the long-term BTI effects caused by the traps in the simulation after 10^4 s of operation, we obtained an increase of 8.5% in the average period and of 18.8% in the average jitter over all the measured samples with time variability included.

The increase in the period is a natural cause of the increase of the V_T caused by the BTI effect. As the impact of each trap is also modeled as an increase on the V_T and, according to basic transistor models, it have a crescent impact on the drain current as it gets larger. The increase on the jitter is caused mainly by this increase of the impact of each trap in the transistor's drain current, which is occurs due to the increase on the V_T caused by the BTI. An increase of 0.3 V in the operation voltage was needed to compensate the impact of the BTI on the RO. The increase in the operation voltage also reduced the jitter as it also decreased the impact of each trap in the transistor's drain current.

Fig. 4(a) shows the cumulative distribution function (CDF) of oscillation period, measured in the simulation of 1000 successive cycles of a 3-stage ring oscillator with the same size as the test circuit. This simulation was performed considering that the transistors were already stressed by 10^{-4} s in the ring oscillator with a duty factor of 0.5. In this figure it is clearly seen that a few traps dominate the behavior, with clear discrete steps in the CDF. This happens because the cause of the jitter in this simulation is the trap activity which varies between discrete levels characterizing the RTN effect. For larger ring oscillators, i.e. ring oscillators formed by larger transistors or with a higher number of stages, this step like distribution is not as clearly noticed due to the increase of the number of traps affecting the signal period as the decrease of the impact of each trap. This case is shown in Fig. 4(b) where the studied circuit was a 7-stage ring oscillator.

A case study consisting of a simulation of the V_{min} a SRAM cell during the stand by condition under the effect of trap activity was performed. Both the PMOS and NMOS core transistors were sized with $(W/L) = (65 \text{ nm}/45 \text{ nm})$ and the NMOS pass transistor
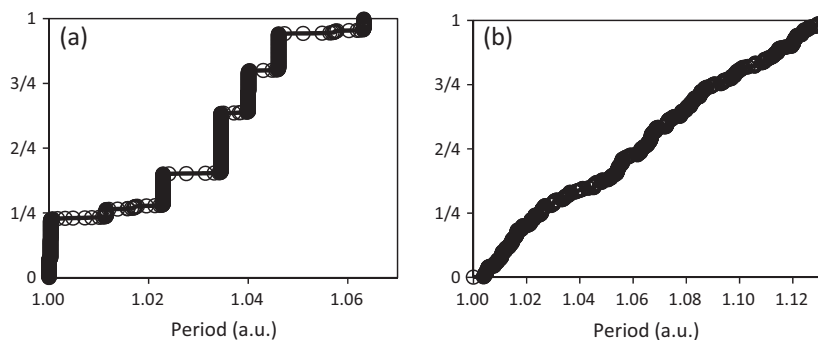
Fig. 4. Cumulative density function of 1000 periods of a (a) 3-stage ring oscillator and (b) of a 7-stage ring oscillator under the effect of trap activity.
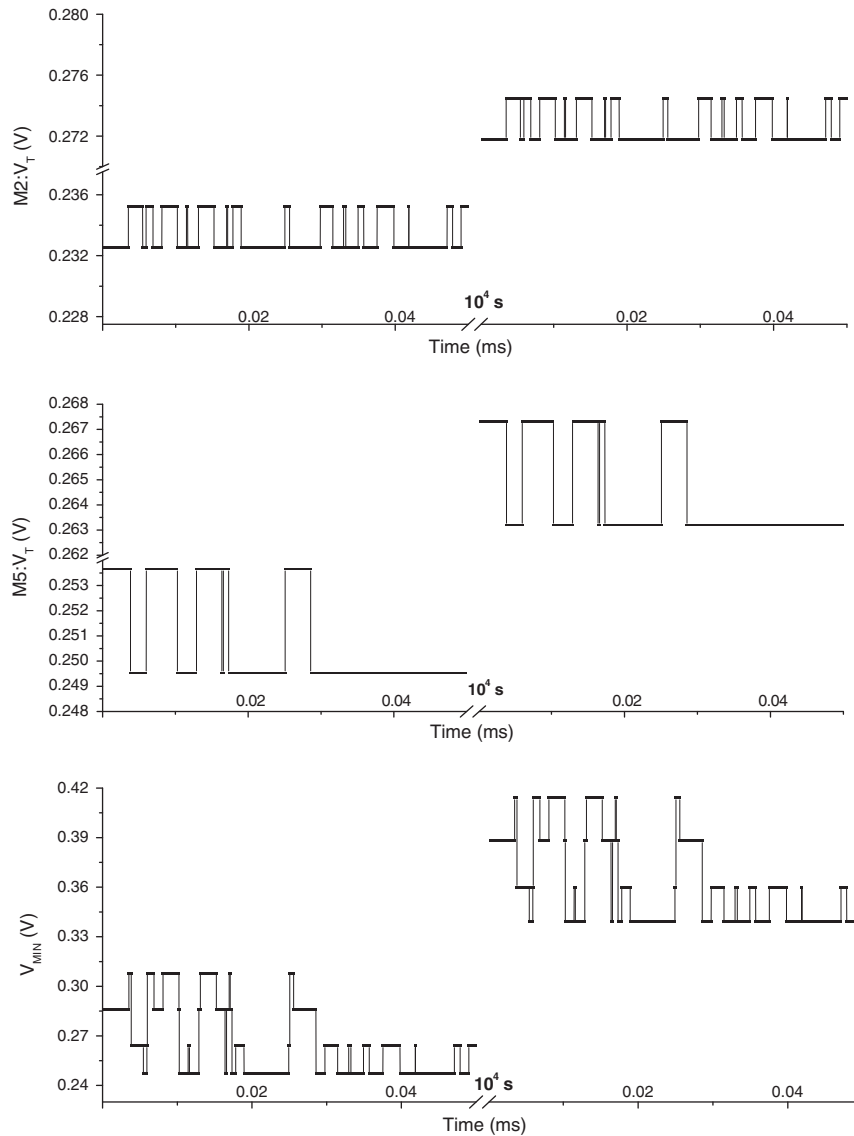
Fig. 5. Threshold voltage as a function of time for the transistors M2 and M5 of the 6T-SRAM case study cell and how these impact SRAM V_{min}. The right hand side depicts the values after an elapsed time of 10^4 s (indicated by the break of 10^4 s shown in the time axis). During this time the cell suffered BTI, as seen in the threshold voltages and SRAM V_{min}.

were sized with $(W/L) = (90 \text{ nm}/45 \text{ nm})$. The V_{min} was considered the minimum supply voltage at which the design has a positive Read Noise Margin.

Fig. 5 shows the V_{min} of a SRAM cell in a transient simulation. The transient simulation was run for two different BTI stress times. The first simulation is for a BTI stress of 100 μs, and the second simulation corresponds to a stress time of 10 ks. Due to the small number of traps in the devices and the constant bias, RTN trap activity was detected only on a PMOS core transistor (M2) and on a NMOS core transistor (M5) during the transient simulation, each of these transistors showing a single RTN trap. From the BTI stress time of 100 μs to 10 ks, the duty cycle on the memory was 0.5, leading to a V_T shift due to BTI in transistor M2 of 25.7 mV and of 9.96 mV in M5. The duty cycle of 0.5 was chosen to avoid degrading some transistors of the cell much more than others which would generate an unbalance leading to a much larger V_{min}.

To allow easy comparison between the BTI stress conditions, the same seed was chosen for the random number generator in the RTN trap simulation for both cases. In other words, RTN activity is the same in both simulations.

Comparing the V_{min} of the SRAM cell with the trap activity seen in the transistor's V_T, we can see that the trap activity translates its impact to the V_{min} parameter. Experimental data showing the impact of RTN on SRAM reliability is shown in [29,33–35]. This effect is very relevant for the test of SRAM cells as it shows that a cell tested working for a given V_{min} condition might not be reliably working for the same condition after just a few instants later due to the trap activity. It is possible to see that both BTI and RTN traps have an important impact on the cell's V_{min}.

Regarding the computational efficiency of the simulation tool, it presented an overhead of around 30% on the simulation time on the case study when compared to the same simulations without considering the trap kinetics, presenting itself as a highly efficient simulation tool. Case studies using a previous version of the tool, capable to simulate solely BTI, are presented in [30–32].

Monte Carlo is a simple and widely employed technique to simulate the impact of charge trapping and de-trapping at the circuit level. However, it can become prohibitive if the simulation of large sample sizes is demanded, as for instance to investigate the far tails of a distribution. In these situations, the use of analytical models

and efficient alternatives to Monte Carlo, as for instance the Response Surface Methodology [36], is demanded. The authors are working on applying these techniques to the simulation of BTI and RTN.

5. Conclusions

A circuit simulation method capable of considering the trap activity during transient electrical simulations was presented. Because it is directly obtained from detailed defect studies and adjusted with experimental data, this approach leads to an accurate tracking of the trap states during the simulation. This allows the analysis of the impact of trap activity in arbitrary circuits. Because the trap kinetics are included in the transistor model, it is possible to use this method with any electrical simulation tool and it also allows the user to extend this methodology to include other time dependent effects. A case study on a ring oscillator demonstrates the impact of the traps on both jitter and BTI, and a case study on a SRAM cell shows how critical the trap activity can be on the reliability of SRAM cells as it affects the V_{min} of the cell. The overhead in the running time of this simulation method presented is slightly larger than a traditional electrical simulation. Overall, this simulation methodology proves to be an efficient tool for analyzing both RTN and BTI.

References

[1] Toledano-Luque M, Kaczer B, Simoen E, Degraeve R, Franco J, Roussel PJ, et al. Correlation of single trapping and detrapping effects in drain and gate currents of nanoscaled nFETs and pFETs. In: 2012 IEEE international reliability physics symposium (IRPS), 15–19 April 2012. p. XT.5.1–XT.5.6.

[2] Grasser T, Kaczer B, Goes W, Reisinger H, Aichinger T, Hehenberger P, et al. The paradigm shift in understanding the bias temperature instability: from reaction–diffusion to switching oxide traps. IEEE Trans Electron Dev 2011;58(11):3652–66.

[3] Kaczer B, Grasser T, Roussel PJ, Franco J, Degraeve R, Ragnarsson L, et al. Origin of NBTI variability in deeply scaled pFETs. In: 2010 IEEE international reliability physics symposium (IRPS), 2–6 May 2010. p. 26–32.

[4] Ashraf N, Vasileska D, Wirth G, Srinivasan P. Accurate model for the threshold voltage fluctuation estimation in 45-nm channel length MOSFET devices in the presence of random traps and random dopants. IEEE Electron Dev Lett 2011;32(8):1044–6.

[5] Leyris C, Pilorget S, Marin M, Minondo M, Jaouen H, Random telegraph signal noise SPICE modeling for circuit simulators. In: Solid state device research conference, 2007. ESSDERC 2007. 37th European, No., 11–13 September 2007. p. 187–190.

[6] Ye Y, Wang CC, Cao Y. Simulation of random telegraph noise with 2-stage equivalent circuit. In: Proceedings of the IEEE/ACM international conference on computer aided design 2010.

[7] Vaidyanathan B, Oates AS. Technology scaling effect on the relative impact of NBTI and process variation on the reliability of digital circuits. IEEE Trans Dev Mater Reliab 2012;12(2):428–36.

[8] Van Der Wel AP. Modeling random telegraph noise under switched bias conditions using cyclostationary RTS noise. IEEE Trans Electron Dev May 2003.

[9] Kolhatkar JS. Steady-state and cyclo-stationary RTS noise in MOSFETS. PhD thesis. The Netherlands: The University of Twente; 2005. <http://doc.utwente.nl/48261/1/thesis-Kolhatkar.pdf>.

[10] Wirth G, da Silva R, Srinivasan P, Krick J, Brederlow R, Statistical model for MOSFET low-frequency noise under cyclo-stationary conditions. In: 2009 IEEE international electron devices meeting (IEDM), 7–9 Dec. 2009. p. 1–4.

[11] Wirth G, Vasileska D, Ashraf N, Brusamarello L, Della Giustina R, Srinivasan P. Compact modeling and simulation of random Telegraph noise under non-stationary conditions in the presence of random dopants. Microelectron Reliab 2012;52:2955–61.

[12] Reisinger H, Grasser T, Ermisch K, Nielen H, Gustin W, Schlunder C. Understanding and modeling AC BTI. In: 2011 IEEE international reliability physics symposium (IRPS), 10–14 April 2011. p. 6A.1.1–6A.1.8.

[13] Tong Boon Tang, Murray AF, Roy S, Methodology of statistical RTS noise analysis with charge-carrier trapping models in circuits and systems I: regular papers. IEEE Trans 2010;57(5):1062–70.

[14] Aadithya KV, Demir A, Venugopalan S, Roychowdhury J. Accurate prediction of random telegraph noise effects in SRAMs and DRAMs. IEEE Trans Comput-Aided Des Integr Circ Syst 2013;32(1):73–86.

[15] Grasser T. Stochastic charge trapping in oxides: from random telegraph noise to bias temperature instabilities. Microelectron Reliab 2012;52(1):39–70. ISSN 0026-2714, doi:10.1016/j.microrel.2011.09.002.

[16] Wirth GI, da Silva R, Kaczer B. Statistical model for MOSFET bias temperature instability component due to charge trapping. IEEE Trans Electron Dev 2011;58(8):2743–51.

[17] Machlup S. Noise in semiconductors: spectrum of a two-parameter random signal. J Appl Phys 1954;25(3):341–3.

[18] Grasser T, Reisinger H, Wagner P, Schanovsky F, Goes W, Kaczer B. The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability. In: 2010 IEEE international reliability physics symposium (IRPS), 2–6 May 2010. p. 16–25.

[19] BSIM 4.6.4 MOSFET model users' manual. Berkeley: EECS Department, University of California; 2009.

[20] Chalkiadaki M-A, Valla C, Poullet F, Bucher M. Why- and how- to integrate Verilog-A compact models in SPICE simulators. Int J Circ Theory Appl 2012. http://dx.doi.org/10.1002/cta.183.

[21] Franco J, Kaczer B, Toledano-Luque M, Bukhori MF, Roussel PJ, Grasser T, et al. Impact of individual charged gate-oxide defects on the entire ID–VG characteristic of nanoscaled FETs. IEEE Electron Dev Lett 2012;33(6). p. 779, 781.

[22] Gerrer L, Ding J, Amoroso SM, Adamu-Lema F, Hussin R, Reid D, et al. Modelling RTN and BTI in nanoscale MOSFETs from device to circuit: a review. Microelectron Reliab 2014;54(4):682–97.

[23] Keyes RW. The effect of randomness in the distribution of impurity atoms on FET thresholds. Appl Phys 1975;8(3):251–9.

[24] Bina M, Rupp K, Tyaginov S, Triebl O, Grasser T, Modeling of hot carrier degradation using a spherical harmonics expansion of the bipolar Boltzmann transport equation. In: 2012 IEEE international electron devices meeting (IEDM), 10–13 December 2012. p. 30.5.1, 30.5.4.

[25] Toledano-Luque M, Kaczer B, Roussel PJ, Grasser T, Wirth GI, Franco J, et al. Response of a single trap to AC negative bias temperature stress. In: 2011 IEEE international reliability physics symposium (IRPS), 10–14 April 2011. p. 4A.2.1–4A.2.8.

[26] Zhao W, Cao Y. New generation of predictive technology model for sub-45nm early design exploration. IEEE Trans Electron Dev 2006;53(11):2816–23.

[27] Toledano-Luque M, Kaczer B, Simoen E, Roussel PhJ, Veloso A, Grasser T, et al. Temperature and voltage dependences of the capture and emission times of individual traps in high-k dielectrics. Microelectron Eng 2011;88(7):1243–1246. ISSN 0167–9317, http://dx.doi.org/10.1016/j.mee.2011.03.097.

[28] Cathignol A, Cheng B, Chanemougame D, Brown AR, Rochereau K, Ghibaudo G, et al. Quantitative evaluation of statistical variability sources in a 45-nm technological node LP N-MOSFET. IEEE Electron Dev Lett 2008;29(6):609–11.

[29] Agostinelli M, Hicks J, Xu J, Woolery B, Mistry K, Zhang K, et al. Erratic fluctuations of sram cache vmin at the 90 nm process technology node. In: IEEE international electron devices meeting, 2005. IEDM technical digest. 5–5 December 2005. p. 655, 658.

[30] Kaczer B, Mahato S, de Almeida Camargo VV, Toledano-Luque M, Roussel PJ, Grasser T, et al. Atomistic approach to variability of bias-temperature instability in circuit simulations. In: Reliability physics symposium (IRPS), 2011 IEEE international, No., 10–14 April 2011. p. XT.3.1–XT.3.5.

[31] Rodopoulos D, Mahato SB, de Almeida Camargo VV, Kaczer B, Catthoor F, Cosemans S, et al. Time and workload dependent device variability in circuit simulations. In: 2011 IEEE international conference on IC design & technology (ICICDT), 2–4 May 2011. p. 1–4.

[32] Camargo VVA, Kaczer B, Wirth G, Grasser T, Groeseneken G. Use of SSTA tools for evaluating BTI impact on combinational circuits. In: IEEE transactions on very large scale integration (VLSI) systems, vol. 22, No. 2, February 2014. p. 280, 285.

[33] Takeuchi K, Nagumo T, Takeda K, Asayama S, Yokogawa S, Imai K, et al. Direct observation of RTN-induced SRAM failure by accelerated testing and its application to product reliability assessment. In: 2010 symposium on VLSI technology (VLSIT), 15–17 June 2010. p. 189, 190.

[34] Takeuchi K, Nagumo T, Hase T. Comprehensive SRAM design methodology for RTN reliability. In: 2011 symposium on VLSI technology (VLSIT), 14–16 June 2011. p. 130, 131.

[35] Yamaoka M, Miki H, Bansal A, Wu S, Frank DJ, Leobandung E, et al. Evaluation methodology for random telegraph noise effects in SRAM arrays. In: 2011 IEEE international electron devices meeting (IEDM), 5–7 December 2011. p. 32.2.1, 32.2.4.

[36] Brusamarello Lucas, Wirth Gilson I, Roussel Philippe, Miranda Miguel. Fast and accurate statistical characterization of standard cell libraries. Microelectron Reliab 2011;51(12):2341–50.