

Modeling of Hot-Carrier Degradation in nLDMOS Devices: Different Approaches to the Solution of the Boltzmann Transport Equation

Prateek Sharma, Stanislav Tyaginov, Yannick Wimmer, Florian Rudolf, Karl Rupp, Markus Bina, Hubert Enichlmair, Jong-Mun Park, *Member, IEEE*, Rainer Minixhofer, *Senior Member, IEEE*, Hajdin Ceric, and Tibor Grasser, *Senior Member, IEEE*

Abstract—We propose two different approaches to describe carrier transport in n-laterally diffused MOS (nLDMOS) transistor and use the calculated carrier energy distribution as an input for our physical hot-carrier degradation (HCD) model. The first version relies on the solution of the Boltzmann transport equation using the spherical harmonics expansion method, while the second uses the simpler drift-diffusion (DD) scheme. We compare these two versions of our model and show that both approaches can capture HCD. We, therefore, conclude that in the case of nLDMOS devices, the DD-based variant of the model provides good accuracy and at the same time is computationally less expensive. This makes the DD-based version attractive for predictive HCD simulations of LDMOS transistors.

Index Terms—Drift-diffusion (DD) scheme, hot-carrier degradation (HCD), n-laterally diffused MOS (nLDMOS), spherical harmonics expansion (SHE).

I. INTRODUCTION

LATERALLY diffused MOS (LDMOS) transistors are attractive for mixed-signal integrated circuits and high-voltage automotive applications [1]. One of the main concerns limiting the lifetime of LDMOS devices is hot-carrier degradation (HCD) [1]–[4]. Although the first observation of this detrimental phenomenon dates back to over four decades ago, the full physical mechanisms are complicated and not yet completely clear, making the predictive modeling

of HCD difficult. As a result, quite often, simplified empirical/phenomenological approaches are used [5], [6]. The most successful among them are based on the so-called energy-driven paradigm proposed in [7]–[10]. These approaches introduce three main modes of HCD: 1) governed by the single-carrier mechanism of Si-H bond dissociation; 2) driven by the multiple-carrier bond-breakage process; and 3) dominated by electron–electron scattering. Thereby, the computationally demanding simulations of the carrier energy distribution functions (DFs) are avoided and the rates of the aforementioned processes are described by empirical formulas that are related to the macroscopic transistor characteristics [10]. Note that these models are derived and calibrated using accelerated stress conditions. Therefore, it is possible that at real operating conditions, the physical picture behind HCD is different, making the models based on empirical expressions not predictive.

A remedy can be a physical HCD model that covers the whole hierarchy of the aspects related to HCD, namely, 1) a thorough carrier transport treatment that provides the information on the carrier energy distribution function needed to 2) model the microscopic mechanism of trap generation and the corresponding rates, and to 3) simulate the characteristics of the degraded devices [11], [12]. The most computationally expensive among these subtasks is the carrier transport treatment, which requires a solution of the Boltzmann transport equation (BTE). This is computationally challenging and becomes even more challenging for LDMOS transistors. First, this is related to the typical dimensions of LDMOS devices, as compared with nanoscale CMOS transistors, and thus to a mesh that contains a large number of cells, i.e., $\sim 10\,000$ [13]. Second, these transistors have a sophisticated architecture, including the bird's beak and the nonplanar interface (Fig. 1), and also high doping gradients in different regions. Furthermore, as we have shown recently [13], both single- and multiple-carrier mechanisms of bond dissociation provide substantial contributions to HCD. More importantly, contrary to the common perception, the multiple-carrier bond-breakage process appears to give a significant contribution also in nMOSFETs with gate lengths as long as $2\ \mu\text{m}$ when stressed at high voltages [14]–[16].

In this context, simplified approaches to the solution of the BTE, such as the drift-diffusion (DD) and energy

Manuscript received December 28, 2014; revised March 6, 2015; accepted April 4, 2015. Date of publication April 29, 2015; date of current version May 18, 2015. This work was supported in part by the European Community within the Seventh Framework Programme through the Mordred Project under Grant 261868 and ATHENIS 3-D Project under Grant 619246 and in part by the Austrian Science Fund under Grant P23598 and Grant P26382. The review of this paper was arranged by Editor E. Rosenbaum.

P. Sharma, Y. Wimmer, and H. Ceric are with the Christian Doppler Laboratory, Institute for Microelectronics, Technische Universität Wien, Wien 1040, Austria (e-mail: sharma@iue.tuwien.ac.at; wimmer@iue.tuwien.ac.at; ceric@iue.tuwien.ac.at).

S. Tyaginov is with the Institute for Microelectronics, Technische Universität Wien, Wien 1040, Austria, and also with the Ioffe Physical-Technical Institute, Russian Academy of Sciences, St. Petersburg 194021, Russia (e-mail: tyaginov@iue.tuwien.ac.at).

F. Rudolf, K. Rupp, M. Bina, and T. Grasser are with the Institute for Microelectronics, Technische Universität Wien, Wien 1040, Austria (e-mail: rudolf@iue.tuwien.ac.at; rupp@iue.tuwien.ac.at; bina@iue.tuwien.ac.at; grasser@iue.tuwien.ac.at).

H. Enichlmair, J.-M. Park, and R. Minixhofer are with ams AG, Unterpremstätten 8141, Austria (e-mail: hubert.enichlmair@ams.com; jongmun.park@ams.com; rainer.minixhofer@ams.com).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TED.2015.2421282

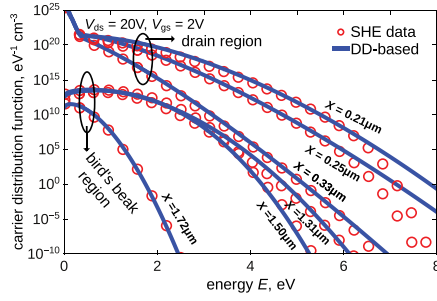


Fig. 3. Electron DFs obtained with ViennaSHE and with the DD-based model for $V_{ds} = 20$ V, $V_{gs} = 2$ V, calculated for different positions near the drain and close to the bird's beak region.

B. Carrier Transport

As mentioned previously, the key ingredient in our HCD model is the carrier energy DF. A solution of the BTE can be obtained either stochastically using the Monte Carlo method [36], [37] or deterministically using the spherical harmonics expansion (SHE) approach [38]. Although the first method was extensively used in the first versions of our HCD model [14], [15], [39], the Monte Carlo approach is not well suited for HCD modeling in LDMOS devices due its enormous computational demands related to resolving the high-energy tails. Thus, our model is implemented in our deterministic BTE solver ViennaSHE [11], [12], [30]. An alternative way, as mentioned before, is to use simplified approaches to the BTE solution such as the DD scheme. In this case, the carrier DF computed with ViennaSHE can be used as a benchmark for the DD-based approach.

1) *BTE Solution*: ViennaSHE is a deterministic BTE solver that considers energy exchange mechanisms, such as the electric field, impact ionization, electron-electron and electron-phonon scattering, scattering at ionized impurities, and full-band effects [38], [40], [41]. A cell-centered discretization scheme used in ViennaSHE simplifies the treatment of material interfaces and can be used on arbitrary grids, not requiring a Delaunay property [42]. As a result, ViennaSHE provides smooth DF curves spreading over many orders of magnitude and over several electronvolts. Fig. 3 shows two families of electron DFs obtained for $V_{gs} = 2$ V and $V_{ds} = 20$ V and for different positions in the device, i.e., one family corresponds to the bird's beak region, while the second one summarizes DFs evaluated for the drain section. One can see that the carrier DFs are severely nonequilibrium. While at the drain, DFs have a cold Maxwellian tail at low energies, the DFs calculated for the bird's beak do not have this rudiment and have a totally different shape. In all cases, the DFs have long high-energy tails.

2) *Drift-Diffusion Scheme*: The electron DFs developed by the Reggiani group are given by [23]

$$f(\varepsilon) = A \exp \left[-\alpha \left(\frac{\varepsilon(1 + \delta\varepsilon)}{k_B T_n (1 + \beta\varepsilon)} \right) \right] \quad (1)$$

where ε is the carrier energy, T_n is the carrier temperature, k_B is the Boltzmann constant, while the parameters A and α are determined using the information on the carrier

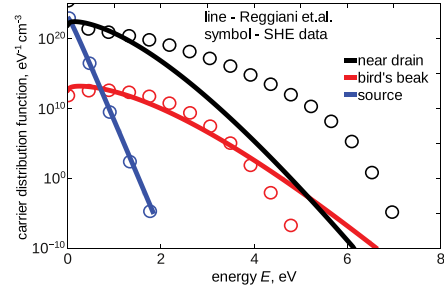


Fig. 4. Comparison of DFs obtained with the Reggiani DD-based model with those simulated using ViennaSHE for stress voltages: $V_{ds} = 20$ V, $V_{gs} = 2$ V, calculated for different positions near the drain, bird's beak, and source region.

concentration n and the carrier temperature T_n [23]. Although the Reggiani model can describe the degradation of the LDMOS device characteristics with good accuracy, the expression (1) appears to be less accurate in the vicinity of the drain region. From Fig. 4, one can see that the high-energy tails of the DFs are underpopulated if this model is used. This leads to a weaker curvature in the $\Delta I_{d,sat}(t)$ and $\Delta I_{d,lin}(t)$ curves.

In order to avoid this inaccuracy, we will use our previously suggested approach [43] to describe the DF. This approach considers the contribution of both hot and equilibrium carriers with the corresponding DF defined as

$$f(\varepsilon) = A \exp \left[-\left(\frac{\varepsilon}{\varepsilon_{ref}} \right)^b \right] + C \exp \left[-\frac{\varepsilon}{k_B T_n} \right]. \quad (2)$$

Here, the first term represents the DFs in the channel section where the carriers are hot, in the bird's beak region as well as the high energetic carriers in the drain region. The pool of cold carriers in the drain/source region is correctly modeled by an additional cold Maxwellian term. The carrier temperature is obtained from postprocessing of the DD simulation results. We extract the electron concentration as a function of the lateral coordinate $n(x)$, the electric field profile $F(x)$, and the carrier mobility $\mu(x)$ from the DD simulations in MINIMOS-NT. These quantities are then used to evaluate the carrier temperature $T_n(x)$ according to

$$T_n = T_L + \frac{2}{3} \frac{q}{k_B} \tau \mu F^2 \quad (3)$$

where T_L is the lattice temperature, q is the modulus of the electron charge, and τ is the energy relaxation time with typical values of $\tau_n = 0.35$ ps for electrons and $\tau_p = 0.4$ ps for holes [17]. The parameters of the DF are then determined using the carrier concentration and the carrier temperature, as well as the DF normalization

$$\int_0^\infty f(\varepsilon) g(\varepsilon) d\varepsilon = n \quad (4)$$

$$\int_0^\infty \varepsilon f(\varepsilon) g(\varepsilon) d\varepsilon = \frac{3}{2} n k_B T_n \quad (5)$$

$$\int_0^\infty f(\varepsilon) d\varepsilon = 1. \quad (6)$$

For the density of states $g(\varepsilon)$, we use the expression proposed in [44]

$$g(\varepsilon) = g_0 \sqrt{\varepsilon} (1 + \eta \varepsilon) \quad (7)$$

which very accurately reproduces the conventional nonparabolic Kane relation but can be integrated analytically [44]. Then, the DFs for different energies are calculated from (2) using the parameters A , C , and ε_{ref} obtained from the above set of (2) and (4)–(6), while the parameter b is assigned a constant value of 1 near the drain and source regions and 2 otherwise. It is worth mentioning that ViennaMesh proves to be beneficial also for the DD simulations in MINIMOS-NT as even the DD approach can be computationally challenging in such devices.

C. Interface State Generation Kinetics

The carrier DFs are used to compute the carrier acceleration integral (AI), which determines the rates of both single- and multiple-carrier processes [11], [12], [30]

$$I_{\text{SC/MC}}^{e/h} = \int_0^\infty f(\varepsilon) g(\varepsilon) v(\varepsilon) \sigma_0 (\varepsilon - \varepsilon_{\text{th}})^p d\varepsilon \quad (8)$$

where $f(\varepsilon)$ is the DF, $g(\varepsilon)$ is the density-of-states, $v(\varepsilon)$ is the carrier group velocity, and $\sigma_0 (\varepsilon - \varepsilon_{\text{th}})^p$ is the reaction cross section. In the case of the single-carrier bond-breakage process the reaction cross section is Keldysh-like [14], [39], with the threshold energy equal to the bond-breakage activation energy. For the multiple-carrier process, the bond is modeled as a truncated harmonic oscillator [27], [29], and the threshold energy corresponds to the distance between the bond vibrational states. An efficient way of bond dissociation is obtained when the bond is first preheated by a series of colder carriers and then dissociated by a solitary hot electron [11], [12], [30]. Thereby, we consider all superpositions of single- and multiple-carrier mechanisms [12], [25]–[28], [30].

The rates of the bond excitation/deexcitation processes triggered by the multiple-carrier mechanism are

$$P_u = I_{\text{MC}} + \omega_e \exp[-\hbar\omega/k_B T_L] \quad (9)$$

$$P_d = I_{\text{MC}} + \omega_e. \quad (10)$$

As for the cumulative passivation/depassivation rates, they are expressed as [11], [12], [30]

$$R_{a,i} = \omega_{\text{th}} \exp[-(E_a - E_i)/k_B T_L] + I_{\text{SC},i} \quad (11)$$

$$\mathfrak{R}_a = \frac{1}{k} \sum_i R_{a,i} \left(\frac{P_u}{P_d} \right)^i \quad (12)$$

$$\mathfrak{R}_p = v_p \exp(-E_p/k_B T_L) \quad (13)$$

with the first term in (11) corresponding to thermal activation of the H atom, while the second one incorporates the effect of hot carriers. Note that each bond level, i , can contribute to the bond-breakage process (11).

Another important factor that affects the bond-breakage kinetics is the activation energy dispersion due to the disorder at the Si/SiO₂ interface. We, furthermore, assume that the bond interacts with the electric field across the oxide which leads to a reduction of the binding energy [11], [12], [30].

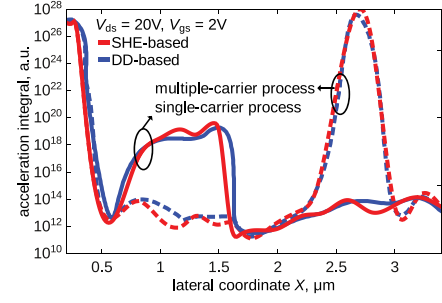


Fig. 5. AI calculated using the DFs obtained with the DD-based model and ViennaSHE for $V_{\text{ds}} = 20$ V, $V_{\text{gs}} = 2$ V for the single- and multiple-carrier processes.

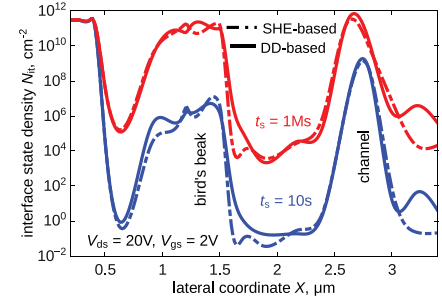


Fig. 6. Interface state density profiles evaluated with the DD- and SHE-based models for stress voltages $V_{\text{ds}} = 20$ V, $V_{\text{gs}} = 2$ V applied for 10 s and 1 Ms.

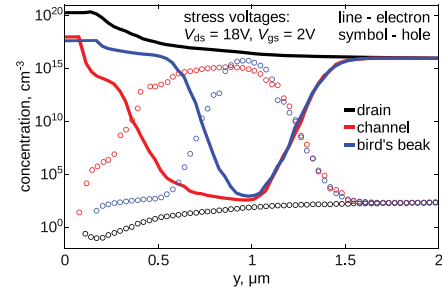


Fig. 7. Electron and hole concentrations as a function of the coordinate y perpendicular to the Si/SiO₂ interface evaluated near the drain region, the bird's beak, and in the channel.

D. Modeling of the Degraded Device

The solution of the kinetic equations set which describes the Si-H bond passivation/depassivation processes leads to the following expression for the interface state density (N_{it}):

$$N_{\text{it}} = \frac{1}{2\tau \mathfrak{R}_p} \frac{1 - f(t)}{1 + f(t)} - \frac{\mathfrak{R}_a}{2\mathfrak{R}_p} \quad (14)$$

$$f(t) = \frac{1 - \tau \mathfrak{R}_a}{1 + \tau \mathfrak{R}_a} \exp(-t/\tau)$$

$$\frac{1}{\tau} = 2\sqrt{\mathfrak{R}_a^2/4 + N_0 \mathfrak{R}_a \mathfrak{R}_p}$$

where N_0 is the density of pristine Si-H bonds present in the fresh device. $N_{\text{it}}(x, t)$ profiles evaluated using (14) are then used as input for the device simulator to model the characteristics of the device for each stress time step. The effect of charged interface traps is twofold: 1) they perturb

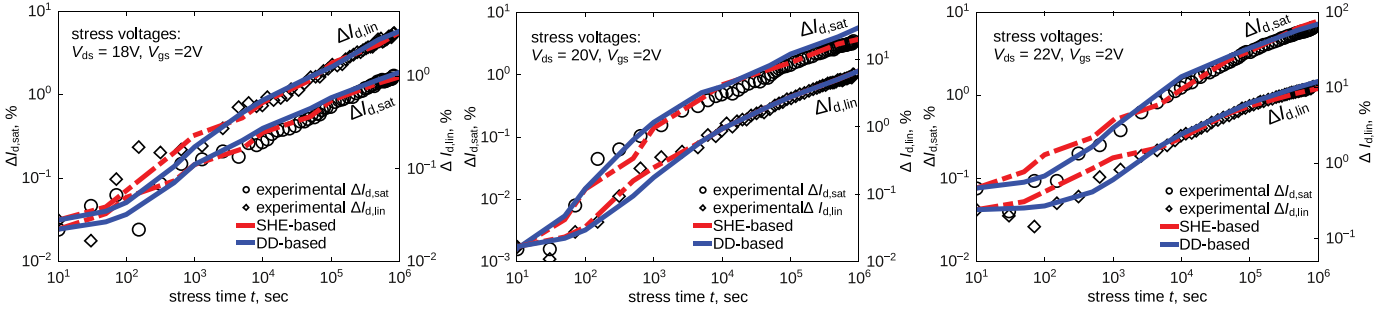


Fig. 8. Experimental change in the saturation and linear drain currents plotted versus simulation obtained with the SHE- and DD-based models for a fixed gate voltage $V_{gs} = 2$ V and three different drain voltages $V_{ds} = 18, 20$, and 22 V.

the local band-bending of the device and 2) they degrade the carrier mobility due to scattering of the charge carriers. The former effect is considered while solving the coupled Poisson's equation and BTE, while for the latter one we use the empirical mobility degradation expression [45], [46]

$$\mu_{\text{degr}} = \frac{\mu_0}{1 + \alpha N_{\text{it}} \exp(-r/r_{\text{ref}})} \quad (15)$$

where μ_0 is the mobility in the virgin device, r is the shortest distance from this local point to the interface, $r_{\text{ref}} = 1$ nm defines the maximum range within which a carrier is still influenced by the field of the trapped charge, while the parameter $\alpha = 10^{-13}$ cm² determines the magnitude of the effect.

IV. RESULTS AND DISCUSSION

The DD-based scheme is able to represent the carrier DFs for the source and channel regions. Note that in these device sections the DFs are not severely perturbed from equilibrium. As already shown in Fig. 3, the agreement between the nonequilibrium DFs is also good, especially near the bird's beak of the nLDMOS transistor. As for the drain device area, a small discrepancy is visible at high energies. At these high energies, however, the DF has dropped by >20 orders of magnitude and this discrepancy does not transform into a significant error of the model. To prove this, we also plot the AI calculated by (8) for both the single- and multiple-carrier processes. Fig. 5 shows that the AIs computed with the SHE- and DD-based approaches are quite similar, and thus the discrepancy in the DFs at high energies visible for the case of the drain region is insignificant. Fig. 5 also demonstrates that the multiple-carrier process plays an important role in large devices such as an nLDMOS transistor and should be considered in the model.

The $N_{\text{it}}(x)$ profiles simulated using SHE- and DD-based approaches for the entire lateral coordinate range and for 10 s and 1 Ms are presented in Fig. 6. It can be seen from Figs. 3 and 5 that the carriers near the drain are rather hot and both the single- and multiple-carrier processes are saturated, thus leading to the N_{it} peak at the drain region. Another peak is pronounced in the vicinity of the bird's beak, which is due to the single-carrier process as the rate of the multiple-carrier process (Fig. 5) is negligible in this region. The third N_{it}

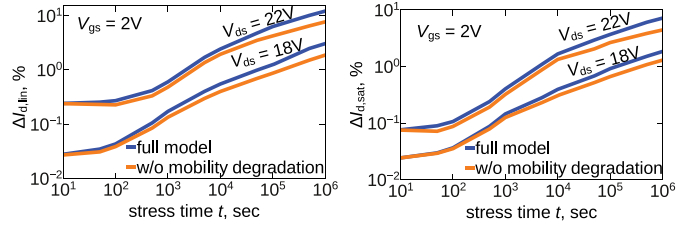


Fig. 9. Relative change in the linear and saturation drain currents simulated with the DD-based version of the model. One can see that if the mobility degradation is not considered, the changes of the linear and saturation drain currents can be severely underestimated. For instance, at stress time of 1 Ms the errors in $\Delta I_{d,\text{lin}}$ and $\Delta I_{d,\text{sat}}$ are 27% and 33%, respectively.

maximum located in the channel at $x \sim 2.8$ μm stems from the common action of the multiple-carrier process of the bond dissociation and the interaction of the dipole moment of the bond with the electric field [13].

The role of this N_{it} peak in the channel is worth discussing. In the previous version of our HCD model [5], [15], the hole contribution to the bond-breakage process was suggested to be the primary cause. This is because the corresponding interface traps are shifted toward the channel center as compared with those states, which are generated near the drain end of the gate by the channel electrons, and as a result, the relative effect of holes is stronger. The hole related damage was also discussed to be important by other groups in the context of HCD in nLDMOS devices [47], [48]. In our nLDMOS transistor, however, the holes have a very low concentration near the Si/SiO₂ interface with values not exceeding 10^5 cm⁻³, i.e., ~ 15 orders of magnitude lower than the electron density (Fig. 7). As a result, while modeling the trap generation kinetics, we neglect the hole-induced bond-breakage rates. The lack of the hole-induced component of the damage is compensated in our model by the common action of colder carriers and the dipole-field interaction, thereby leading to the important N_{it} peak inside the channel, which substantially affects the device characteristics.

The normalized experimental change of the linear and saturation drain currents simulated with the SHE- and DD-based versions of our HCD model is plotted together with the experimental data in Fig. 8 for a fixed gate voltage of $V_{gs} = 2$ V and a series of three different drain voltages: $V_{ds} = 18, 20$, and 22 V. One can see that the agreement

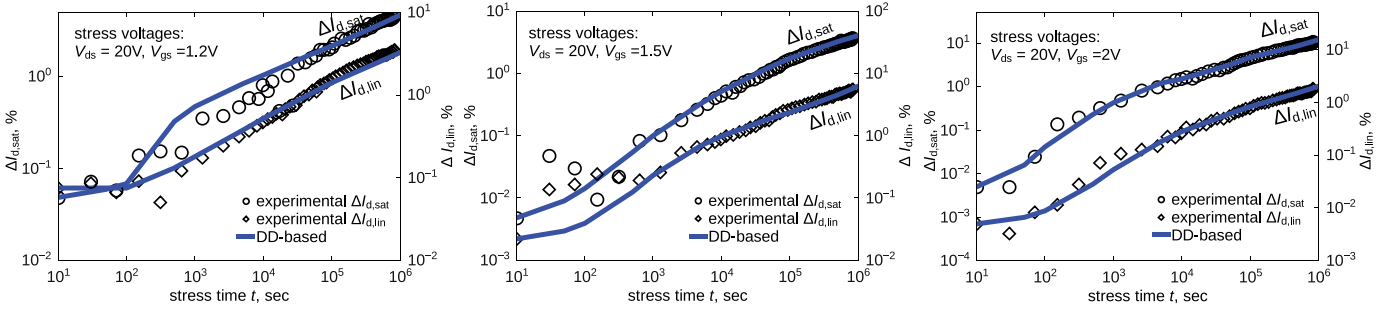


Fig. 10. Change in the saturation and linear drain currents: experiment versus the DD-based model. Results are obtained for a fixed drain voltage $V_{ds} = 20$ V and three different gate voltages $V_{gs} = 1.2, 1.5$, and 2 V.

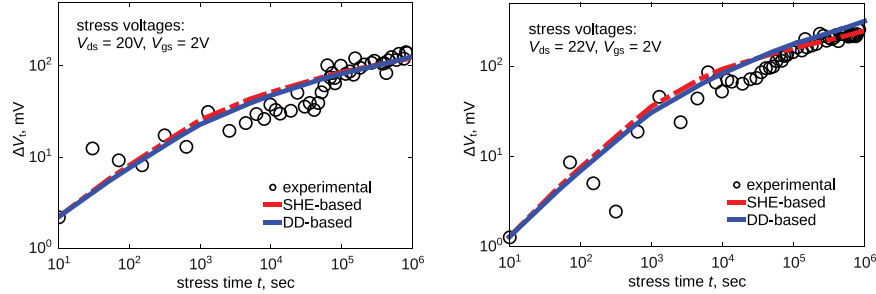


Fig. 11. Comparison of the change in the threshold voltage obtained from experiments and simulations, using the SHE- and DD-based models, for stress voltages $V_{gs} = 2$ V and $V_{ds} = 20$ and 22 V for stress times up to 1 Ms.

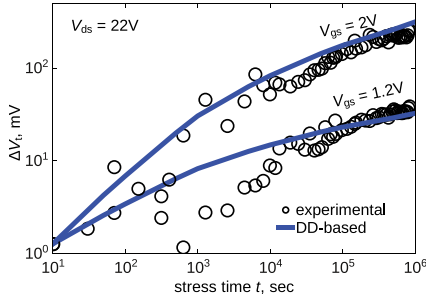


Fig. 12. Threshold voltage shift versus stress time. A comparison between experiment and the simulations with the DD-based model for a fixed drain voltage $V_{ds} = 22$ V and two different gate voltages $V_{gs} = 1.2$ and 2 V.

between the experimental results and the simulated data is very good. It is important to emphasize that the $\Delta I_{d,lin}(t)$ and $\Delta I_{d,sat}(t)$ curves obtained with the SHE- and DD-based versions of the model are almost the same within the whole experimental time window. This makes the latter version attractive for efficient and predictive HCD simulations of nLDMOS devices. Fig. 9 shows the $\Delta I_{d,lin}(t)$ and $\Delta I_{d,sat}(t)$ traces simulated with the DD-based version of the model with and without the effect of mobility degradation (15). One can see that for the entire stress time window, the current degradation simulated considering only the electrostatics perturbation due to the interface state buildup is substantially underestimated.

To check the DD-based model in greater detail, we plot the normalized changes in the linear and saturation drain currents simulated exclusively with the DD-model for a fixed $V_{ds} = 20$ V and three different $V_{gs} = 1.2, 1.5$, and 2 V

in Fig. 10. It is worth emphasizing that the DFs used for the data in Fig. 10 are obtained with the DD-based approach without additional tuning of the parameters in order to mimic the ViennaSHE results. We conclude that the agreement between the experimental data and the degradation traces is very good. This is also the case for the threshold voltage shifts $\Delta V_{th}(t)$ for $V_{gs} = 2$ V and $V_{ds} = 20$ and 22 V obtained with both versions of our HCD model and plotted versus the measured $\Delta V_{th}(t)$ traces, as shown in Fig. 11. Again, as in the case of the drain current degradation, we apply our DD-based model to represent $\Delta V_{th}(t)$ traces for $V_{ds} = 22$ and $V_{gs} = 1.2$ and 2 V without using the ViennaSHE DFs as a reference (Fig. 12), and observe good agreement between experiments and theory. We finally emphasize that all simulations were of course carried out with the same parameter set.

V. CONCLUSION

We have applied our physical model of the HCD to represent the degradation in an nLDMOS transistor. Two versions of the model have been examined, i.e., a version which employs the carrier DFs obtained from a deterministic BTE solver and one which uses the simpler DD approach. The electron DFs obtained with the DD-based model were compared with those simulated with the SHE approach and good agreement between them was shown. Although some discrepancy between the DFs computed with these two models is visible in the drain region, this discrepancy was shown to not translate into an error in the DD-based HCD model. Such a conclusion can be drawn based on the good agreement between the carrier AIs evaluated with the two versions of

the model for both single- and multiple-carrier processes of Si-H bond dissociation. The corresponding interface state density profiles are also almost identical for a wide range of stress times and stress conditions.

The degradation of the linear and saturation drain currents and the threshold voltage shift were represented by both versions of our model for different combinations of drain and gate voltages using a unique set of parameters. Good agreement between the results obtained with SHE- and DD-based versions of the model suggests that the efficient DD model is well suited for describing the HCD in nLDMOS devices.

REFERENCES

- [1] S. Reggiani *et al.*, "Characterization and modeling of electrical stress degradation in STI-based integrated power devices," *Solid-State Electron.*, vol. 102, no. 12, pp. 25–41, 2014.
- [2] S. Manzini and A. Galliano, "Avalanche injection of hot holes in the gate oxide of LDMOS transistors," *Solid-State Electron.*, vol. 44, no. 7, pp. 1325–1330, 2000.
- [3] D. Brisbin, A. Strachan, and P. Chaparala, "1-D and 2-D hot carrier layout optimization of N-LDMOS transistor arrays," in *Proc. IEEE Int. Integr. Rel. Workshop Final Rep. (IIRW)*, Oct. 2002, pp. 120–124.
- [4] P. Moens, G. Van den Bosch, and G. Groeseneken, "Competing hot carrier degradation mechanisms in lateral n-type DMOS transistors," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar./Apr. 2003, pp. 214–221.
- [5] S. Tyaginov, I. Starkov, H. Enichlmair, J. Park, C. Jungemann, and T. Grasser, "Physics-based hot-carrier degradation models (invited)," *ECS Trans.*, vol. 35, no. 4, pp. 321–352, 2011.
- [6] S. Tyaginov and T. Grasser, "Modeling of hot-carrier degradation: Physics and controversial issues," in *Proc. IEEE Int. Integr. Rel. Workshop Final Rep. (IIRW)*, Oct. 2012, pp. 206–215.
- [7] S. E. Rauch and G. La Rosa, "The energy-driven paradigm of NMOSFET hot-carrier effects," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 4, pp. 701–705, Dec. 2005.
- [8] C. Guerin, V. Huard, and A. Bravaix, "The energy-driven hot-carrier degradation modes of nMOSFETs," *IEEE Trans. Device Mater. Rel.*, vol. 7, no. 2, pp. 225–235, Jun. 2007.
- [9] S. Rauch and G. La Rosa, "CMOS hot carrier: From physics to end of life projections, and qualification," in *Proc. Int. Rel. Phys. Symp. (IRPS)*, 2010.
- [10] Y. M. Randriamihaja *et al.*, "Microscopic scale characterization and modeling of transistor degradation under HC stress," *Microelectron. Rel.*, vol. 52, no. 11, pp. 2513–2520, 2012.
- [11] S. Tyaginov *et al.*, "A predictive physical model for hot-carrier degradation in ultra-scaled MOSFETs," in *Proc. Int. Conf. Simulation Semiconductor Process. Devices (SISPAD)*, Sep. 2014, pp. 89–92.
- [12] M. Bina *et al.*, "Predictive hot-carrier modeling of n-channel MOSFETs," *IEEE Trans. Electron Devices*, vol. 61, no. 9, pp. 3103–3110, Sep. 2014.
- [13] Y. Wimmer *et al.*, "Physical modeling of hot-carrier degradation in nLDMOS transistors," in *Proc. IEEE Int. Integr. Rel. Workshop Final Rep. (IIRW)*, Oct. 2014, pp. 58–62.
- [14] S. E. Tyaginov *et al.*, "Interface traps density-of-states as a vital component for hot-carrier degradation modeling," *Microelectron. Rel.*, vol. 50, nos. 9–11, pp. 1267–1272, 2010.
- [15] S. Tyaginov *et al.*, "Secondary generated holes as a crucial component for modeling of HC degradation in high-voltage n-MOSFET," in *Proc. Int. Conf. Simulation Semiconductor Process. Devices (SISPAD)*, Sep. 2011, pp. 123–126.
- [16] Y. M. Randriamihaja *et al.*, "Hot carrier degradation: From defect creation modeling to their impact on NMOS parameters," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2012, pp. XT.15.1–XT.15.4.
- [17] T. Grasser, T.-W. Tang, H. Kosina, and S. Selberherr, "A review of hydrodynamic and energy-transport models for semiconductor device simulation," *Proc. IEEE*, vol. 91, no. 2, pp. 251–274, Feb. 2003.
- [18] S. Tyaginov, I. Starkov, C. Jungemann, H. Enichlmair, J.-M. Park, and T. Grasser, "Impact of the carrier distribution function on hot-carrier degradation modeling," in *Proc. Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2011, pp. 151–154.
- [19] S. Reggiani *et al.*, "Physics-based analytical model for HCS degradation in STI-LDMOS transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 3072–3080, Sep. 2011.
- [20] H. G. Reik and H. Risken, "Distribution functions for hot electrons in many-valley semiconductors," *Phys. Rev.*, vol. 124, pp. 777–784, Nov. 1961.
- [21] D. Cassi and B. Ricco, "An analytical model of the energy distribution of hot electrons," *IEEE Trans. Electron Devices*, vol. 37, no. 6, pp. 1514–1521, Jun. 1990.
- [22] K. Hasnat *et al.*, "Thermionic emission model of electron gate current in submicron NMOSFETs," *IEEE Trans. Electron Devices*, vol. 44, no. 1, pp. 129–138, Jan. 1997.
- [23] S. Reggiani *et al.*, "TCAD simulation of hot-carrier and thermal degradation in STI-LDMOS transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 691–698, Feb. 2013.
- [24] S. Reggiani *et al.*, "TCAD predictions of linear and saturation HCS degradation in STI-based LDMOS transistors stressed in the impact-ionization regime," in *Proc. 25th ISPSD*, May 2013, pp. 375–378.
- [25] A. Haggag, W. McMahon, K. Hess, K. Cheng, J. Lee, and J. Lyding, "High-performance chip reliability from short-time-tests-statistical models for optical interconnect and HCI/TDDDB/NBTI deep-submicron transistor failures," in *Proc. 39th Annu. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2001, pp. 271–279.
- [26] W. McMahon, K. Matsuda, J. Lee, K. Hess, and J. Lyding, "The effects of a multiple carrier model of interface trap generation on lifetime extraction for MOSFETs," in *Proc. Int. Conf. Modeling Simulation Microsyst.*, vol. 1, 2002, pp. 576–579.
- [27] W. McMahon and K. Hess, "A multi-carrier model for interface trap generation," *J. Comput. Electron.*, vol. 1, no. 3, pp. 395–398, 2002.
- [28] A. Haggag, M. Lemanski, G. Anderson, P. Abramowitz, and M. Moosa, "Realistic projections of product F_{max} shift and statistics due to HCI and NBTI," in *Proc. 45th Annu. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2007, pp. 93–96.
- [29] A. Bravaix, C. Guerin, V. Huard, D. Roy, J.-M. Roux, and E. Vincent, "Hot-carrier acceleration factors for low power management in DC-AC stressed 40 nm NMOS node at high temperature," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2009, pp. 531–548.
- [30] S. Tyaginov *et al.*, "Physical modeling of hot-carrier degradation for short- and long-channel MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Jun. 2014, pp. XT.16.1–XT.16.8.
- [31] (2014). *ViennaSHE*. [Online]. Available: <http://viennashe.sourceforge.net>
- [32] *Sentaurus Process, Advanced Simulator for Process Technologies*, Synopsys, Inc., Mountain View, CA, USA.
- [33] *MINIMOS-NT Device and Circuit Simulator*, Inst. Microelectron., TU Wien, Vienna, Austria.
- [34] *MiniMOS-NT*. [Online]. Available: <http://www.globaltcad.com/en/products/minimos-nt.html>, accessed May 2014.
- [35] (2014). *ViennaMesh*. [Online]. Available: <http://viennamesh.sourceforge.net/>
- [36] C. Jungemann and B. Meinerzhagen, *Hierarchical Device Simulation*. New York, NY, USA: Springer-Verlag, 2003.
- [37] M. V. Fischetti and S. E. Laux, "Monte Carlo study of sub-band-gap impact ionization in small silicon field-effect transistors," in *Proc. Int. Electron Devices Meeting (IEDM)*, Dec. 1995, pp. 305–308.
- [38] S.-M. Hong, A.-T. Pham, and C. Jungemann, *Deterministic Solvers for the Boltzmann Transport Equation*. Vienna, Austria: Springer-Verlag, 2011.
- [39] S. E. Tyaginov *et al.*, "Hot-carrier degradation modeling using full-band Monte-Carlo simulations," in *Proc. 17th IEEE Int. Symp. Phys. Failure Anal. Integr. Circuits (IPFA)*, Jul. 2010, pp. 1–5.
- [40] K. Rupp, T. Grasser, and A. Jüngel, "On the feasibility of spherical harmonics expansions of the Boltzmann transport equation for three-dimensional device geometries," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2011, pp. 34.1.1–34.1.4.
- [41] K. Rupp, P. W. Lagler, T. Grasser, and A. Jüngel, "Inclusion of carrier-carrier-scattering into arbitrary-order spherical harmonics expansions of the Boltzmann transport equation," in *Proc. 15th Int. Workshop Comput. Electron. (IWCE)*, May 2012, pp. 1–4.
- [42] K. Rupp, M. Bina, Y. Wimmer, A. Jüngel, and T. Grasser, "Cell-centered finite volume schemes for semiconductor device simulation," in *Proc. Int. Conf. SISPAD*, Sep. 2014, pp. 365–368.
- [43] T. Grasser, H. Kosina, C. Heitzinger, and S. Selberherr, "Accurate impact ionization model which accounts for hot and cold carrier populations," *Appl. Phys. Lett.*, vol. 80, no. 4, pp. 613–615, 2002.

- [44] T. Grasser, H. Kosina, C. Heitzinger, and S. Selberherr, "Characterization of the hot electron distribution function using six moments," *J. Appl. Phys.*, vol. 91, no. 6, pp. 3869–3879, 2002.
- [45] H.-S. Wong, M. H. White, T. J. Krutsick, and R. V. Booth, "Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET's," *Solid-State Electron.*, vol. 30, no. 9, pp. 953–968, 1987.
- [46] A. P. G. Prakash, S. C. Ke, and K. Siddappa, "High-energy radiation effects on subthreshold characteristics, transconductance and mobility of n-channel MOSFETs," *Semicond. Sci. Technol.*, vol. 18, no. 12, pp. 1037–1042, 2003.
- [47] E. Riedlberger, C. Jungemann, A. Spitzer, M. Stecher, and W. Gustin, "Comprehensive analysis of the degradation of a lateral DMOS due to hot carrier stress," in *Proc. IEEE Int. Integr. Rel. Workshop Final Rep. (IIRW)*, Oct. 2009, pp. 77–81.
- [48] D. Varghese, P. Moens, and M. A. Alam, "ON-state hot carrier degradation in drain-extended NMOS transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2704–2710, Oct. 2010.

Authors' photographs and biographies not available at the time of publication.