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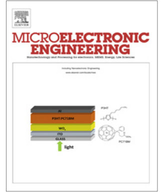

Coupled simulation to determine the impact of across wafer variations in oxide PECVD on electrical and reliability parameters of through-silicon vias

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ABSTRACT

We demonstrate a coupled equipment- and feature-scale process simulation and its application to plasma-enhanced chemical vapor deposition (PECVD) as part of a sequence for the fabrication of a through-silicon via (TSV) interconnect. The TSV structure is characterized electrically and mechanically by means of finite element simulation. This chain allows one to determine the effects of process variations on the electrical and reliability characteristics of the TSV. The simulations predict an across wafer variation of the parasitic DC capacitance between the tungsten metallization and the silicon substrate of about 3%. However, mechanical simulations indicate only a minor influence of the oxide layer thickness variation on the reliability performance of the TSV.

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1. Introduction

Three-dimensional (3D) integration of different semiconductor technologies is a key challenge for the future evolution of enhanced electron devices and systems by increasing the density of components and integrating broader functionality into a single integrated circuit. Through-silicon via (TSV) technology creates a direct electrical path through the entire silicon substrate between, for instance, high-impedance sensors and their associated analog frontend or to a bond/bump pad for stacking to another silicon circuit. Such a structure is generated through a sequence of multiple etching and deposition steps after the CMOS processing including metallization has been completed.

Variability of the processing parameters of these etching and deposition steps, including the variability across the wafer, leads to changes of key TSV geometry parameters such as aspect ratio and thicknesses of deposited layers which strongly influence the electrical and reliability properties of the TSV. In this work, a coupled equipment- and feature-scale process simulation and its application to layer deposition as part of a sequence for the fabrication of TSVs is demonstrated. The resulting structures are studied with respect to their electrical characteristics and reliability by means of finite element (FEM) simulations.

2. Modeling of the PECVD process for SiO_2 deposition

Part of the processing sequence studied is the plasma-enhanced chemical vapor deposition (PECVD) of a SiO_2 layer in a capacitively coupled plasma (CCP) reactor. In this work, the profile of the deposited SiO_2 layer and its variation across the wafer is investigated by means of simulation. To model the deposition process it is assumed that the adsorbed TEOS fragments are saturated on the surface and that the process is therefore governed by the local fluxes of oxygen ions and radicals [1]. The equipment modeling of a PECVD reactor containing argon and oxygen has been carried out using the Q-VT [2] software which is based on the plasma process simulator HPEM [3]. The reactor studied is a CCP reactor with the gas showerhead as one electrode at the top and the wafer carrier platen as the other electrode. This configuration leads to a maximum ion concentration in the approximate middle between the two electrodes. In the simulation, each of the two electrodes was

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powered with 100 W using a dual-frequency system with 20 MHz for the showerhead electrode and 4 MHz for the wafer carrier platen electrode. For the simulation, the pressure and the mass flow were set to 40 mTorr and 100 sccm, respectively. The mass flow supplied through the showerhead electrode consists of molecular oxygen (95%) and argon (5%). The most important species for the deposition process to be considered in the feature-scale simulation are the oxygen radicals and O_2^+ ions. As an example, Fig. 1 shows the simulated reactor along with the concentration of the O_2^+ ions. Fig. 2 shows the fluxes of oxygen radicals and O_2^+ ions at the substrate versus the distance from the reactor center axis. These fluxes are provided as a boundary condition for feature-scale modeling.

In order to simulate profile evolution on the feature scale, a phenomenological model [4] is employed which describes the local deposition rate R as a composition of contributions from neutrals and ions:

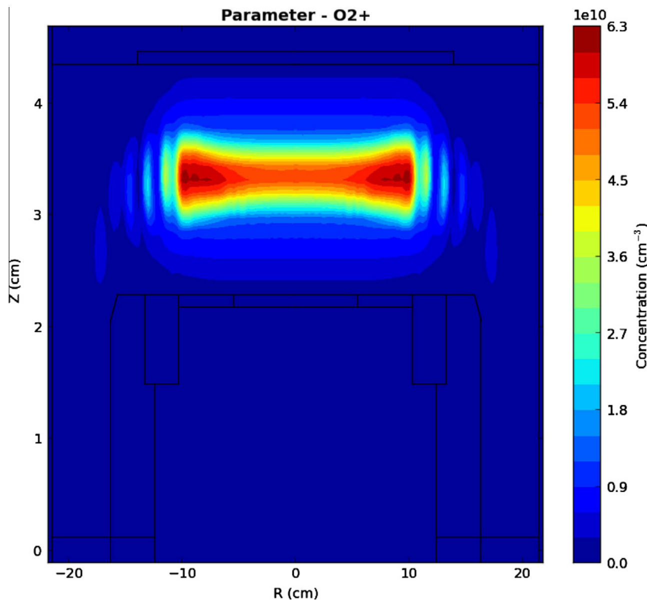

Fig. 1. Equipment simulation result (O_2^+ ions) for a PECVD reactor. The total mass flow and the pressure are 100 sccm and 40 mTorr, respectively. The electrical power (dual-frequency) is 200 W. The substrate (200 mm wafer) is placed on top of the block in the center of the figure. Please note the different scales on R and Z axis which have been chosen for better visualization. The black lines in the figure denote the geometry of the reactor, showing the showerhead electrode at the top and the wafer carrier platen in the middle. For the simulation, a rotationally symmetric geometry has been assumed, a cross section of which is shown in the figure.

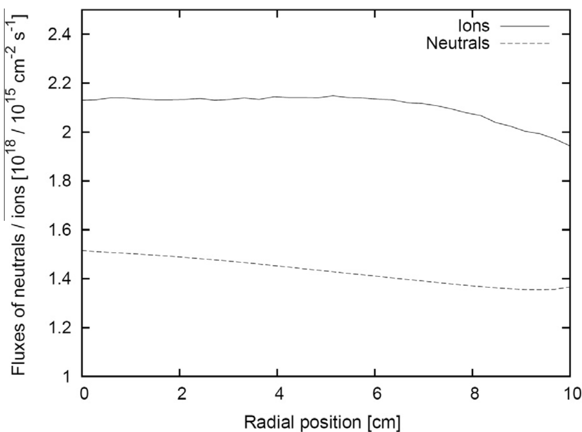

Fig. 2. Fluxes of oxygen neutrals (radicals) and O_2^+ ions at the substrate versus distance from the center axis for the equipment simulation shown in Fig. 1.

$$R \sim s_c\, F_{\mathrm{neutral}} + F_{\mathrm{ion}} \quad (1)$$

where s_c, F_{neutral}, and F_{ion} are the sticking coefficient of the neutrals, the flux of the neutrals, and the flux of the ions, respectively. The parameters of the model are the relative contribution r of the neutrals to the growth rate in planar sections, the sticking coefficient of the neutrals, and the standard deviation σ of the angular distribution of the ions. In the model [4], separate paths leading to deposition due to the interaction of the surface with neutrals and ions are assumed.

The model is implemented into the in-house tool DEP3D [5]. Due to the absence of actual rate and profile data, for the position on the center axis of the reactor (at 0.0 cm) a typical feature-scale model parameter set (r = 0.8, s_c = 0.15, σ = 0.1) according to literature [4] has been used. This can be justified by the fact that this work focuses on the across wafer variations of the model parameters rather than on their absolute values. The variations of the fluxes allow one to determine the variation of the feature-scale model parameters when varying the feature position on the wafer and to simulate the resulting profiles. The variation of the model parameter r can be calculated according to:

$$r = \frac{1}{1 + k_r \frac{F_{\mathrm{ion}}}{F_{\mathrm{neutral}}}}, \quad (2)$$

where k_r is a parameter which needs to be determined for a given position, for instance the center of the wafer, by imposing a value for r. The parameter k_r does not vary with varying fluxes, as it is a constant depending only on the proportionality constants according to Eq. (1). In other words, the logic train is as follows: the typical parameter r as mentioned above is assumed for the position at the center of the wafer. The fluxes F_{ion} and F_{neutral} as determined by equipment simulation allow the calculation of k_r according to Eq. (2). Since k_r is constant, the variations of the fluxes F_{ion} and F_{neutral} across the wafer allow one to calculate the variation of r across the wafer according to Eq. (2).

Additionally, the changes of the growing thickness when varying the feature position on the wafer can be determined according to:

$$R = k_{\mathrm{rate}}(F_{\mathrm{neutral}} + k_r F_{\mathrm{ion}}), \quad (3)$$

where R is the thickness growing in one-dimensional regions of the structure. k_{rate} is a model parameter which does not depend on the fluxes [4]. Therefore, using Eq. (3) the relative changes of the growth rate can be ascertained by determining the changes of the fluxes F_{neutral} and F_{ion}.

As an example, the simulated profiles of a layer deposited by oxide PECVD are shown in Fig. 3. In order to determine the variations of the model parameters, the typical parameter set mentioned above (r = 0.8, s_c = 0.15, σ = 0.1) has been assigned to the position at the center of the wafer. Using Eqs. (2) and (3), the changes of r and R across the wafer have been calculated. For instance, for a position at the wafer rim (radial position of 10 cm), a value for r of 0.8 and a growing thickness which is equal to 0.9 times the growing thickness at the center of the wafer are obtained. Therefore, for the example studied here, the profile change is due to the change of the growing thickness rather than due to the change of the conformality (governed by the parameter r in addition to s_c which is assumed to be independent of the local fluxes). For other reactor configurations leading to different variations of the fluxes of neutral and ions across the wafer, this behavior can differ.

To study the impact of the changes of the PECVD oxide profile on the electrical and reliability performance, a process sequence for the fabrication of a TSV structure [6] has been studied. The simulated TSV geometry relies on 2D/3D simulations (with the assumption of rotational symmetry) as shown in Fig. 4. It should

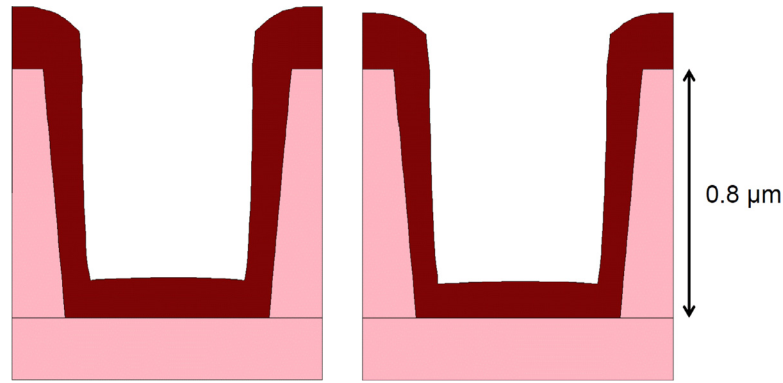

Fig. 3. Simulated profiles (cross sections) of PECVD oxide layers deposited into rotationally symmetric contact holes at different positions on the wafer. The dark red region corresponds to the deposited oxide layer. The left side and the right side show the profiles at the wafer center and at the wafer rim (radial position of 10 cm), respectively. The difference of the growing thickness on top is 10% with respect to the value for the position at the wafer center. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

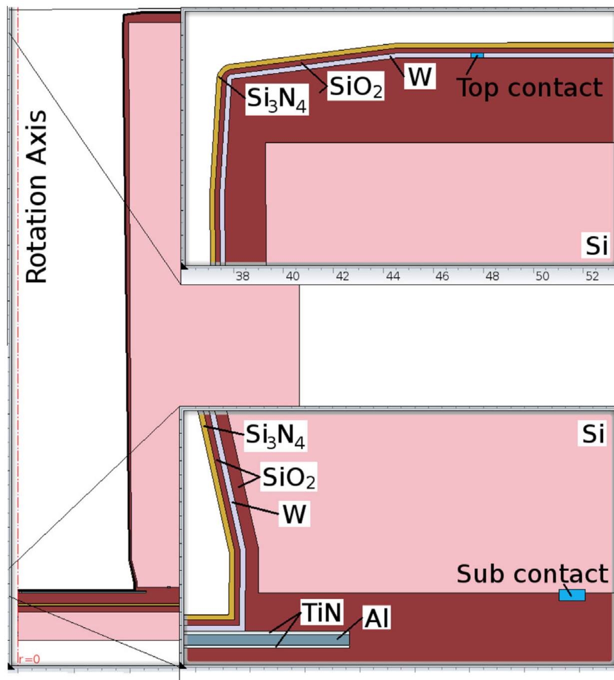

Fig. 4. Simulated TSV structure. The left part shows one half of the via cross section, with close ups on the right. The changing thickness from top to bottom of the oxide layer between silicon and tungsten is clearly visible.

also be noted that the TSV sidewalls are assumed to be flat and only the effect of notching at the bottom of the hole is included. The scallops which can be present on the sidewalls due to the etching process and which may have an additional influence on the electrical performance [7] are not included in order to reduce simulation complexity. The aspect ratios between the thin sidewall materials (W, SiO_2, Si_3N_4) and the thicker isolation oxide and silicon make the meshing of the full 3D structure unfeasible.

The PECVD layer forms part of the complete oxide layer in addition to SACVD (sub-atmospheric chemical vapor deposition) layers. The latter ones have been modeled using the single-precursor model for chemical vapor deposition described previously [8]. It has to be noted that equipment related variations for the SACVD processes which are not part of this study can also contribute to variations of the structures and thus of the electrical performance. Therefore, the variations derived for the PECVD part of the oxide deposition shown in this work need to be complemented by the SACVD variations. Theoretically, the dependence on the wafer position could become more or less pronounced, depending on the influence of the wafer position in the SACVD process. In addition to the variations due to the deposition processes themselves, variations of the etching profile across the wafer can have an impact on the layer profiles and on the performance of the TSVs.

3. Electrical and mechanical modeling of the TSV structures

The simulated structures for the different positions on the wafer were provided to FEM simulation for electrical and reliability characterization using COMSOL Multiphysics 4.3a with an adaptation to include a compact electromigration model [9]. The model determines the growth of the electromigration-induced stress at the initial stages of electromigration. Once the critical stress – a material dependent property – is reached, the material is said to contain a nucleated void, which has the potential to grow and cause an increase in the TSV resistance and eventual failure.

3.1. Modeling the electrical performance of the TSV structures

The variation of neutral and ion fluxes with varying radial position, shown in Fig. 2, results in a variation in the deposited oxide thickness, which in turn, causes the TSV parasitic capacitance to depend on the TSV position on the wafer. This is shown in Fig. 5 (bottom), where it becomes clear that the TSVs placed at locations exhibited to lower neutral and ion fluxes have an increased parasitic capacitance. The DC capacitance variation amounts to about 3% between wafer center and wafer rim. The frequency dependence of the TSV capacitance can be seen in Fig. 5 (top), where the simulation is performed using a boron-doped bulk silicon ($2.15 \cdot 10^{15}$ cm^{-3}). The high-frequency parasitic capacitance does not vary significantly between the differently-located TSVs, as is expected since at high frequencies the devices leave the capacitive and enter the resistive region of operation, which depends less on the oxide thickness [10]. This simulation enables a small-signal analysis of the TSV, depicted as an LRC circuit, with an extracted resistance and inductance of approximately 400 mΩ and 4.3 pH, respectively.

3.2. Modeling the electromigration-induced stress through the TSV

Figs. 6–8 show the reliability performance of the TSV located at the center, whose profile can be seen in Fig. 4 (left). The electromigration simulations are performed for an applied current of 1 A at a

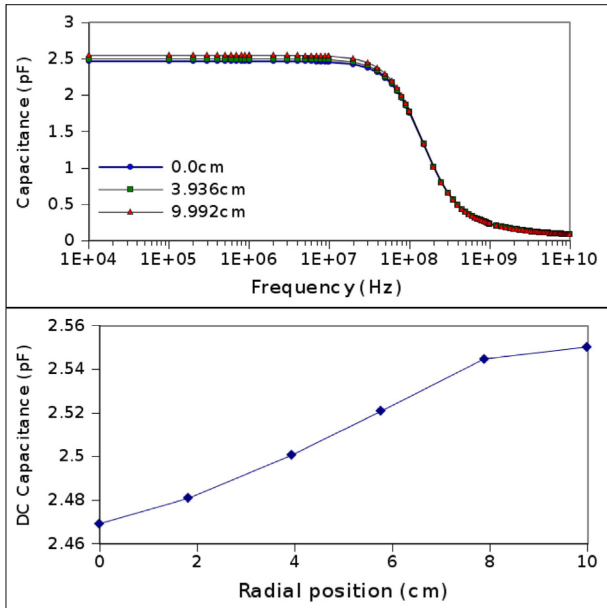

Fig. 5. Simulated TSV capacitance between the *Top* contact and the *Sub* contact from Fig. 4. The top figure shows the frequency dependence of the capacitance. The bottom figure shows the radial position dependence of the capacitance at 0 Hz.

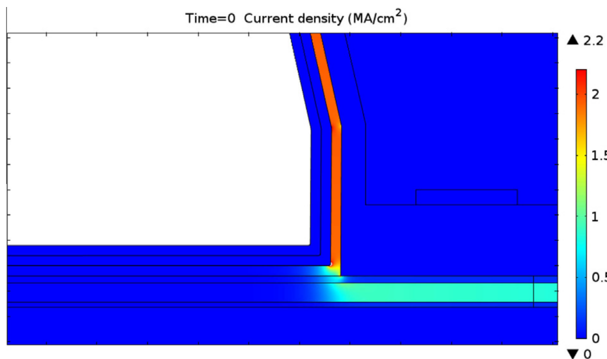

Fig. 6. Simulation of the current density distribution, when a current of 1 A is applied to the TSV depicted in Fig. 4. The aluminum layer experiences a current density of approximately 1 MA/cm^2.

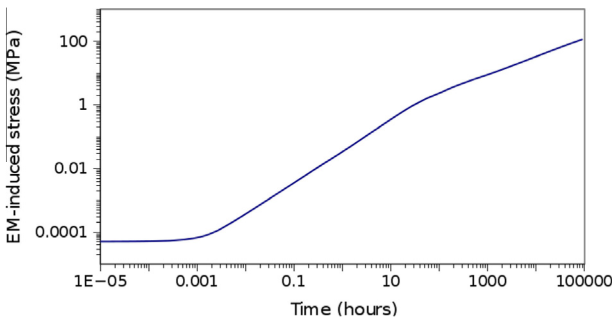

Fig. 7. Simulation of the electromigration-induced stress in the aluminum layer, when a current of 1 A is applied to the TSV depicted in Fig. 4. The current density through the metal layers is shown in Fig. 6. The aluminum layer experiences a current density of approximately 1 MA/cm^2.

stress-free temperature to avoid thermal effects in the TSV. The resulting current density distribution through the bottom aluminum layer is shown in Fig. 6. The aluminum, being the material where electromigration-induced failure is of highest concern, experiences a maximum current density of approximately 1 MA/cm^2.

At this current density level, the evolution of the electromigration-induced stress over time is shown in Fig. 7. An analysis of the stress curve suggests that the stress evolution follows a pattern, already observed and modeled in dual-damascene interconnects [9]. The stress evolution is shown to experience an initial linear stress growth after approximately 10 s of operation, followed by a square root stress growth after approximately 30 h of operation. Therefore, the simulated stress response agrees well with the observed square root stress increase obtained by Korhonen [11]. Within the first 30 h of operation, an approximate stress of 30 MPa is reached. After this, the stress grows to approximately 100 MPa by the end of the 10 year simulation period.

The electromigration-induced stress at the end of the 10 year period is depicted in Fig. 8. A stress level of about 100 MPa is observed. This level does not vary with the TSV's location, because the stress level is affected by the movement of vacancies through the metal layers due to an applied current density. The observed variation of the oxide thickness is not large enough to significantly change the mechanical constraints of the aluminum line and thereby influence the electromigration response.

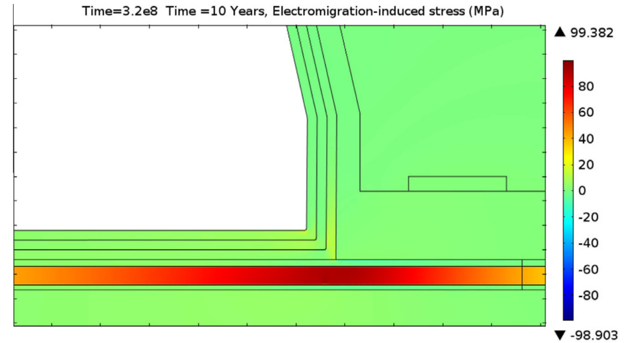

Fig. 8. Electromigration-induced stress of the TSV depicted in Fig. 4 with a current density distribution from Fig. 6. After 10 years of operation, the aluminum layer experiences a stress of approximately 100 MPa.

4. Conclusions

Process-induced variations have a significant impact on the operation of the fabricated devices or interconnect structures. To be able to capture the effect of manufacturing parameters on the resulting structures, equipment simulation is needed. The implementation of this analysis for a PECVD process has been demonstrated which needs treatment of a plasma process on the equipment as well as on the feature scale. The interface between both scales is based on transferring the relevant neutral and ion flux data. This allows one to study the influence of the equipment settings on the structure geometry. In the example presented, the influence of the feature position is considered. Further studies will also take into account for instance variations of equipment settings such as pressure, mass flow, or electrical power. Finally, by transferring the structures to a FEM simulation tool, the influence of the equipment parameters on quantities such as electrical characteristics or mechanical stress development has been analyzed.

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