# On The Fly Characterization of Charge Trapping Phenomena at GaN/Dielectric and GaN/AlGaN/Dielectric Interfaces Using Impedance Measurements

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***Abstract*—Charge trapping phenomena at interfaces of GaN–based semiconductors with a dielectric are one of the major concerns in modern MIS–HEMT technologies. Fundamental questions about the nature and the behavior of interface defects must still be answered. We address these questions by investigating devices with and without an AlGaN layer at the the interface with the dielectric, using MIS capacitor test structures.**

**We consider different methodologies to perform and analyze impedance measurements and the results are compared and discussed. Special attention is paid to the uncertainties and limitations inherent to different techniques, as well as the challenges due to the composite structure of GaN/AlGaN devices. We introduce an *on the fly* technique which allows the extraction of the device drift during stress. This enables us to suggest a lower and upper boundary for the amount of device degradation.**

**The experimental results indicate the presence of similar defects at GaN and AlGaN surfaces, which therefore appear to be intrinsic to the III–N material.**

## I. Introduction

Today, wide bandgap materials have attracted most of the interest and research effort of the semiconductor industry. The use of gallium–nitride (GaN) and composite aluminum–gallium–nitride (GaN/AlGaN) structures would bring many advantages because of the superior material properties.

Still, reliability problems challenge the technological development in this direction. Research groups focus their activities on trapping phenomena taking place in the bulk material [1]–[3] as well as at interfaces [4]–[7]. For metal–insulator–semiconductor (MIS) structures like high electron mobility transistors (HEMT) interface traps might play a key role. The questions to be answered regard the microscopic nature of such defects, their characteristic time constants and the transport mechanism from the charge carrier source through the gate stack to the defect states.

Many different techniques for the study of charge trapping have been developed during the past decades. Some of them study the response of devices to stress [4], continuous or pulsed between different bias points (stress–recovery experiments). Others aim to extract defect properties from impedance characteristic studying the frequency response in a small signal approximation [8], [9]. Our aim is to combine these two aspects, by investigating the role of large and small signal excitation on device drift.

## II. Experimental Details

The test structures used in this work are MIS capacitors as shown schematically in Fig. 1. Both GaN/dielectric and heterogeneous GaN/AlGaN/dielectric structures are used and compared. The peculiarity of the latter is the presence of a two–dimensional electron gas (2DEG) at the GaN/AlGaN interface. An additional Si–doped GaN ($10^{18}\,\mathrm{cm}^{-3}$) layer is inserted 100 nm deep into the unintentionally doped (UID) GaN, in order to provide enough carriers in devices without AlGaN. For the sake of comparison, the same doped layer is inserted in the GaN/AlGaN structures as well. The dielectric is a 50 nm thick SiN layer. The gate metal is made of aluminum, with circular shape of 50 µm diameter.

All measurements are performed with an Agilent 4294A impedance analyzer on test structures at wafer level. The data are taken between 500 Hz and 1 MHz, which is the range of frequencies for which it is possible to compensate for the parasitic effects of the cable extensions and the test fixtures.

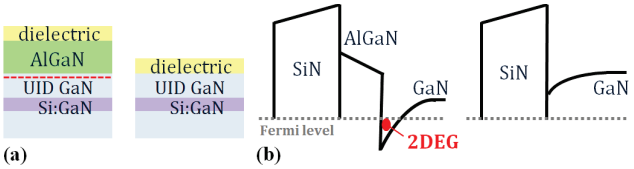


Fig. 1. (a) Schematic cross–section of the test structures. The red dashed line shows the position of the two–dimensional electron gas (2DEG). (b) Band diagrams (conduction edge only): the GaN/AlGaN structure is normally–on.

## III. Impedance Characteristic

In order to investigate trapping phenomena at the interface with the dielectric, the measured observable should be interpreted according to an appropriate model. We choose to study the impedance of MIS structures and its dependence on the gate large signal (DC) bias, as it reflects the charge distribution throughout the device. Varying the frequency of the applied small signal (AC) excitation we get information about the device frequency response. Also, this measurement can be performed on MIS capacitors as well as on fully processed HEMTs.

Common analysis techniques like Terman, conductance and transconductance methods [8], [9] make assumptions and approximations which must be carefully verified when used on GaN/AlGaN structures. The very first problem in applying such methods is the composite nature of GaN/AlGaN devices. An exhaustive treatment is required when modeling the capacitance–voltage (CV) characteristic of a MIS capacitor. It was shown that the behavior of the AlGaN layer changes in response to the applied bias [10]: below the *spill–over* voltage, it can

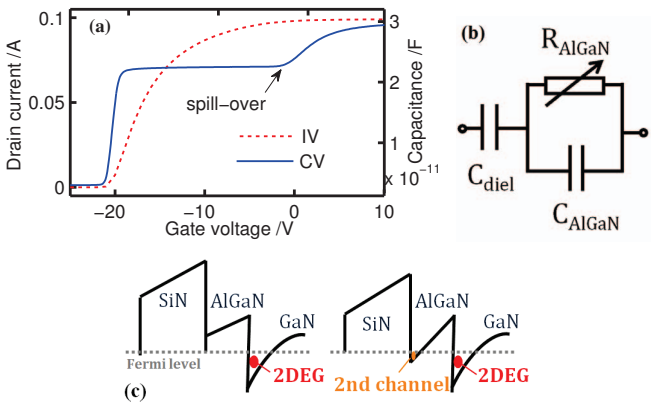


Fig. 2. (a) Typical capacitance–voltage curve (CV), compared with a transfer characteristic (IV) on a MIS–HEMT. (b) Circuit diagram model of the GaN/AlGaN MIS structure. (c) Band diagram before (left) and after (right) spill–over conditions.

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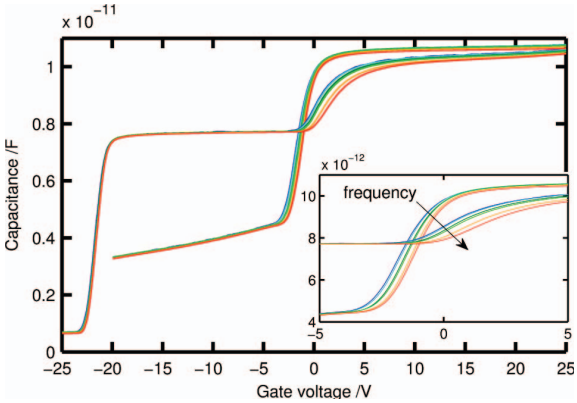


Fig. 3. CV characteristics at various frequencies, from 500 Hz to 1 MHz. The curve showing two steps is taken on a GaN/AlGaN structure, the curve with one step on a GaN–only capacitor. The inset provides a close–up of the region of interest.

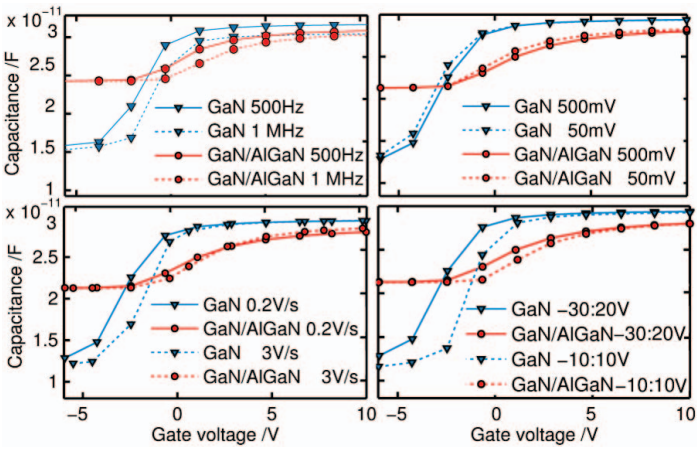


Fig. 4. Overview of CV dependence on measurement parameters. *Top left:* frequency; *top right:* oscillator level; *bottom left:* sweep rate; *bottom right:* sweep range.

be considered as an insulator, whereas it becomes conducting for higher values (Fig. 2a). This gives rise to the frequency dependent response depicted in Fig. 3. Good agreement with experimental data can be obtained by simulation using a circuit model which describes the AlGaN layer as a parallel resistor–capacitor (RC) branch (Fig. 2b) with a voltage dependent resistance [11]. The physical interpretation of this model is the creation of a second electron channel at the AlGaN/dielectric interface when the conduction band edge is pulled below the Fermi level (Fig. 2c). Under such conditions equilibrium is reached by electron transfer through the AlGaN layer. At the interface with the dielectric, electrons are easily trapped. The transport mechanism between the 2DEG and the second channel is still under debate [11], [12]. A correct model of the impedance characteristic should include this behavior, but unfortunately all existing methods assume a simpler structure assigning a certain impedance to the ensemble of traps at the interface [5]–[7]. This approximation does not allow to distinguish which part of the observed impedance is due to the electron transfer through the AlGaN layer and which to the trapping mechanism close to the dielectric.

The impedance characteristic shows a strong dependence on measurement conditions such as frequency, sweep rate, bias range and oscillator level. Fig. 4 shows an overview of the experimental conditions that influence the shape of capacitance–voltage measurements. Both structures with and without the AlGaN layer show similar capacitance– and conductance–voltage behavior when varying these parameters, as well as strong hysteresis (not shown). It is therefore reasonable that in both cases the response of trapped charge causes a frequency dependence, with an additional contribution from the transport through the AlGaN layer for composite structures.

Another important reason for device drift is the interaction with states in the GaN bulk (buffer traps) [2], [3]. This has a prominent effect in reverse bias conditions but is negligible in forward bias. Therefore we limit our measurements to positive polarity of the gate voltage in order to study interface states only.

## IV. Evaluating interface trapped charge

Since impedance characteristics depend heavily on measurement parameters, a direct analysis would lead to inaccurate estimation of defect properties. It is nevertheless possible to compare characteristics measured under the same conditions. Two complete CV sweeps on a fresh device and on a device stressed for 100 s at 10 V are shown in Fig. 5a. The regions which provide information about the effect of the stress are those around the first and the second increase of capacitance ($C_1$ and $C_2$), or around the first and the second peak of conductance ($G_1$ and $G_2$) as shown in Fig. 5b. Outside these intervals, impedance measurements are not sensitive to voltage drift.

The voltage drift is calculated by taking the difference of the two complete CV curves. For each value of capacitance, the corresponding bias values before and after stress are subtracted. The difference $\Delta V$ is plotted in Fig. 5c as a function of the gate voltage of the stressed CV curve. Drift information can only be obtained in the vicinity of $C_1$ and $C_2$. The $\Delta V$ around $C_1$ has a constant value for all points in the interval, while around $C_2$ it shows an increase followed by a decrease. In fact, in the first region we observe a parallel shift towards positive voltages (interpreted as trapping of negative charge at the interface with the dielectric), whereas in the second region the shift is combined with a certain distortion.

The voltage drift is also calculated as the distance between the positions of the conductance peaks. For comparison, the values $G_1$ and $G_2$ are shown in Fig. 5c. The value from the first peak gives the same information as the CV characteristic at $C_1$. The drift calculated from the second peak is instead slightly different. This is consistent with the fact that the properties of the AlGaN/dielectric interface are changed after stress, thus changing the conductance peak's position, magnitude or shape. We remark that a complete interpretation of the second conductance peak requires knowledge of both the AlGaN layer

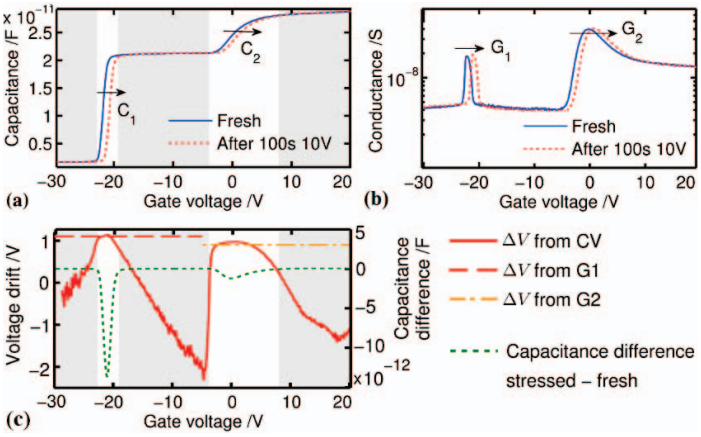


Fig. 5. (a) Capacitance and (b) conductance characteristic of a fresh GaN/AlGaN device and after 100 s at 10 V. (c) Voltage drift calculated by difference from the characteristics of Fig. 5a. The regions sensitive to the drift are around −21 V and from −3 V to 8 V (outside the shaded areas). These are the intervals where the capacitance difference between stressed and fresh CV is not zero. The values from $G_1$ and $G_2$ are calculated as the difference of the position of the conductance peaks maximum. The same information is obtained from the $C_1$ and the $G_1$ regions.

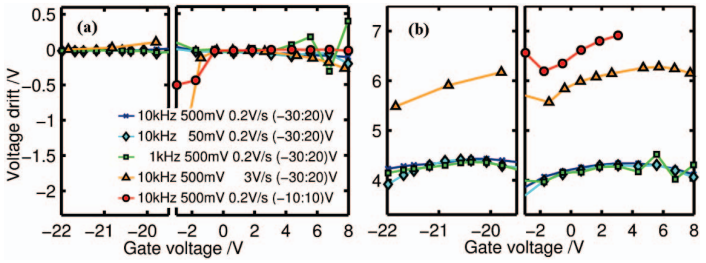


Fig. 6. (a) Voltage drift after 100 s at 0 V for various measurement conditions: frequency 1 kHz and 10 kHz, oscillator level 500 mV and 50 mV, sweep rate 0.2 V/s and 3 V/s, sweep range between −30 V and 20 V and between −10 V and 10 V. These variations do not affect the result: $\Delta V$ is zero in all cases. (b) The voltage drift after 100 s at 20 V stress is the same when varying small signal properties (frequency and oscillator level), but varies for different DC bias sweeping conditions (sweep rate and range).

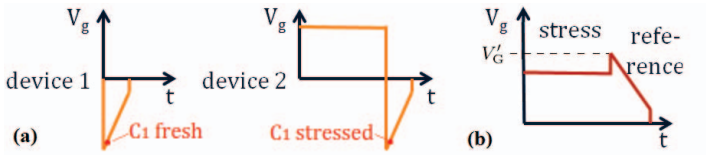


Fig. 7. Schematic representation of transient measurements: (a) comparison of the capacitance value at $C_1$ on a fresh device (left) and after stress on another device (right) with the MSM technique, and (b) recording impedance during stress, followed by a reference CV characteristic for the OTF approach.

and the AlGaN/dielectric interface frequency responses.

In order to validate this approach, we evaluate the impact of different measurement conditions on the calculated drift. We apply an AC signal alone to the device (DC bias is 0 V) and compare the sweep after a transient of 100 s with a fresh one, changing sweeping parameters. The result can be seen in Fig. 6a: the drift is not sensitive to frequency, oscillator level, sweep rate and sweep range.

We repeat the experiment applying a rather high DC stress bias of 20 V (Fig. 6b). Both tests prove that the AC signal has a negligible impact with respect to DC bias: the small signal approximation is valid. Conversely, sweeping conditions have a great influence on the calculated voltage drift when applying forward DC bias during stress because they cause additional stress.

In order to minimize such effects the impedance must be measured immediately after the stress transient. The inevitable delay between stress and impedance measurement is the intrinsic limitation of this approach. This is well studied on silicon technology, especially for MOSFETs subject to bias temperature instability [13]. We adopt the same nomenclature used in literature and call such an approach the measurement–stress–measurement technique (MSM). The principle of this method consists in recording the quantity of interest at the bias point which allows the highest sensitivity to voltage drift and minimizing the measurement delay, as shown in Fig. 7a. By properly choosing the voltage so that the first measured value lies between the depletion capacitance and the first plateau, one single point is enough to determine the shift of the CV curve. In our case, the measurement delay is about 250 ms.

The most suitable bias point for the measurement is around the first capacitance step, which corresponds to the threshold voltage of MIS–HEMTs [10]. Such gate bias corresponds to a recovery condition with respect to forward bias stress, therefore the device undergoes a partial recovery during the measurement delay. The obtained $\Delta V$ therefore results in an underestimation of the real value.

The same MSM approach is found in previous works and is used for impedance measurements [14] as well as drain current measurements on MIS–HEMTs to evaluate the threshold voltage drift [10].

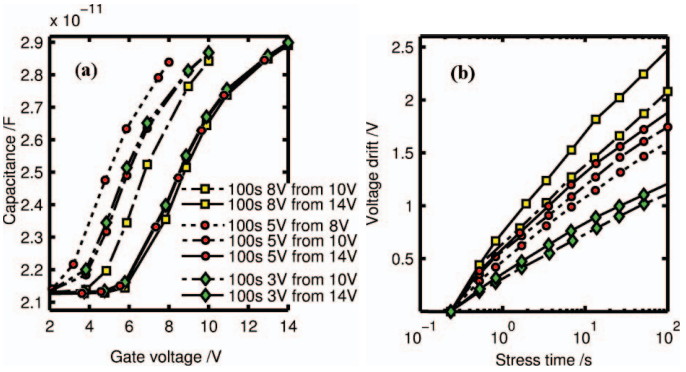


Fig. 8. (a) Reference curves measured by sweeping the gate voltage after stress from different $V'_G$ values (6 V, 10 V, 14 V) to zero. (b) Temporal evolution of drift during stress, as calculated using the reference curves shown on the left. The inaccuracy of the OTF method is due to the additional stress caused by the sweep measurement. The $\Delta V$ of the first measurement point is arbitrarily set to zero, since its real value is unknown.

## V. On the fly approach for transient measurement

Another way to determine the amount of drift is to calculate it directly from the transient data using a reference characteristic. The values of the transient at fixed voltage are compared to the values of a characteristic measured right afterwards, as sketched in Fig. 7b. This approach has the advantage to provide information about the $\Delta V$ from each experimental point measured during stress. For this reason it is called *on the fly* (OTF). It is assumed that the CV characteristic shifts parallel during the stress, so that the calculation of $\Delta V$ is possible from these two measurements on the same device. Such an assumption neglects the change in shape of the CV curve during stress. This procedure is used in various other investigations of threshold voltage drift of silicon MOSFETs subject to bias temperature instability [13], [15].

In order to have a reference that can be used for the whole transient, the first point is measured at a higher level of stress than the transient's fixed value. Fig. 8a shows the difference between curves with various gate voltage maximum values, $V'_G$. The additional stress has a prominent effect on the reference curve. The choice of $V'_G$ determines the amount of additional right shift after the stress transient. The qualitative comparison of different stress levels is independent on $V'_G$. However, changing its value from slightly above stress to larger values results in different amount of shift and distortion of the curve, which causes a large variation of the calculated $\Delta V$ with this method, as shown in Fig. 8b. The most reliable reference is the one which causes the least additional stress to the device. Of course, it is impossible to perform a CV measurement which does not add any additional stress. This is the limitation intrinsic to all OTF methods. The most accurate $\Delta V$ value calculated in this way is therefore the one with the smallest overestimation. This corresponds to the curve in Fig. 8b which leads to the smallest device drift.

Unfortunately, the amount of $\Delta V$ at the first measurement point is unknown. This is a systematic error due to a fundamental experimental limitation. Ideally, we expect a constant value of the capacitance for very short times. This would happen if we were able to measure the device impedance before trapping or transport phenomena start to play a role. However, we have never observed such an effect so far but always a behavior which is compatible with a linear relationship with the logarithm of time. This is consistent with previous investigations [10]. Therefore, we conclude that the time constants associated with those phenomena are approximately uniformly distributed even to times smaller than our measurement capabilities, similarly to what has been concluded for silicon transistors [16].

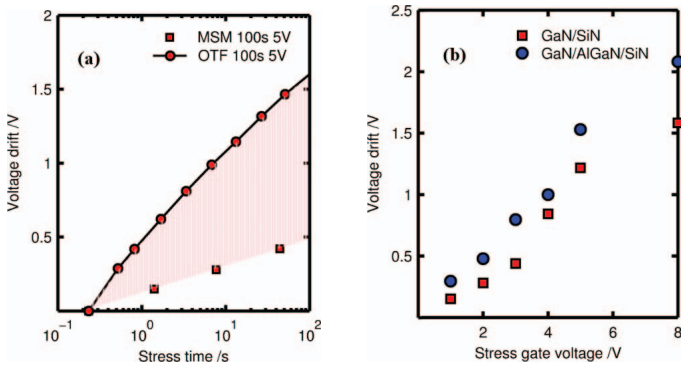


Fig. 9. (a) Device degradation during stress, calculated with MSM and OTF methods. The MSM technique strongly underestimates the drift value due to the partial recovery during the measurement delay; the OTF method, on the other hand, overestimates it because of the additional stress during the measurement of the reference and because the curve distortion is neglected. These quantities provide an upper and lower boundary for the real value of the device drift as shown by the shaded area. (b) Comparison of device drift after 100 s of forward bias stress on structures with and without the AlGaN layer, calculated with the OTF method for different values of stress gate voltage.

## VI. Discussion

We calculate the voltage drift after forward bias stress by CV curve comparison (MSM) and from the transient impedance data (OTF). The temporal evolution of $\Delta V$ for devices stressed at 5 V for 100 s is given in Fig. 9a.

The OTF method is sensitive to the overall influence of drift and distortion during stress at forward bias. We must use a reference CV curve which is subject to a small additional shift and distortion. While these contributions are indistinguishable from the effect of stress, the error can be minimized by tuning the sweeping parameters. A rather high sweep rate determines a small impact on the curve distortion and the starting gate voltage can be chosen small enough to cause the least additional stress still allowing $\Delta V$ calculation. Because of the limitations of this technique we can consider the OTF value as an upper limit of the real device drift, except for the offset due to the unknown $\Delta V$ value at the first measurement point.

The MSM method is subject to the opposite problem. By changing the bias abruptly to the $C_1$ region, the device is subject to recovery until the first point is measured. The voltage drift obtained in this way is therefore inevitably underestimated. In our case the delay is 250 ms at recovery bias. We believe that such relaxation affects the calculated $\Delta V$ value more severely than the additional stress of the OTF technique. However, the MSM approach provides a lower boundary of device drift. Its real value must lie in between the boundaries provided by the MSM and the OTF techniques.

Finally, a comparison between structures with and without AlGaN layer is made. We perform stress experiments with the OTF approach on both test structures, as shown in Fig. 9b. We observe similar properties of the interfaces of the dielectric with GaN and AlGaN. Both structures show frequency dispersion, strong hysteresis and a similar behavior after forward bias stress. This indicates that part of the device drift can be associated to defects at the interface between the III–N material and the dielectric. A recent experiment showed that the type of dielectric does not impact drift properties [17]: $\Delta V$ scales according to the dielectric constants and device geometry. From these observations we can conclude that the defects responsible for device drift must lie at the III–N material surface.

## VII. Conclusions

We show how to measure and compare impedance characteristic on GaN/AlGaN MIS structures. We point out the difficulties arising from the direct analysis of CV or conductance curves and the inaccuracies that can occur when determining the voltage drift from comparison of two impedance characteristics.

We suggest a reliable method to estimate device degradation which provides information *on the fly*, *i.e.* during stress transients, describing the necessary precautions to minimize all error sources.

Furthermore, we extract the temporal behavior of $\Delta V$ during stress. The results are consistent with a semilogarithmic dependence which has been found by previous experiments and other publications. We show that it is possible to suggest a lower and upper bound for the real value of voltage drift using different measurement techniques.

Finally, a comparison between GaN and GaN/AlGaN devices is made: observations indicate the presence of defects intrinsic to the III–N material surface, whose contribution to drift must be added to the transport phenomena in composite structures during spill–over conditions.

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