of the conductive filament during multiple switching cycles, we make use of the Ni-HfO2-Si based metal-insulator-semiconductor (MIS) stack with a transistor test structure so that the lateral location of the filament along the source to drain can be probed electrically by considering the weighted ratio of source and drain currents measured. Our analysis reveals that filaments can evolve in spatially uncorrelated locations and switching is not always caused by the same filament over and over again. A simple statistical model is also provided to justify the inferences of the electrical study. The probability of a new filament nucleating elsewhere in the dielectric is a strong function of the oxide barrier thickness as well as the curvature radii of the previously ruptured metal filament edges.

**OB1_3** - Physically-based extraction methodology for accurate MOSFET degradation assessment, *Giulio Torrente[1], Jean Coignus[2], Sophie Renard[1], Alexandre Vernhet[2], Gilles Reimbold[2], David Roy[1] and Gérard Ghibaudo[3] - [1]STMicroelectronics, [2]CEA, [3]IMEP*

**Abstract:** This paper analyzes the conventional parameter extraction methodologies applied for stressed MOSFET devices highlighting the complexity to accurately get and separate both electrostatic and transport degradations. The key point lies in an accurate Coulomb scattering assessment from the linear Id-Vg characteristics whenever the amount of interface charges/traps becomes significant. Thus, we propose and validate a novel technique that addresses easily a good estimation of the electrostatic drift and extracts the mobility at each gate potential directly from the experimental data without considering any model for the transport.

**OB1_4** - Statistics of Retention Failure in the Low Resistance State for Hafnium Oxide RRAM using a Kinetic Monte Carlo Approach, *Nagarajan Raghavan[1], Daniel Frey[2], Michel Bosman[3] and Kin Leong Pey[1] - [1]Singapore University of Technology and Design (SUTD,) [2]Massachusetts Institute of Technology (MIT), [3]A*STAR Institute of Materials Research and Engineering (IMRE)*

**Abstract:** Retention is one of the key reliability metrics for non-volatile memory devices. In oxygen ion transport based resistive switching memory (OxRAM), the retention phenomenon has been well studied from an electrical perspective and physical mechanisms explaining the origin of retention loss have also been speculated to support the observed data. However, the stochastic aspects of retention loss and its variability deserve to be investigated so that the time-dependent shift in the resistance distribution and the retention failure time statistics can be better quantified and estimated for a given set of operating conditions. We propose here a phenomenological Markovian multi-state model combined with the percolation framework and ion diffusion theory to analyze the distributions of retention failure in the low resistance state for OxRAM devices.

**OB1_5** - Comparison of Analytic Distribution Function Models for Hot-Carrier Degradation Modeling in nLDMOSFETs, *Prateek Sharma[1], Stanislav Tyaginov[1], Yannick Wimmer[1], Florian Rudolf[1], Karl Rupp[1], Hubert Enichlmair[2], Jong Mun Park[2], Hajdin Ceric[1] and Tibor Grasser[1] - [1]TU Wien, [2]AMS AG*

**Abstract**: We analyze the applicability of different analytic models for thecarrier distribution function (DF), namely the heated Maxwellian, the Cassi model, the Hasnat model, the Reggiani model, and our own approach,to describe hot-carrier degradation (HCD) in nLDMOS devices. As a reference, we also obtain the carrier distribution function as an exact solution of the Boltzmann transport equation. The DFs evaluated with these models are used to simulate the bond-breakage rates, the interface state density profiles and changes of such device characteristics as the linear and saturation drain currents as well as the threshold voltage. We show that the heated Maxwellian model leads to an underestimated HCD at long stress times. This trend is also typical for the Cassi and Hasnat models but in these models HCD is underestimated in the entire stress time window. As for the Reggiani model, it cannot properly represent the high-energy tails of the DF near the drain, and thus leads to a weaker curvature of the degradation traces. We show finally that our model is capable of capturing DFs with very good accuracy, and as a result the change of the device characteristics with stress time.

**OB1_6** - Reliability of high-speed SiGe:C HBT under electrical stress close to the SOA limit, *Thomas Jacquet[1], Grazia Sasso[2], Niccolo Rinaldi[2], Klaus Aufinger[3], Thomas Zimmer[1], Vincenzo d'Alessandro[2] and Cristell Maneux[1] - [1]IMS laboratory, University of Bordeaux, [2]Department of Electrical Engineering and Information Technology, University of Naples Federico II, [3]Infineon Technologies AG*

**Abstract:** The reliability of high-speed SiGe:C HBT under electrical stress close to the Safe Operating Area (SOA) limit is analysed and modeled. A long time stress test, up to 1000h, is performed at bias conditions chosen according to application targeted for these transistors. During the aging tests, Gummel plots are measured at fixed time to analyse the evolution of base and collector current. At low level injection, we observed an increase of the base current whereas the collector current remains constant for the whole Vbe range and during the 1000h aging time. By means of 2D TCAD simulations, this evolution of base current is attributed to trap activity at the emitter-base junction periphery. Based on TCAD simulation results, we propose an aging law using a differential equation that has been implemented in HiCUM L2 v2.33. This reliability-aware compact model should allow designers creating reliability-aware circuit architectures at an early stage of the design procedure, well before real circuits are actually fabricated.

- **POSTERS SESSION B1**

**PB1_1** - Wire width dependence of hot carrier degradation in silicon nanowire gate-all-around MOSFETs, *Jin Hyung Choi[1] and Jong Tae Park[2] - [1]Incheon National University, [2]Incheon national University*

**Abstract:** The increase of hot carrier degradation with decreasing wire width in nanowire gate-all-around (GAA) MOSFETs have been investigated though experiment and device simulation. From the systematical analysis of measurement and simulation, the increase of device degradation for narrow devices is dominantly governed by the increased current density, the larger lateral and vertical fields, and the increased interface state generation rather than by floating body effects. The increase of hot carrier degradation with decreasing wire width is likely to proportional to the surface-to-volume ratio of nanowires.

**PB1_2** - Electrical characterization of multiple leakage current paths in HfO2/Al2O3-based nanolaminates, *Alberto Rodriguez[1], Mireia Gonzalez[2], Jordi Suñe[1], Enrique Miranda[1] and Francesca Campabadal[2] - [1]Universitat Autonoma de Barcelona, [2]CNM*

**Abstract:** The generation of multiple leakage current paths in metal-insulator-semiconductor (MIS) structures with a HfO2/Al2O3-based nanolaminate grown by the ALD technique as insulator material was investigated. The devices were stressed at selected constant voltages in order to determine with a high accuracy the occurrence time of every single breakdown event in a time range spanning around 120 s. The final result of the experiment is a current-time characteristic with well-defined current steps. It is shown that using a