CMOS-Compatible Spintronic Devices

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***Abstract*— Silicon is perfectly suited for spin-driven applications. Recent progress and challenges regarding CMOS-compatible spin-based devices are reviewed. A realization of an intrinsic non-volatile logic-in-memory architecture in an MRAM array is demonstrated.**

***Index Terms*— Silicon spintronics, SpinFET, STT MRAM, non-volatile logic-in-memory**

I. Introduction

With CMOS miniaturization rapidly approaching its intrinsic limits a search for a new technology capable to compliment or replace CMOS is accelerating. The principle of MOSFET operation is fundamentally based on the charge degree of freedom of electrons. Another intrinsic electron property, the electron spin, attracts at present much attention as a possible candidate for complementing the charge degree of freedom in future devices [1]–[6]. The electron spin state is characterized by one of the two of its possible projections on a given axis and could be used in digital information processing. It takes a small amount of energy to invert the spin orientation, which is necessary for low power applications. The electron spin can be pointing in any direction on a unit Bloch sphere. This property is used in quantum computing, however, a successful implementation of such a computer based on spin qubits in silicon requires cryogenic temperatures [7].

The spin relaxation time for conducting electrons, describing the characteristic time of non-equilibrium spin relaxation towards its equilibrium value, is in the range of nanoseconds at room temperature [8], [9]. Thus, the spin diffusion length is in a micrometer range, and the spin of conducting electrons can be used to encode, transfer, and process information. In this case the electron spin degree of freedom is used in its binary mode. Importantly, transferring the spin information does not require a charge current flow. This decoupling of spin from charge makes the spin degree of freedom promising for low-power application.

The idea of complimenting or even replacing the charge degree of freedom by spin is around for almost three decades, even a demonstration of basic elements necessary for spin related applications, such as injection of spin-polarized currents in silicon, spin transport, spin manipulation, and detection, was missing until recently. Although it seems straightforward to inject spin-polarized carriers into silicon from a ferromagnetic contact, a fundamental conductivity mismatch between a ferromagnetic metal contact and silicon prevents spin injection. A special technique [10] based on the attenuation of hot electrons with spins anti-parallel to the magnetization of the ferromagnetic film allows creating an imbalance between the electrons with spin-up and spin-down in silicon, thus injecting spin-polarized current. The spin-coherent transport through the device was studied by applying an external magnetic field causing the precession of spins during their propagation from source to drain [1]. The detection is performed with a similar hot electron spin filter. The experimental set-up represents a first two-terminal spin-driven silicon device which can be envisaged working at room temperature. The first demonstration of coherent spin transport through an undoped 350μm thick silicon wafer [11] has triggered a systematic study of spin transport properties in silicon [6]. In the following we briefly review the recent progress in spin-driven applications based on silicon and CMOS-compatible devices.

II. Silicon Spin Field-Effect Transistor

A spin field-effect transistor (SpinFET) is composed of two ferromagnetic contacts (source and drain), linked by a non-magnetic silicon channel region. The ferromagnetic contacts inject and detect spin-polarized electrons, in analogy to polarizer and analyzer as indicated already long ago by Datta and Das [1]. Because of the effective spin-orbit interaction in the channel the spin of an electron injected from the source starts precessing. The electrons with spin, or to be more precise with the direction of the magnetic moment, aligned to the drain magnetization direction can easily leave the channel to the drain, thus contributing to the current. The total current through the device depends on the relative angle between the magnetization direction of the drain contact. An additional current modulation is achieved by tuning the strength of the spin-orbit interaction in the semiconductor region, which depends on the effective electric field and can be controlled by applying a gate voltage. In order to realize the SpinFET, an efficient spin injection, detection, and propagation must be possible [12]. A solution to the impedance mismatch problem preventing spin injection from a metal to a semiconductor is the introduction of a potential barrier between the metal ferromagnet and the semiconductor.

Two schemes to analyze the spin injection into a semiconductor are available [6]. A signal at room temperature obtained for both n- and p-doped silicon was documented in 2009 [13]. Electrical signals believed to be corresponding to spin injection through silicon dioxide at 500K have also been reported [14]. However, there is a several orders of magnitude discrepancy between the signal measured and the theoretical value. It turns out that the signal is stronger in three-terminal

measurements, while it is weaker in the non-local scheme [6]. Similar observations were also made for germanium as well as for other semiconductors [15]. Recently, the large amplitude of the signal observed in the three-terminal injection method was attributed to resonant tunneling through deep impurities [16]. The reasons for these discrepancies are heavily debated [6], [16]–[19].

The spin signal observed with the non-local scheme in degenerate silicon at room temperature [20] is believed to be due to a genuine spin injection. The amplitude of the signal is an order of magnitude weaker [6] than predicted by the theory, which is consistent with a possible spin polarization loss at the interfacial states in the ferromagnetic contacts. Spin transport in a non-degenerate n-doped silicon at room temperature was also successfully achieved [21]. Interestingly, the magnitude of the spin signal exceeds 1mV for a bias electric current of 1mA, ten times larger than previously reported for degenerate silicon.

For the functionality of a SpinFET the possibility to transfer the excess spin injected from the source to the drain electrode is essential. The excess spin, or more precisely the spin projection on a given axis, is not a conserved quantity, in contrast to charge. While diffusing, it gradually relaxes to its equilibrium value which is zero in a non-magnetic semiconductor. A good agreement between the experimentally observed and calculated spin life time as a function of temperature has been achieved in bulk silicon [8]. In contrast to the mobility, the spin relaxation depends significantly on the doping atom type in heavily doped silicon [22]. As it has been revealed in [9], [22], [23], the spin relaxation is due to the scattering between the valleys along different crystallographic axes (f-processes), while the electron mobility is determined by intravalley elastic scattering. Therefore, the momentum relaxation time is governed by the tail of the ionized impurity potential at large distances from an impurity, which is identical for donors considered in [22], while the spin relaxation is due to the short range impurity potential behavior where spin-orbit interaction is the strongest, thus giving rise to spin relaxation dependence on the doping atom type [22].

In confined electron systems of transistor channels the valley degeneracy, or rather the degeneracy between the two-dimensional subbands, is lifted due to different confinement energies for different valleys. It is well known that in (001) oriented silicon inversion channels the energy spectrum consists of primed and unprimed subbands. Despite partial degeneracy lifting in confined systems, the spin lifetime is significantly shorter in gated structures [24] due to the existence of the interface. Uniaxial stress applied along [110] direction is very efficient in boosting the spin lifetime in (001) silicon films. It turns out that the remaining two-fold degeneracy of the unprimed subbands is successfully lifted by shear strain efficiently produced by [110] stress. This reduces significantly the principal contribution to the spin relaxation in thin films due to surface roughness and acoustic phonons mediated g-type scattering between the equivalent valleys along the same crystallographic axis, or, more precisely, the intersubband spin relaxation. Stress techniques and especially uniaxial stress along [110] oriented channels are routinely used by the semiconductor industry to enhance the transistor performance. It is therefore very attractive to use the same well developed techniques to increase the spin lifetime. It makes the use of thin SOI films for spin applications very promising, because the spin lifetime is boosted by an order of magnitude.

Electric spin manipulation in silicon is possible, however, because the spin-orbit interaction in silicon is weak, the channel length needed to achieve a pronounced resistance modulation is close to a micrometer [25]. As efficient means of all-electric spin manipulation in silicon are yet to be discovered, the long spin lifetime and spin diffusion length allow to transfer the injected spin at large distances. This makes silicon attractive for use as efficient spin interconnects [26] in lateral spin valves and logic gates [27] known as all-spin logic [28]. Spin interconnects are critical for emerging spin-driven devices as they allow avoiding the spin-charge signal conversion thus reducing energy, delay, and circuitry.

For short silicon channels, the remaning option is to exploit the relative magnetic orientation of the source and drain ferromagnetic contacts [12]. This adds reprogrammability, when the information is additionally stored in the relative magnetization orientation of the source and drain. It is important that, once modified, the drain magnetization remains infinitely long without any extra power applied. However, the magnetoresistance ratio of 10% demonstrated so far at 12K for a 10μm long silicon [29] channel is not sufficient for applications. It is far inferior to the magnetoresistance ratio in magnetic tunnel junctions, where the two ferromagnetic metals are separated by a thin tunnel barrier.

III. Magnetic Tunnel Junctions and MRAM

Spins do not interact efficiently with electric fields. The use of magnetic fields for spin and magnetization manipulation is undesirable due to scaling restrictions for the wire cross-sections in magnetic coils. An efficient coupling between the magnetic and electric degree of freedom is achieved in magnetic tunnel junctions (MTJs) at the quantum mechanical level. In MTJs a high resistance difference between the parallel and anti-parallel relative magnetization orientation is reported. These structures are attractive for information storage as they allow reading the binary information by efficiently converting relative magnetization orientations into very distinct voltage signals. Importantly, a memory cell based on an MTJ is non-volatile, scalable, simple in structure, requires relatively low operating voltages, and exhibits low power consumption, high operation speed, and high endurance. The prediction [30], [31] of purely electrical switching of the magnetization by means of the spin transfer torque (STT) makes STT magnetic random access memory (MRAM) a promising candidate for future universal memory. Indeed, STT-MRAM is characterized by small cell size ($4F^2$) and high density inherent to DRAM, fast access time (less than 10ns) intrinsic to SRAM, non-volatility and long retention time subject to flash as well as high endurance (10^{14}). Most importantly, STT-MRAM is compatible with CMOS technology as MTJs are typically grown on the top of a silicon wafer. Several companies are

working on developing STT-MRAM commercially, with first products already on the market.

The spin-polarized current is only a fraction of the total charge current passing through the cell, high currents are required to switch the magnetization direction of the recording layer. The reduction of the current density required for switching and the increase of the switching speed without compromising the thermal stability preserved are the most important challenges in STT-MRAM developments.

Depending on the orientation of the layer magnetizations, the magnetic elements are divided into perpendicular with out-of-plane magnetization and in-plane with the magnetization lying in the plane of the magnetic layers. The problem of a relatively high switching current density in in-plane structures is rooted in the specificity of the switching dynamics, when the magnetization must turn out of plane, which results in an additional penalty contribution to the switching barrier. In in-plane structures the thermal barrier separating the two stable states is due to the shape anisotropy alone and is therefore lower than the switching barrier. The solution of this problem is to resort to perpendicular MTJs. Indeed, in perpendicular MTJs the switching path is the same as the path for magnetization reversal due to thermal agitations. Therefore, the switching barrier is equal to the thermal barrier. However, the reduction of the Hilbert damping and thus the switching current density [32] and the increase of thermal stability in perpendicular structures [33] are substantial challenges for the known materials and prompt an effortful search for new materials with superior characteristics. In order for STT-MRAM to become a competitive alternative to DRAM, it is mandatory to have MTJs with a large thermal stability barrier E over 80 $k_B T$, a small junction size (less than 20nm in diameter), and a higher than 100% TMR ratio [34]. Many materials for the recording magnetic layer and the ferromagnetic electrodes have been explored. It appears that a composite structure [35] of the recording layer is needed to fulfill the requirements. It is shown [34] that a carefully designed recording layer containing a Co/Pt multilayer with a CoFeB/Ta insertion layer provides MTJs with the desired characteristics.

Another solution to the switching time and current reduction without sacrificing the thermal stability is to use an in-plane structure with a composite free layer as recording layer, which is made of two half-elliptic parts separated by a narrow gap [36]. The switching becomes not only faster but also more uniform, without compromising the thermal stability.

It has been discovered recently that a current passing through a non-magnetic material with high values of the spin Hall angle may flip the magnetization in a nanomagnet fabricated on it [37]. Based on this phenomenon, a three-terminal MTJ has been suggested, where the magnetization of the recording layer is switched by the torque generated by the spin current appearing due to the Rashba effect and/or the spin Hall effect from the current passing in a non-magnetic material. If a VLSI compatible material, Cu doped with 10% Ir, is used as a channel material, the switching happens at a current density less than 10^6 Acm^{-2} [38], comparable to that reported in two-terminal MTJs. Magnetization reversal in an MTJ with perpendicular magnetization due to the spin torques produced by the current in a non-magnetic material has also been recently reported [39].

An electric field alters the properties of a ferromagnet, in particular the magnetization anisotropy, through the modulation of the carrier density. A combination of STT and electric field mediated switching allows to reverse the magnetization faster and more reliably [40]. An electric field also helps to invert the magnetization in a three-terminal MTJ.

Materials with high spin Hall angle or Rashba torques are required for efficient switching in three-terminal MTJs. Due to the spin-momentum locking in the conducting states at the interface resulting in a large spin polarization, when the current is flowing through the states [41], a relatively new class of materials, topological insulators, are promising for spintronic applications. Indeed, a very large spin transfer torque [42] and magnetization switching by giant spin-orbit torque [43] were recently reported in a magnetic heterostructure containing a topological insulator, prompting for a swift appearance of devices with topological insulators on the market.

IV. STT-MRAM-Based Logic-in-Memory

The realization of MTJ-based non-volatile logic gates has been successfully demonstrated, for which the MTJ devices are used simultaneously as non-volatile memory cells and main computing elements [44], [45]. The logic implementation using MTJ-based logic gates relies on a conditional switching behavior provided by state-dependent current modulations on the output (target) MTJs. This modulations are caused by the differences in the MTJs' resistances for different initial logic states. Asymmetry between the source and target MTJs channels is addressed by an innovative solution [46] of using the access transistor as a voltage-controlled resistor. Therefore, implication logic can be intrinsically implemented with commercial MRAM arrays.

V. Conclusion

Because of the recent ground-breaking experimental and theoretical findings silicon is now gaining momentum to be used in electronic applications involving spin. Mechanical stress routinely applied to enhance the electron mobility can also be used to boost the spin lifetime. An efficient coupling between the electrical and the magnetic degrees of freedom makes STT-MRAM a viable candidate for future universal memory. Implication logic gates in STT-MRAM arrays opens the road towards intrinsic logic-in-memory architecture, where the same elements are employed to store and to process information. Regardless of an ultimate progress, many challenges are laying ahead. In particular, finding efficient ways of manipulating spins in silicon by voltages could open new ways towards low-power high performance computational architectures.

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REFERENCES

[1] S. Datta and B. Das, "Electronic analog of the electro-optic modulator," *Appl. Phys. Lett.*, vol. 56, no. 7, pp. 665–667, 1990.

[2] G. A. Prinz, "Magnetoelectronics," *Science*, vol. 282, no. 5394, pp. 1660–1663, 1998.

[3] M. Johnson, *Magnetoelectronics*. Elsevier, 2004.

[4] I. Zutic, J. Fabian, and S. Das Sarma, "Spintronics: Fundamentals and applications," *Rev. Mod. Phys.*, vol. 76, pp. 323–410, Apr 2004.

[5] J. Fabian, A. Matos-Abiaguea, C. Ertler, P. Stano, and I. Zutic, "Semiconductor spintronics," *Acta Phys. Slovaca*, vol. 57, pp. 565–907, 2007.

[6] R. Jansen, "Silicon spintronics," *Nature Materials*, vol. 11, pp. 400–408, 2012.

[7] D. D. Awschalom, L. C. Bassett, A. S. Dzurak, E. L. Hu, and J. R. Petta, "Quantum spintronics: Engineering and manipulating atom-like spins in semiconductors," *Science*, vol. 339, no. 6124, pp. 1174–1179, 2013.

[8] J. L. Cheng, M. W. Wu, and J. Fabian, "Theory of the spin relaxation of conduction electrons in silicon," *Phys. Rev. Lett.*, vol. 104, p. 016601, Jan 2010.

[9] P. Li and H. Dery, "Spin-orbit symmetries of conduction electrons in silicon," *Phys. Rev. Lett.*, vol. 107, p. 107203, Sep 2011.

[10] I. Appelbaum, B. Huang, and D. J. Monsma, "Electronic measurement and control of spin transport in silicon," *Nature*, vol. 447, pp. 295–298, 2007.

[11] B. Huang, D. J. Monsma, and I. Appelbaum, "Coherent spin transport through a 350 micron thick silicon wafer," *Phys. Rev. Lett.*, vol. 99, p. 177209, Oct 2007.

[12] S. Sugahara and J. Nitta, "Spin-transistor electronics: An overview and outlook," *Proc. IEEE*, vol. 98, no. 12, pp. 2124–2154, Dec 2010.

[13] S. P. Dash, S. Sharma, R. S. Patel, M. P. de Jong, and R. Jansen, "Electrical creation of spin polarization in silicon at room temperature," *Nature*, vol. 462, pp. 491–494, 2009.

[14] C. Li, O. van 't Erve, and B. Jonker, "Electrical injection and detection of spin accumulation in silicon at 500K with magnetic metal/silicon dioxide contacts," *Nature Communications*, vol. 2, p. 245, 2011.

[15] M. Tran, H. Jaffres, C. Deranlot, J.-M. George, A. Fert, A. Miard, and A. Lemaitre, "Enhancement of the spin accumulation at the interface between a spin-polarized tunnel junction and a semiconductor," *Phys. Rev. Lett.*, vol. 102, p. 036601, Jan 2009.

[16] Y. Song and H. Dery, "Magnetic-field-modulated resonant tunneling in ferromagnetic-insulator-nonmagnetic junctions," *Phys. Rev. Lett.*, vol. 113, p. 047205, Jul 2014.

[17] R. Jansen, A. M. Deac, H. Saito, and S. Yuasa, "Injection and detection of spin in a semiconductor by tunneling via interface states," *Phys. Rev. B*, vol. 85, p. 134420, Apr 2012.

[18] A. Spiesser, H. Saito, R. Jansen, S. Yuasa, and K. Ando, "Large spin accumulation voltages in epitaxial Mn_5Ge_3 contacts on Ge without an oxide tunnel barrier," *Phys. Rev. B*, vol. 90, p. 205213, Nov 2014.

[19] K.-R. Jeon, H. Saito, S. Yuasa, and R. Jansen, "Energy dispersion of tunnel spin polarization extracted from thermal and electrical spin currents," *Phys. Rev. B*, vol. 91, p. 155305, Apr 2015.

[20] T. Suzuki, T. Sasaki, T. Oikawa, M. Shiraishi, Y. Suzuki, and K. Noguchi, "Room-temperature electron spin transport in a highly doped Si channel," *Appl. Phys. Express*, vol. 4, p. 023003, 2011.

[21] T. Sasaki, Y. Ando, M. Kameno, T. Tahara, H. Koike, T. Oikawa, T. Suzuki, and M. Shiraishi, "Spin transport in nondegenerate Si with a spin MOSFET structure at room temperature," *Phys. Rev. Applied*, vol. 2, p. 034005, Sep 2014.

[22] Y. Song, O. Chalaev, and H. Dery, "Donor-driven spin relaxation in multivalley semiconductors," *Phys. Rev. Lett.*, vol. 113, p. 167201, Oct 2014.

[23] Y. Song and H. Dery, "Analysis of phonon-induced spin relaxation processes in silicon," *Phys. Rev. B*, vol. 86, p. 085201, Aug 2012.

[24] J. Li and I. Appelbaum, "Modeling spin transport in electrostatically-gated lateral-channel silicon devices: Role of interfacial spin relaxation," *Phys. Rev. B*, vol. 84, p. 165318, Oct 2011.

[25] D. Osintsev, V. Sverdlov, Z. Stanojeviĉ, A. Makarov, and S. Selberherr, "Temperature dependence of the transport properties of spin field-effect transistors built with InAs and Si channels," *Solid-State Electron.*, vol. 71, pp. 25 – 29, 2012.

[26] S.-C. Chang, S. Manipatruni, D. Nikonov, I. Young, and A. Naeemi, "Design and analysis of Si interconnects for all-spin logic," *Magnetics, IEEE Transactions on*, vol. 50, no. 9, pp. 1–13, Sept 2014.

[27] H. Dery, P. Dalal, L. Cywinki, and L. Sham, "Spin-based logic in semiconductors for reconfigurable large-scale circuits," *Nature*, vol. 447, pp. 573–576, 2007.

[28] B. Behin-Aein, D. Datta, S. Salahuddin, and S. Datta, "Proposal for an all-spin logic device with built-in memory," *Nature Nanitechnology*, vol. 5, pp. 266–270, 2010.

[29] T. Marukame, T. Inokuchi, M. Ishikawa, H. Sugiyama, and Y. Saito, "Read/write operation of spin-based MOSFET using highly spin-polarized ferromagnet/MgO tunnel barrier for reconfigurable logic devices," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, Dec 2009, pp. 1–4.

[30] J. Slonczewski, "Current-driven excitation of magnetic multilayers," *Journal of Magnetism and Magn. Materials*, vol. 159, no. 1-2, pp. L1–L7, 1996.

[31] L. Berger, "Emission of spin waves by a magnetic multilayer traversed by a current," *Phys. Rev. B*, vol. 54, pp. 9353–9358, Oct 1996.

[32] S. Ikeda, K. Miura, H. Yamamoto, K. Mizunuma, H. D. Gan, M. Endo, S. Kanai, J. Hayakawa, F. Matsukura, and H. Ohno, "A perpendicular-anisotropy CoFeB-MgO magnetic tunnel junction," *Nature Materials*, vol. 9, no. 9, pp. 721–724, 2010.

[33] D.-S. Wang, S.-Y. Lai, T.-Y. Lin, C.-W. Chien, D. Ellsworth, L.-W. Wang, J.-W. Liao, L. Lu, Y.-H. Wang, M. Wu, and C.-H. Lai, "High thermal stability and low Gilbert damping constant of CoFeB/MgO bilayer with perpendicular magnetic anisotropy by Al capping and rapid thermal annealing," *Appl. Phys. Lett.*, vol. 104, no. 14, p. 142402, 2014.

[34] S. Ishikawa, H. Sato, M. Yamanouchi, S. Ikeda, S. Fukami, F. Matsukura, and H. Ohno, "Co/Pt multilayer-based magnetic tunnel junctions with a CoFeB/Ta insertion layer," *Journal of Applied Physics*, vol. 115, no. 17, p. 17C719, 2014.

[35] H. Sato, E. C. I. Enobio, M. Yamanouchi, S. Ikeda, S. Fukami, S. Kanai, F. Matsukura, and H. Ohno, "Properties of magnetic tunnel junctions with a MgO/CoFeB/Ta/CoFeB/MgO recording structure down to junction diameter of 11nm," *Applied Physics Letters*, vol. 105, no. 6, p. 062403, 2014.

[36] A. Makarov, V. Sverdlov, D. Osintsev, and S. Selberherr, "Reduction of switching time in pentalayer magnetic tunnel junctions with a composite-free layer," *Phys. Status Solidi- Rapid Research Letters*, vol. 5, no. 12, pp. 420–422, 2011.

[37] L. Liu, C.-F. Pai, Y. Li, H. W. Tseng, D. C. Ralph, and R. A. Buhrman, "Spin-torque switching with the giant spin Hall effect of tantalum," *Science*, vol. 336, no. 6081, pp. 555–558, 2012.

[38] M. Yamanouchi, L. Chen, J. Kim, M. Hayashi, H. Sato, S. Fukami, S. Ikeda, F. Matsukura, and H. Ohno, "Three terminal magnetic tunnel junction utilizing the spin Hall effect of iridium-doped copper," *Applied Physics Letters*, vol. 102, no. 21, p. 212408, 2013.

[39] C. Zhang, M. Yamanouchi, H. Sato, S. Fukami, S. Ikeda, F. Matsukura, and H. Ohno, "Magnetization reversal induced by in-plane current in Ta/CoFeB/MgO structures with perpendicular magnetic easy axis," *Journal of Applied Physics*, vol. 115, no. 17, p. 17C714, 2014.

[40] S. Kanai, Y. Nakatani, M. Yamanouchi, S. Ikeda, H. Sato, F. Matsukura, and H. Ohno, "Magnetization switching in a CoFeB/MgO magnetic tunnel junction by combining spin-transfer torque and electric field-effect," *Applied Physics Letters*, vol. 104, no. 21, p. 212406, 2014.

[41] C. Li, O. van 't Erve, J. T. Robinson, Y. Liu, L. Li, and B. Jonker, "Electrical detection of charge-current-induced spin polarization due to spin-momentum locking in Bi_2Se_3," *Nature Nanotechnology*, vol. 9, p. 218, 2014.

[42] A. R. Mellnik, J. S. Lee, A. Richardella, J. L. Grab, P. J. Mintun, M. H. Fischer, A. Vaezi, A. Manchon, E.-A. Kim, N. Samarth, and D. C. Ralph, "Spin-transfer torque generated by a topological insulator," *Nature*, vol. 511, pp. 449–451, 2014.

[43] Y. Fan, P. Upadhyaya, X. Kou, M. Lang, S. Takei, Z. Wang, J. Tang, L. He, L.-T. Chang, M. Montazeri, G. Yu, W. Jiang, T. Nie, R. N. Schwartz, Y. Tserkovnyak, and K. L. Wang, "Magnetization switching through giant spin-orbit torque in a magnetically doped topological insulator heterostructure," *Nature Materials*, vol. 13, pp. 699–704, 2014.

[44] A. Lyle, S. Patil, J. Harms, B. Glass, X. Yao, D. Lilja, and J. ping Wang, "Magnetic tunnel junction logic architecture for realization of simultaneous computation and communication," *IEEE Trans. Magn.*, vol. 47, no. 10, pp. 2970–2973, Oct 2011.

[45] H. Mahmoudi, T. Windbacher, V. Sverdlov, and S. Selberherr, "Implication logic gates using spin-transfer-torque-operated magnetic tunnel junctions for intrinsic logic-in-memory," *Solid-State Electron.*, vol. 84, pp. 191–197, 2013.

[46] ——, "MRAM-based logic array for large-scale non-volatile logic-in-memory applications," in *International symposium on Nanoscale Architectures (NANOARCH)*, July 2013, pp. 26–27.