Hierarchical TCAD Device Simulation of FinFETs

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***Abstract*—A framework for FinFET design studies is presented. Our physics-based modeling approach allows to accurately capture the effects of channel cross-section, orientation and strain as well as contact resistance – for the first time all in one tool. Using this approach as a reference, the predictiveness of empirical TCAD models is extended by re-calibration. Our hierarchical tool chain is embedded in an industry-proven framework equipped with DOE and optimization modules. The capabilities are demonstrated in a simulation study on a recent FinFET technology node.**

I. Introduction

The introduction of non-planar devices brings new degrees of freedom to transistor designs. Quantum confinement can be utilized as performance booster as can mechanical stress in the channel. However, evaluating how design decisions affect device performance is far less straightforward than it used to be for planar technology. In planar technology the inversion condition in a semiconductor channel could be characterized by a single figure, the effective field E_{eff} [1]. In a nano-scale non-planar channel this is not possible.

In our previous work we have demonstrated one way of dealing with the added complexity in modeling and simulation of non-planar channels in a physically grounded way [2]. The approach involved solving the linearized Boltzmann transport equation on top of the channel subband structure to extract mobility and channel conductance.

In the first part of this work, we will expand on this approach and demonstrate how it can be coupled to a device simulator. This, however comes with increased computational cost with respect to empirical device modeling. In the second part we will show how an automated calibration framework can be used to provide empirical device model parameters for non-planar channels based on physical modeling. The re-calibration re-establishes the validity of the empirical models for a particular non-planar channel allowing to obtain simulation results quickly but still with the required predictiveness.

II. Physical Device Modeling

In our extended physical device modeling approach, we couple the classical device simulator Minimos-NT [3] with the electronic structure and transport solver VSP [4]. The coupling is done by decomposing the simulation domain along the channel direction into two-dimensional slices, as illustrated in Fig. 1 and Fig. 2. At each iteration step, Minimos-NT invokes an instance of VSP on each slice to calculate the confined carrier densities, from which a correction potential is extracted, as well as channel mobilities - see Fig. 3. Minimos NT passes electrostatic potential and quasi-Fermi energies

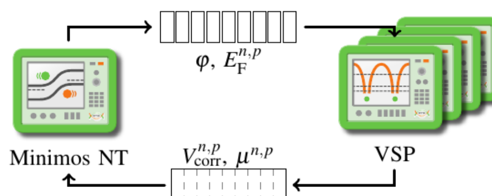

Figure 1. Schematic overview of the coupling between the classical device simulator Minimos-NT and the quantum mechanical simulator VSP. Minimos-NT invokes a VSP instance on each of the slices. The VSP results are combined and fed beck to Minimos-NT.

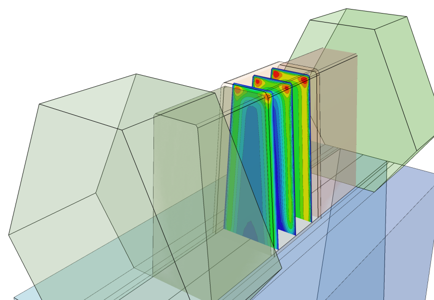

Figure 2. Self-consistent carrier concentration on slices in the channel of the device. Charge concentrates at the corners, which demands a full two-dimensional solution of the Schroedinger equation.

for electrons and holes, from which VSP can determine the subband structure and its occupancy. The data on each slice is then extruded and interpolated back onto the three-dimensional simulation domain before starting the next iteration step. This self-consistent quantum correction approach ensures a stable and fast convergence of the three-dimensional problem. It can be observed that, upon convergence, carrier densities from

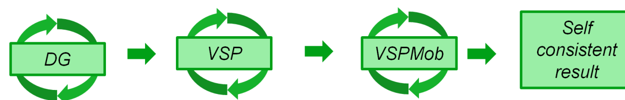

Figure 3. The iteration scheme for device simulation with self-consistent quantum correction and mobility evaluation comprises three blocks: block I - empirical models for density and mobility are run; block II - self-consistent quantum correction provided by VSP is used with empirical mobility models; block III - self-consistent quantum correction and mobility provided by VSP are used. Each block is iterated until convergence is achieved.

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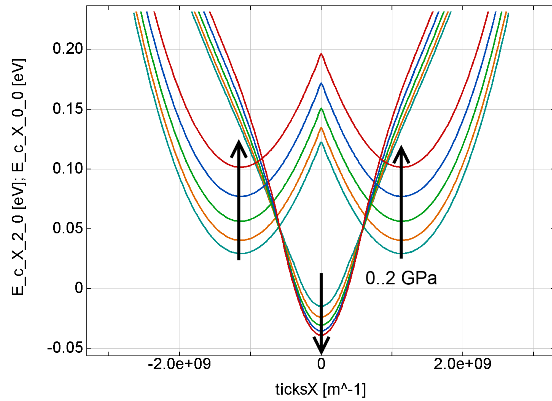

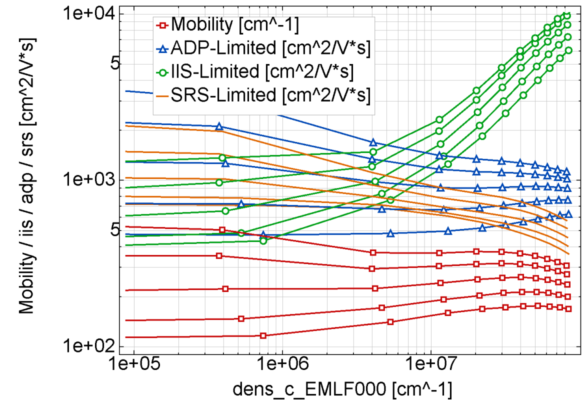

Figure 4. **Left:** subband structure of the nMOS FinFET. The effect of tensile stress along ⟨110⟩ channel direction is shown: One valley type move up in energy where as the opposite one moves down which yields a valley re-population. Also, the dispersion relation is changed which results in an decreasing transport carrier mass for the given stress conditions directly affect the carrier mobility. **Right:** the effect of the stress conditions on the channel mobility; the contributions of all the different scattering processes are shown as function of inversion density.

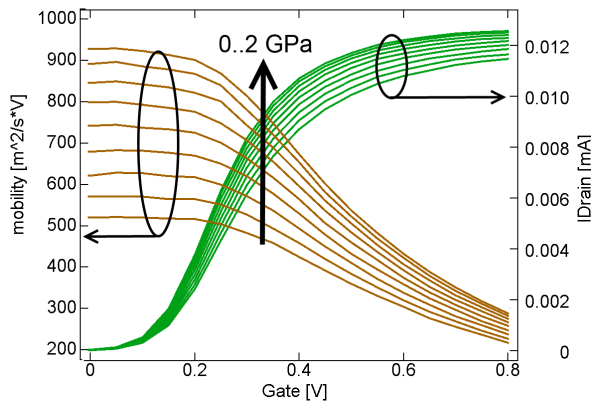

Figure 5. Effect of uni-axial stress along ⟨100⟩ channel direction on the channel mobility (left) and linear transfer characteristic (right).

Minimos-NT and VSP become identical. The approach enables one to investigate the effect of channel cross-section, orientation and strain without the need to adjust model parameters as explained in Fig. 4 and Fig. 5. The framework was used to study the effect of channel width, doping, and length as shown in Figs. 6 to 10.

III. Empirical Device Modeling

The empirical device model is based on the density-gradient/drift-diffusion equations with unified Philips and enhanced Lombardi mobility models [5], [6], and a piezo-resistivity model for stress-induced mobility enhancement. The GTS Framework module for automated scripting and optimization (c.f. Fig. 11 and Fig. 12) was used to fit the empirical model parameters to the physical simulations in three steps: In the first step, the γ-parameter of the density-gradient model and α and β-parameters of the Cauchy boundary condition were calibrated by fitting the C/V curve to a self-consistent Schrödinger-Poisson result obtained from VSP. Figure 13 shows excellent agreement of the C/V-curves over a wide range of fin widths and channel dopings. In the second step, the mobility models are calibrated individually for each of the scattering processes such as impurity, lattice, or surface roughness scattering (c.f. Fig. 14). In the third step, the actual mobility is calibrated for the target window. A reasonable agreement over a range of gate voltages, fin widths and dopings can be achieved as demonstrated in Fig. 15.

IV. Conclusion

A hierarchical device simulation tool-chain, which includes physical transport modeling, is necessary to make sensible predictions for non-planar devices (Fig. 7). Such a tool-chain was presented where physical models for density and mobility are embedded directly into the classical device simulation, while leaving the option of automated fitting of empirical models for particular device designs. The seamless integration of both approaches in one framework significantly extends the predictive window of device simulation in TCAD.

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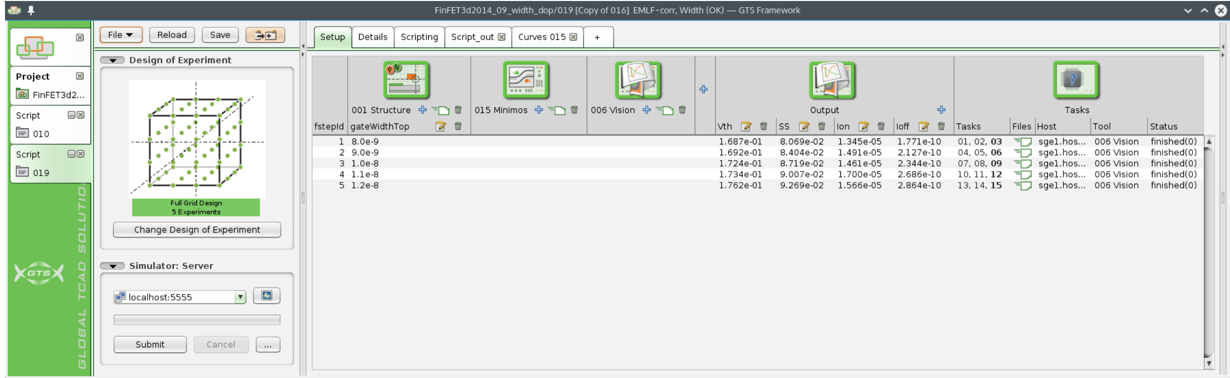

Figure 6. Design of experiment (DOE) setup for the simulations presented: I) Template-based structure generation, II) Device simulation with physical models, III) Device parameter extraction using post-processing module. Results are shown on-the-fly in the output column during the simulation run. DOE simulation tasks are automatically distributed on a compute cluster using an SGE interface of our job server.

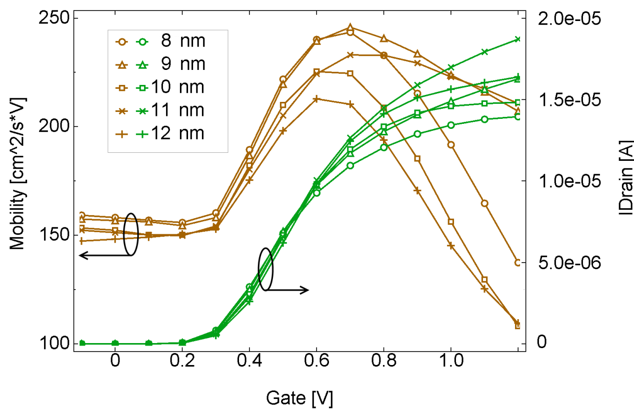

Figure 7. The effect of the fin width on low-field mobility and linear drain current is shown. It is remarkable that no simple relation between channel width and current is found, as would be expected when only considering the inversion charge.

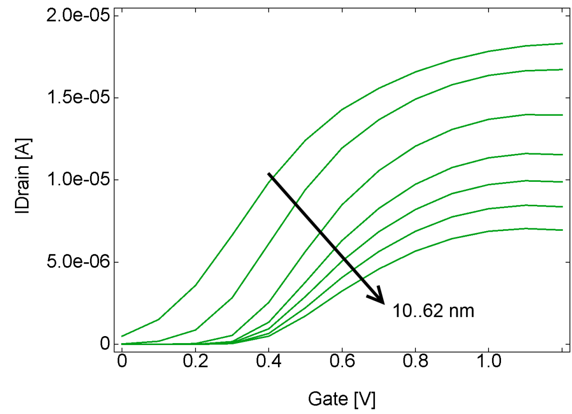

Figure 9. The effect of channel length scaling on the linear transfer characteristic is shown.

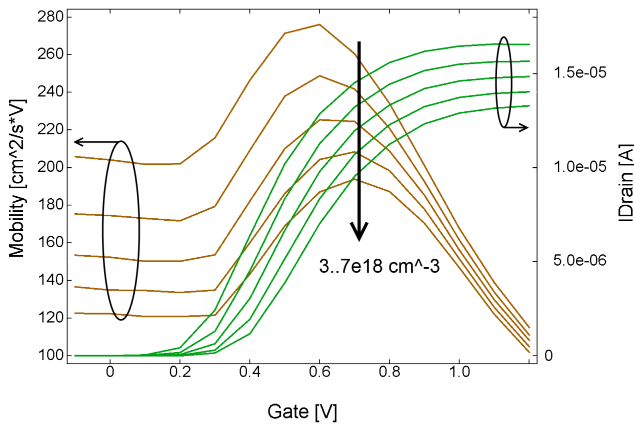

Figure 8. Channel doping on one hand shifts the threshold voltage, but on the other hand considerably reduces the channel mobility by ionized impurity scattering.

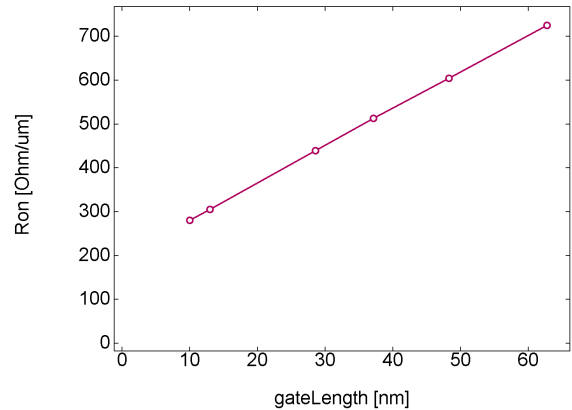

Figure 10. Based on the on-current according to the figure above, the on-resistance is plotted as a function of the channel length. It allows to extract the contact resistance of the transistor.

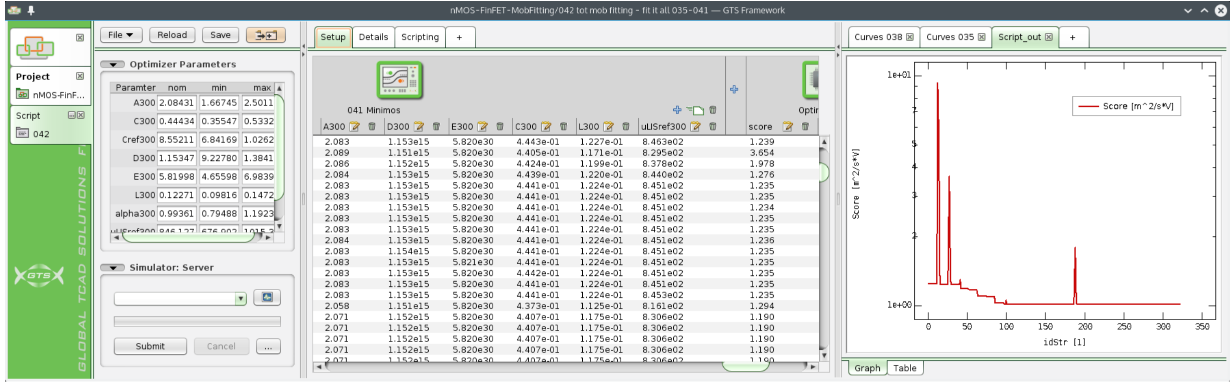

Figure 11. Empirical device simulation models calibrated using a built-in optimization framework; the empirical model parameters to be fitted are shown in the table. The deviation between empirical and physical results is used as score function, which is minimized in the optimization runs as shown in the diagram at the right hand side.

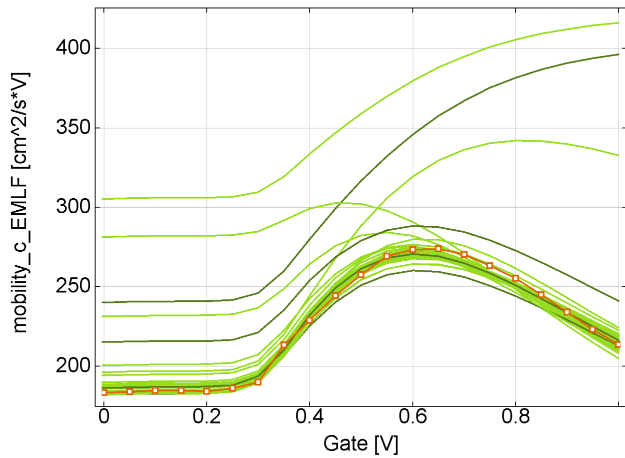

Figure 12. A simultaneous optimization of all partial mobilities is applied. Here, the overall mobility during the optimization run is shown.

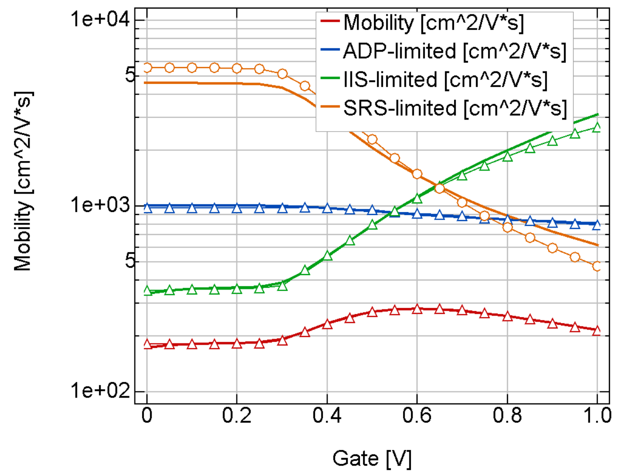

Figure 14. Fitting the components of the empirical mobility model (lines) to the physical model (symbols). Overall mobility is plotted red.

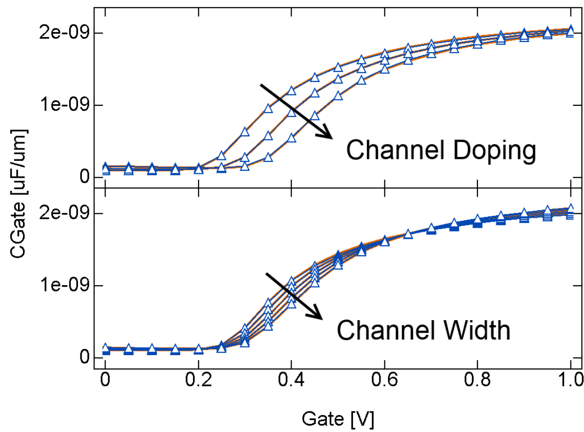

Figure 13. Models calibrated by CV-simulations with Minimos-NT (lines) and VSP (symbols). Variation of channel doping (3×10^{18} cm^{-3} to 7×10^{18} cm^{-3}) and channel width (8 nm to 12 nm).

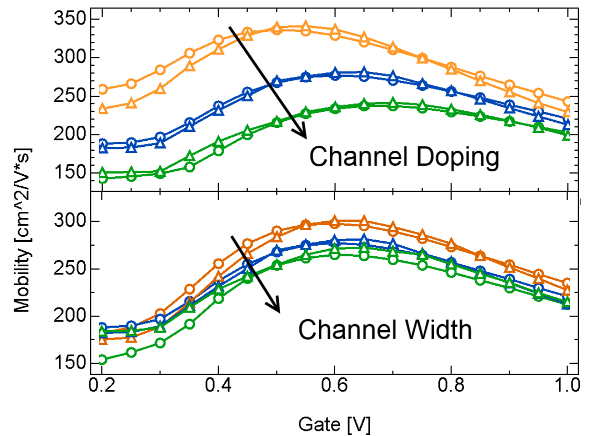

Figure 15. Calibrated mobility model; Minimos-NT (lines) and VSP (symbols). Variation of channel doping (3×10^{18} cm^{-3} to 7×10^{18} cm^{-3}) and fin width (8 nm to 12 nm).