Impact of Across-Wafer Variation on the Electrical Performance of TSVs

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***Abstract*—A simulation methodology is presented by which measured equipment variation during silicon DRIE is quantified and the effective variation in the electrical performance of the final TSV devices is found. Using the level set method, process simulations are performed in order to generate structures representative of the equipment variation. The across-wafer variation of the resulting scallop geometry is about 20%, while the electrical performance, including the resistance, capacitance, and inductance of the devices was found to not vary beyond 1%.**

***Keywords*—TSV; DRIE variation; process simulation; TCAD**

I. Introduction

Recently, the semiconductor industry has directed considerable effort towards introducing more functionality to applications beyond memory and logic through vertical – or three-dimensional (3D) – integration [1]. This involves the fabrication of electrical interconnections through the entire thickness of the wafer [2]. At the core of vertical integration is a through-silicon via (TSV) which electrically connects the front and back sides of the wafer. Several studies deal with the reliability and performance of filled TSVs [3] as well as open metal-lined TSVs [4]. Open TSVs are desired when the stress build-up due to material thermal expansion is a concern. The presence of a void in the middle of the TSV allows for material expansion, avoiding the reliability concerns related to copper pumping which is common to filled TSVs [3]. However, an open TSV requires more wafer area and quite complex processing techniques.

The processing steps to manufacture an open TSV include deep reactive ion etching (DRIE) followed by the deposition of an isolation oxide, a barrier material, a metal film – tungsten, in this study – and a passivation layer. The process is complex and some deviations in the process conditions are expected [5]. Recently, the effects of the process equipment variation on the performance of an open tungsten-lined TSV was presented by Roger et al. [5]. In addition, the across-wafer variations in oxide plasma enhanced chemical vapor deposition (PECVD) effects on the electrical and reliability parameters of TSVs was quantitatively described by Baer et al. [6].

In this study, the impact of the across-wafer variation during silicon DRIE on the electrical parameters of TSVs is presented. The maximum, minimum, and median values across the wafer are examined using a combination of measurements of the fabrication equipment in addition to reactor and feature scale simulation tools.

II. TSV Fabrication Steps

Prior to fabricating the TSVs, the CMOS processing sequence is applied to generate the devices. Subsequently, the wafer is thinned down to a required thickness and bonded. Three main steps describe TSV fabrication: (1) the opening of the intermetal dielectrics; (2) the etching of the CMOS wafer using a DRIE process with an etch-stop metal layer at the bond side; and (3) oxide isolation, metalization, and further passivation deposition steps [4]. The effects of the plasma equipment variation during the DRIE step are addressed in further detail.

A. Deep Reactive Ion Etching

After opening the inter-metal dielectrics on the top side of the wafer and depositing an etch-stop layer (metal or oxide) at the bottom side, the etching proceeds using the so-called Bosch or DRIE process [7]. This process consists of a sequence of polymer deposition and etching steps. The polymer is applied using a plasma deposition in a C_4F_8 environment. A subsequent etching step in an ion-enhanced SF_6 (or SF_6/O_2) plasma environment ensures that the bottom of the deposited polymer is etched away, while the sidewall is protected. The etching step is a simultaneous physical and chemical process.

After the physical ion etching process has removed the polymer at the trench bottom, the chemical etching process is free to proceed with a further removal of the silicon at the exposed trench bottom, while the sides remain protected with the previously-deposited polymer. After hundreds of deposition/etch cycles are applied, a trench remains with a sidewall roughness in the form of scallops which result from the cycled nature of the process. The sizes of the scallops depend on the deposition and etch rates used during the DRIE process. In this work, the DRIE process proceeds using initial 2-step cycles (C_4F_8, SF_6) followed by the primary 3-step cycles (C_4F_8, SF_6/O_2, SF_6).

B. Chemical Vapor Deposition of Oxide

After the etch process is complete, an oxide layer must be deposited to isolate the silicon substrate from the TSV metal which will connect the top and bottom of the wafer. This layer must not be deposited using high-temperature CVD techniques, because the TSV processing is performed at the end of the full CMOS process flow. Therefore the maximum allowed temperature is in the order of 400°C, which is achieved using three deposition steps: (1) PECVD is used to initiate oxide

deposition; (2) sub-atmospheric chemical vapor deposition (SACVD) is used as a second spacer oxide deposition step; and (3) PECVD is used once again in order to get the optimal spacer layer thickness along the full TSV sidewall. The effect of these deposition steps on the performance of the TSV is given in more details in [6]. After the deposition of the isolation oxide a liner and tungsten are deposited using CVD techniques.

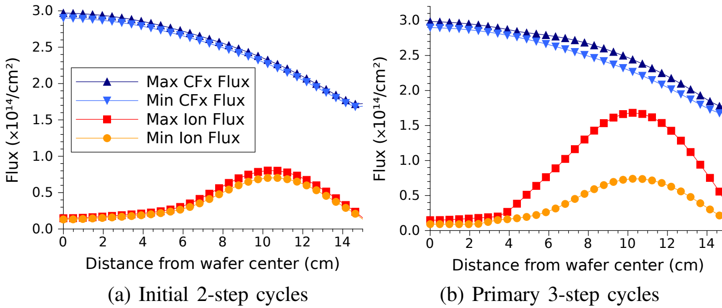
III. Simulation Methodology

Our analysis aims to correlate the variability sources on the equipment level to the electrical parameters of the final devices. Hence, the simulation flow must properly account for the concentration of gases in the chamber, the wafer etching, and the electrical parameter extraction. It is not feasible to treat those three steps together in a unique physics-based model, but a more suitable approach is to resolve them separately, linking them in a forward chain, as described in detail in [5].

A. Equipment Variability Sources

Despite a rigorous control of the injected species in the plasma chamber, some variation can be observed in the concentrations of relevant gases and the duration of their presence in the chamber. Because the process used involves two types of DRIE etching – 2-step and 3-step cycles described earlier – there are several potential variation sources which have to be considered. During the polymer deposition C_4F_8 is injected into the chamber and some variation in the gas flow rate, and thus in the deposition-relevant CF_x and ion fluxes, is noted. For the 2-step cycles, the etch step is performed by the injection of SF_6 into the chamber; variation in the SF_6 concentration results in a variation of the flux of the relevant F and ion etching species. For the 3-step DRIE processes, after the initial C_4F_8 polymer deposition, a SF_6/O_2 etch step is performed. This introduces an additional O flux which varies along with the gas concentration variation and plays a significant role in the silicon etching process [8].

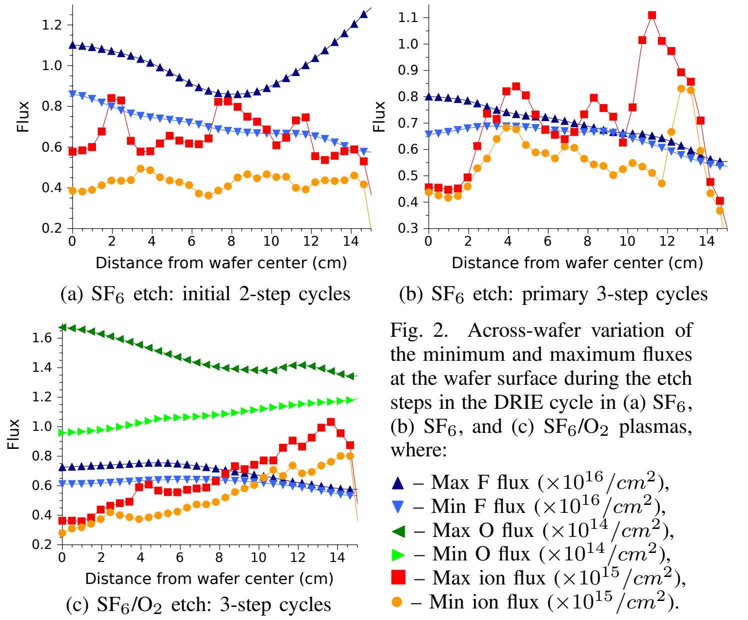
1) DRIE - C_4F_8 Polymer Deposition: the across-wafer variation of the minimum and maximum CF_x and ion fluxes during the C_4F_8 deposition step is given in Fig. 1. The CF_x flux is composed of the dominant neutral deposition species, where CF_x=CF+CF_1+CF_2.



(a) Initial 2-step cycles (b) Primary 3-step cycles

Fig. 1. Across-wafer variation of the minimum and maximum CF_x and ion fluxes during the polymer deposition steps in the DRIE sequence.

2) DRIE - SF_6 and SF_6/O_2 Etching: the across-wafer variation of the minimum and maximum F, O, and ion fluxes during the SF_6 and SF_6/O_2 etching steps is given in Fig. 2. The fluoride (F) flux is the dominant neutral etch species. The fluxes shown in Fig. 1 and Fig. 2 are obtained with Quantemol VT [9] simulations, a software based on the Hybrid Plasma Equipment Model.



(a) SF_6 etch: initial 2-step cycles (b) SF_6 etch: primary 3-step cycles

(c) SF_6/O_2 etch: 3-step cycles

Fig. 2. Across-wafer variation of the minimum and maximum fluxes at the wafer surface during the etch steps in the DRIE cycle in (a) SF_6, (b) SF_6, and (c) SF_6/O_2 plasmas, where:

▲ – Max F flux ($\times 10^{16}/cm^2$),
▼ – Min F flux ($\times 10^{16}/cm^2$),
◀ – Max O flux ($\times 10^{14}/cm^2$),
▶ – Min O flux ($\times 10^{14}/cm^2$),
■ – Max ion flux ($\times 10^{15}/cm^2$),
● – Min ion flux ($\times 10^{15}/cm^2$).

B. Etch Rate Extraction

Using the relevant deposition and etching fluxes given in Fig. 1 and Fig. 2 TSV geometries are generated, representative of several locations along the wafer surface. The simulations are performed using an in-house tool based on the level set and ray tracing techniques [10] in combination with several models for polymer deposition and silicon etching [8], [11]. Performing the necessary number of simulations using the physical flux-driven models is not feasible due to computational limitations, therefore the isotropic/vertical rates which correspond to the neutral/ion fluxes, respectively, are calculated. Fig. 3a and Fig. 3b show the relationship between the relevant fluxes and the resulting deposition and etch rates.

For the C_4F_8 deposition steps the relationship between the wafer surface flux of CF_x and the ionic species to the isotropic and vertical deposition rates is calculated. A similar analysis was performed for the etching step in SF_6 and SF_6/O_2 plasmas. This fast geometry generation approach was used instead of a full physical simulation in order to generate multiple TSV geometries, which represent the across-wafer variation, but also the minimum, maximum, and median fluxes at each location on the wafer. Using the relationships between the deposition/etch rates and the respective fluxes, several TSV structures are generated, similar to the one shown in Fig. 3c, which represents a TSV fabricated in the middle of the wafer with median neutral and ion fluxes.

IV. Electrical Simulation Results

In order to find the across-wafer variation of the TSV geometry and electrical performance, TSVs were generated using the maximum, minimum, and median neutral and ion fluxes along 21 locations between the middle and the edge of the wafer. This resulted in a total of 63 structures, 3 for

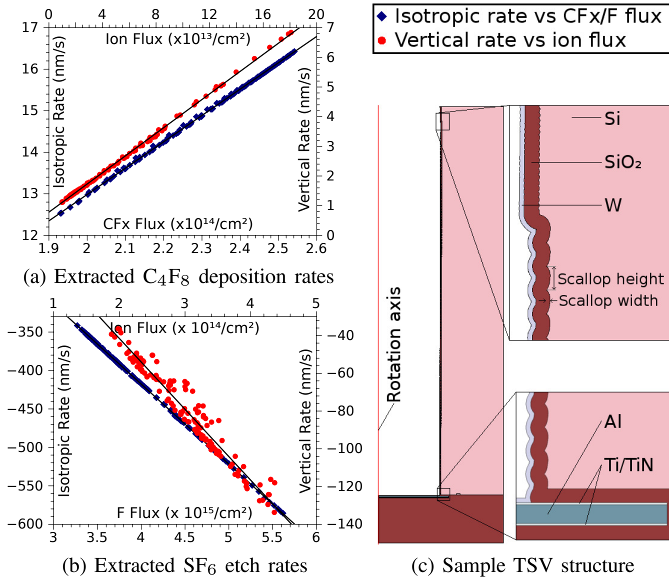


Fig. 3. Extracted isotropic and vertical rates' dependence on the neutral and ion fluxes at the wafer surface for the (a) polymer deposition and (b) etching steps and (c) a sample TSV geometry, prepared for electrical simulations. The fluxes shown are normalized from measurements to standard expected values.

each test location on the wafer. The dimensions of the large scallops along the TSV sidewall are given in Fig. 4, where the data is normalized to the average value. The variation of the scallop width appears to be highest in the middle of the wafer, where the maximum and minimum vary by 10% from the average. The scallop height varies by almost 20% from the average, spiking between the wafer middle and its edge.

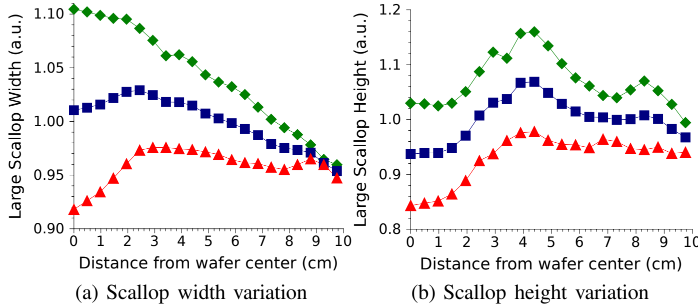


Fig. 4. Across-wafer variation in the scallop (a) width and (b) height using maximum (♦), minimum (▲), and median (■) fluxes from Fig. 1 and Fig. 2.

The structures are used as input for the COMSOL Multiphysics software [12] where they are meshed and the necessary device simulations are performed in order to obtain the resistance, capacitance, and inductance for all structures. The resulting across-wafer variation for the electrical parameters is shown in Fig. 5. Although the scallops show variation up to 20%, this does not appear to translate to the electrical performance, where all values stay within 1% of the average.

V. Conclusion

Process equipment-induced variations have an impact on the electrical operation of fabricated interconnect structures. In addition, the non-homogeneity of the etchant fluxes along the wafer surface introduces across-wafer variations in the fabrication process and in-turn in the device performance. An analysis of this phenomenon was performed for a DRIE process for an open tungsten-lined TSV technology using measured equipment variation as well as reactor-scale and feature-scale simulations. It was found that although geometrical variations of up to 20% are observed between the middle and edge of the wafer, the electrical performance does not vary by more than 1%.

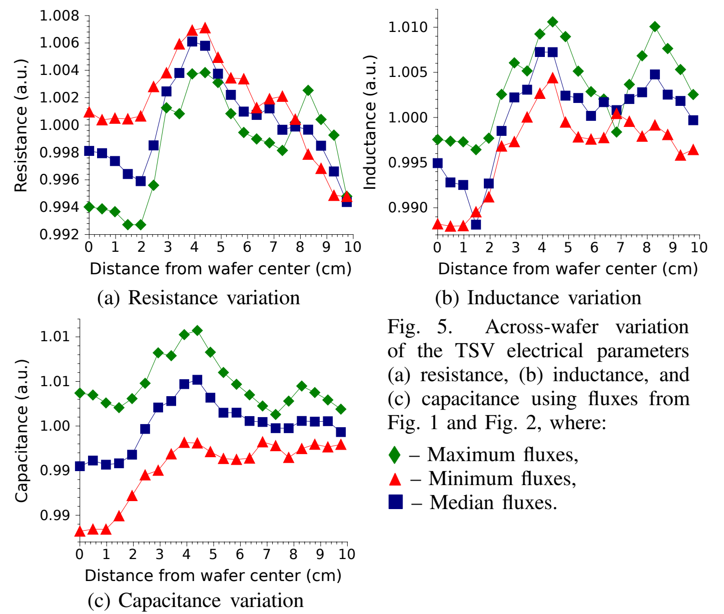


Fig. 5. Across-wafer variation of the TSV electrical parameters (a) resistance, (b) inductance, and (c) capacitance using fluxes from Fig. 1 and Fig. 2, where:
- ♦ – Maximum fluxes,
- ▲ – Minimum fluxes,
- ■ – Median fluxes.

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