Charge Feedback Mechanisms at Forward Threshold Voltage Stress in GaN/AlGaN HEMTs

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***Abstract*—Charge trapping in the insulating layer of gallium-nitride (GaN) metal-insulator-semiconductor high-electron-mobility transistors (MIS-HEMTs) is a serious reliability challenge but is still poorly understood. We demonstrate here that the observed V_{th} drift and recovery can be understood as charge capture and emission following a non-radiative multi-phonon (NMP) mechanism into traps with widely distributed properties. Furthermore, due to the large amount of trapped charge, the feedback of that charge on the surface potential and thus on the capture and emission times has to be considered self-consistently in order to correctly explain the temporal changes in their distributions.**

I. Introduction

Compared to other technologies, GaN MIS-HEMTs offer superior electronic properties in terms of breakdown voltage, on-state resistance and switching behaviour [1]. One major reliability issue in both normally-on and normally-off MIS-HEMTs, is the threshold voltage (V_{th}) drift at forward gate bias stress [2]–[5]. Studies of the degradation behaviour have revealed broad distributions of capture and emission times as well as second-order effects attributed to the interaction of trapped charges with the channel through the barrier and a coulomb feedback effect on the surface potential [3], [6].

We show here that our non-radiative multi-phonon (NMP) charge trapping model previously developed for silicon technologies [7] is able to explain the observed degradation and recovery behaviour for different gate stress biases. Furthermore, we prove the strong impact of the coulomb feedback on the V_{th} drift kinetics.

II. Experimental

Our devices consist of a 10 nm thick AlGaN barrier (18% Al) on top of a 1 µm thick GaN buffer and a gate length of 1 µm. A silicon-nitride layer is used as gate dielectric and for the access regions, see Fig. 1 for a simplified schematic. V_{th} recovery traces after increasing stress times were recorded using an ultra-fast measurement setup [3] for various stress voltages at 25 °C.

III. Simulation setup

For the simulations we use our device simulator Minimos-NT [8] on a slightly simplified device geometry,

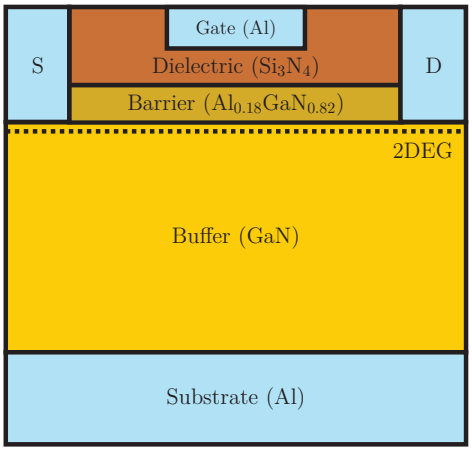

Fig. 1. Simplified device geometry of our devices. A 10 nm thick AlGaN barrier is placed on top of a 1 µm thick GaN layer. The thickness of the gate dielectric is 25 nm and the gate length is 1 µm. For the simulations, the access regions as well as the source and drain lengths are scaled to 500 nm. The contact material is aluminum.

where the source/drain-gate spacers and contact length are set to 500 nm and the substrate is replaced by a metal layer to reduce the computational effort.

The net piezoelectric charge at the barrier-buffer interface was chosen according to [9]. For the barrier-dielectric interface, the net amount of piezoelectric charge was estimated by comparing the threshold voltages of devices with different dielectric thicknesses (see Fig. 2). In thermal equilibrium, the net positive charge at the barrier-dielectric interface defines the threshold voltage of the device. Assuming ideal capacitors, the voltage divider between barrier and gate dielectric at different geometries can be used to calculate the net charge from the threshold voltages.

Deep donor traps with an energy level of 2.8 eV above the GaN valence band were placed into the buffer and barrier layer with concentrations of $1 \times 10^{16}\,\mathrm{cm}^{-3}$ and $5 \times 10^{16}\,\mathrm{cm}^{-3}$, respectively. A thermionic field emission model is used to describe the transfer of electrons and holes from the GaN channel to the dielectric interface. The workfunction difference for the aluminum gate is set to $E_w = -1.95$ V according to [10].

Recent studies have demonstrated that the traps responsible for the threshold voltage drift are located near the dielectric interface [11]. Therefore, the NMP traps

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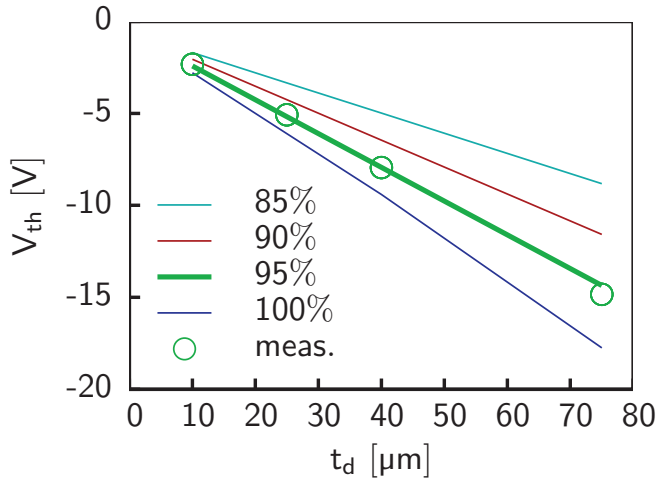

Fig. 2. The positive counter-charges at the dielectric interface and thus the electrostatic surface potential were estimated by comparing V_{th} at different dielectric thicknesses. V_{th} is shown for different fractions of positive and piezoelectric charges at the dielectric interface. As can be seen, best agreement is obtained when 95 % of the piezoelectric charges are compensated.

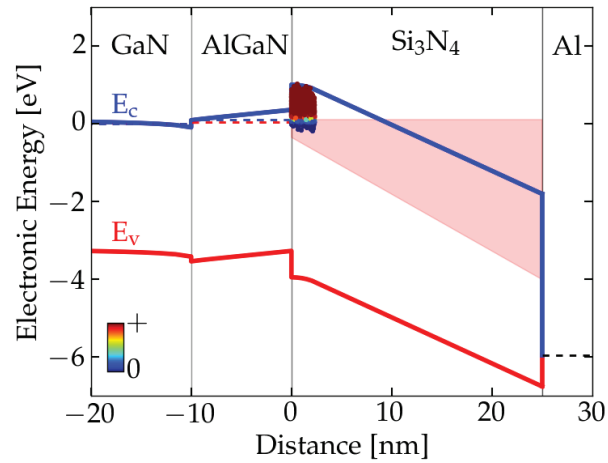

Fig. 3. The band energy profile along a cut through the gate shows the influence of the applied piezoelectric charges as well as the location of the applied NMP traps at $V_g = 4\,V$ in thermal equilibrium. The active energy region, defined as the region, where the NMP traps can capture an electron, is marked as red area. The charge state of each NMP trap is depicted by its color.

were placed uniformly distributed within 2 nm from the dielectric interface. The concentration of NMP traps was determined based on the interface concentration obtained from Fig. 2.

IV. Results and Discussion

The resulting band energy diagram for 0 V together with the trap distribution is depicted in Fig. 3. The red area is spanned by connecting the Fermi levels at the barrier-dielectric interface and the gate at two different gate voltages. This so called active energy region marks the energy band within the insulator where traps can capture electrons under a fixed bias condition. The red and blue dots at the dielectric interface mark the position of the NMP traps within the band gap, their equilibrium charge is given by their color. The change in the surface potential due to coulomb feedback can also be seen in the active energy area, which then becomes a polygon instead of a triangle.

For a correct description, it is mandatory that the transient simulation setup closely follows the experimental procedure [3], [5], which consists of a series of stress pulses with different stress times and voltages applied to a single device and monitors the recovery between the pulses (MSM setup [7], Fig. 4). In order to focus on the traps in the insulating layer and to rule out poorly understood barrier related effects, the stress voltages are selected to be in the overspill region, where a second electron channel is formed at the dielectric interface at high forward gate biases. During recovery, emitted electrons are transported away from the interface through thermionic field emission and the barrier field.

With two sets of normally-distributed NMP traps, one describing the more permanent and one the more recoverable part of the degradation, excellent agreement for three different stress conditions is achieved (see Fig. 5). Although the absolute value of the V_{th} drift is very large

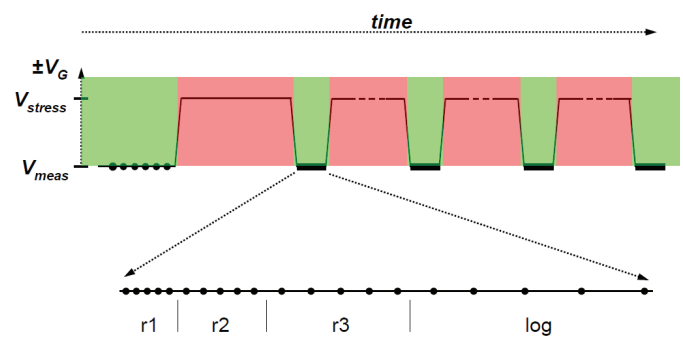

Fig. 4. The sequences of gate bias stress and recovery over time. The stress times between subsequent cycles are multiplied by a factor of 10. The recovery points are uniformly distributed on a log scale.

compared to other technologies, even for the highest ΔV_{th} only a small number of defects are occupied. Assuming the defect density calculated from Fig. 2, the largest ΔV_{th} in Fig. 5 corresponds to a trap occupancy of approximately 25%. It has to be noted that this value is still a conservative estimate, since only donor-like traps are considered, providing exactly the necessary amount of positive initial charge.

The large trap density together with the fact that in GaN HEMTs the electron channel is separated from the interface through a barrier layer results in a strong sensitivity of the surface potential on the trap occupancy. This is in contrast to silicon technologies, where this effect is typically negligible since at usual MOSFETs operating conditions a considerable amount of charge is present at the interface. This makes the surface potential not very sensitive to changes of the trap occupancy. The impact of the V_{th} drift on the surface potential of the HEMT can be seen in Fig. 6. As depicted, the change in the surface potential can be 2.8 V above the equilibrium value for the highest stress bias during the MSM sequence. Subsequently, the strong shift in the surface potential has

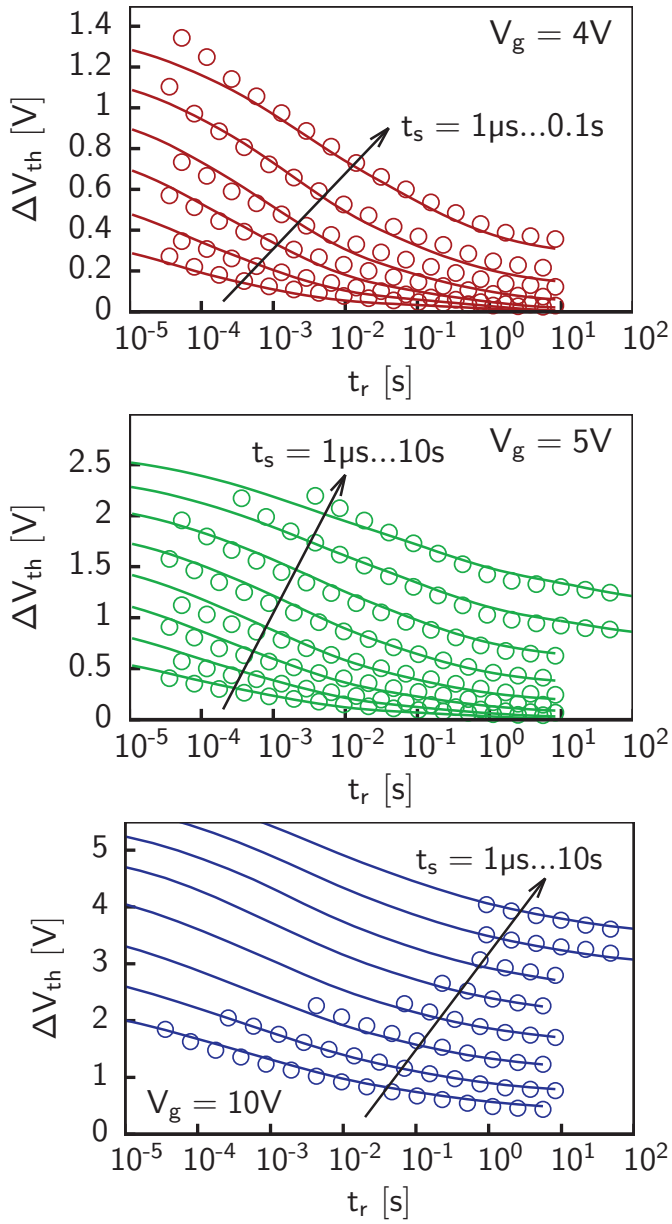

Fig. 5. Simulated and measured ΔV_{th} recovery curves for measurement-stress-measurement sequences with stress voltages of 4 V (red), 5 V (green) and 10 V (blue). Note that the measured forward drift behaviour and its stress time and bias dependency is described by two sets of NMP trap parameters.

a significant impact on the V_{th} drift characteristics. Even if the potential shift is partly reversed during recovery, a permanent shift of φ_s builds up during the measurement sequence. The amount of surface potential drift strongly depends on the previous stress and recovery cycles and causes a shift of the effective trap energies.

The impact of charge feedback on the overall drift is shown in Fig. 7. If the simulations are not performed self-consistently, that is the trapped charges are not considered for the calculation of the capture and emission times, almost twice as much degradation compared to self-consistent simulations is observed. This effect can be understood by looking at the capture/emission time (CET)

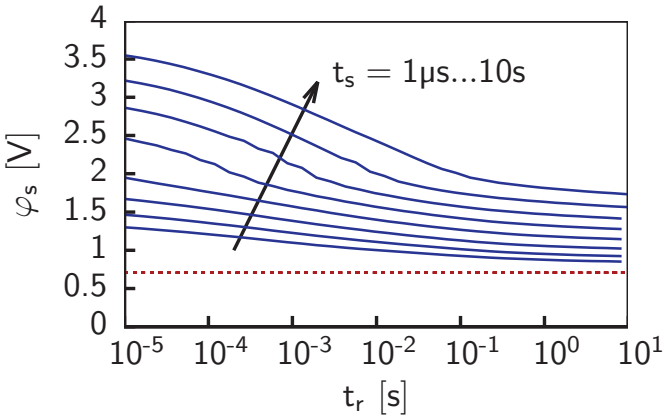

Fig. 6. The surface potential for increasing stress times during recovery at $V_g = 10$ V. The equilibrium value is given by the dotted red line. The permanent shift in φ_s causes a shift of the effective trap energies. Note that this shift depends on the previous stress and recovery cycles.

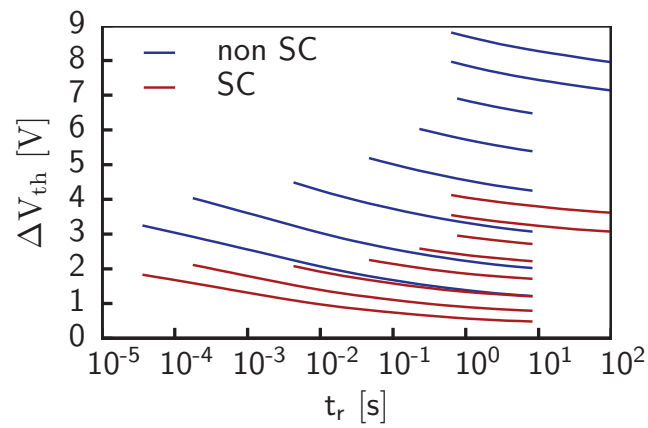

Fig. 7. A comparison between self-consistent (SC) and non self-consistent simulation at $V_g = 10$ V. It can be seen that the influence of the trap occupancy on the degradation dynamics is very strong, which is in contrast to silicon based devices. For self-consistent simulations, the inhomogeneous potential in the oxide leads to changes in the shape of the recovery transients.

maps in Fig. 8 [12]. Initially, almost all traps are empty and thus positively charged. During the first stress cycle (top row), most of the defects are pulled into the active energy region (red areas as described in Fig. 3), where they can potentially become occupied by an electron.

If a significant amount of defects capture a charge, the local potential at the defect site increases, causing a shift to larger time constants for the defects and their nearest neighbours. Also the Fermi level at the dielectric interface and thus the surface potential depends on the charge state of the defects. During recovery, a large fraction of those defects emit their charge again, reversing most of those effects. However, some defects remain charged, resulting in a residual shift of the local potential and therefore a change of time constants for some of the defects. The amount of residual shift strongly depends on the recovery time between two stress cycles. During the next stress cycle, a smaller number of defects will capture a charge because of the energetically higher distribution of defects caused by the remaining surface potential shift after recovery.

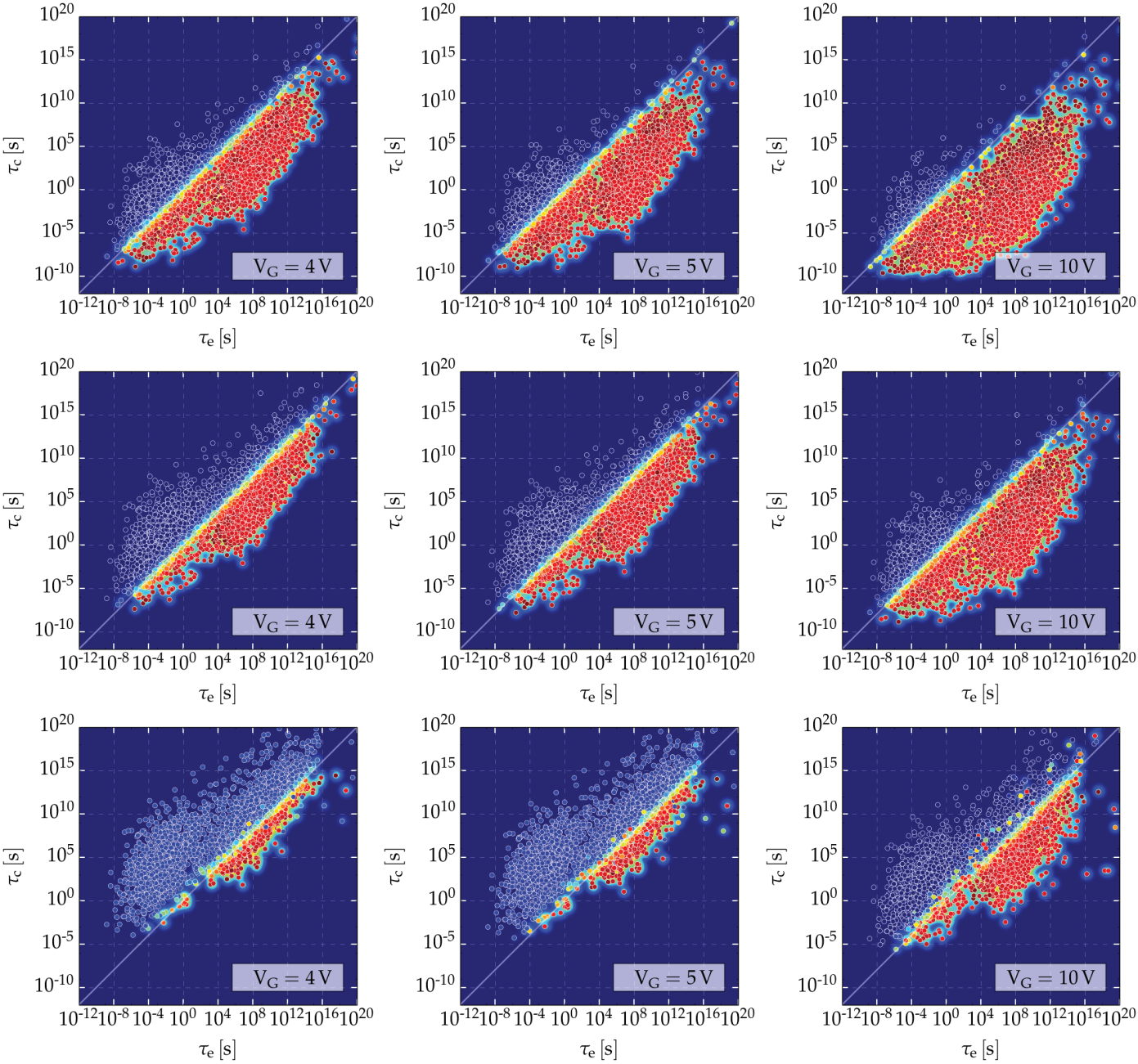

Fig. 8. CET maps for stress voltages of 4 V, 5 V, and 10 V (from left to right). The top and mid rows are extracted from transient simulations after accumulated stress times of 1 µs and 11.11 s, whereas the bottom row shows the thermodynamic equilibrium. Charges located in the active energy region at a particular time (see Fig. 3) can potentially capture an electron (red). It can be seen that those charges are a function of stress bias and time, but also the recovery during the MSM sequences. With increasing stress times, the charge distributions in the CET map converge toward their equilibrium values (bottom row).

The second row in Fig. 8 shows the defects after the last stress cycle. It can be seen that the charge feedback mechanism already results in a significant shift in the time constants compared to the first stress cycle. With increasing degradation, the active energy region for the defects shrinks, meaning that the amount of charges which can be trapped decreases from cycle to cycle. The asymptotic limit of this behaviour can be seen in the third row, where the thermodynamic equilibrium for the three stress voltages is shown.

The degradation caused by subsequent stress cycles are not equivalent to a single stress pulse with the same overall stress time because the local potential affecting each trap at the beginning of each stress cycle is a function of the stress and recovery history. As stated before, the surface potential at the dielectric interface is very sensitive to changes in the trap occupancy, making the Fermi level seen by the traps stress and recovery dependent too. Furthermore, the spatial distribution of traps in the interface region also causes an inhomogeneous potential in the oxide. This inhomogeneous energy shift seen by each individual trap also induces changed trapping kinetics, which can be seen in Fig. 7.

V. Conclusions

We have demonstrated that the experimentally observed V_{th} drift in GaN MIS-HEMTs can be well described using a non-radiative multi-phonon model for charge capture and emission. Our investigation of the charge-feedback mechanisms at forward bias stress conditions show that the observed V_{th} drift can only be modelled correctly by self-consistent, transient simulations. In particular, the degradation can only be described correctly when the stress and recovery history is taken into account because the surface potential and thus the effective trap energies are a function of stress history. Finally, we show that the inhomogeneous potential in the oxide leads to changes in the kinetics for each individual trap, which has to be considered for an accurate description.

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