Reliability of Single-Layer MoS_2 Field-Effect Transistors with SiO_2 and hBN Gate Insulators

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***Abstract*—We study the hysteresis and bias-temperature instabilities in single-layer MoS_2 FETs with SiO_2 and hBN gate insulators and attempt to capture the correlation between these phenomena. In agreement with previous literature reports, our results show that the use of hBN as a gate insulator reduces the hysteresis. Furthermore, we show that the impact of the bias-temperature instabilities is weaker for MoS_2/hBN transistors. However, at higher temperature the reliability of MoS_2/hBN FETs is reduced due to thermally activated charge trapping.**

I. Introduction

Molybdenum disulfide (MoS_2) is a next-generation "beyond graphene" material which is now considered a promising candidate for future device applications. Contrary to graphene, MoS_2 has a sizable bandgap of around 1.3 – 1.8 eV [1], which thus allows to overcome the main limitation of graphene for electronic applications. In the meantime, numerous groups have succeded at fabricating MoS_2 FETs with either SiO_2 [2–13], Al_2O_3 [14, 15] or hexagonal boron nitride (hBN) [16] as a gate insulator. However, investigation of their reliability has been mostly restricted to statements confirming the existance of a hysteresis in the gate transfer characteristics for different measurement conditions [3, 4, 9, 15, 16]. In addition, only few attempts at analyzing the bias-temperature instabilities (BTI) in MoS_2 FETs have been undertaken so far [7, 8, 10], albeit limited to MoS_2/SiO_2 devices. In particular, the recovery dynamics have not been analyzed at all by now.

Here we perform a detailed study of both the hysteresis and BTI in single-layer MoS_2 FETs with SiO_2, hBN/SiO_2 and hBN insulators, and capture the correlation between these phenomena. Also, we quantify the observed BTI degradation/recovery dynamics using the universal relaxation model [17, 18] which has been previously developed for Si technologies. Finally, we compare our findings for different devices and draw some conclusions regarding the considerably improved reliability of MoS_2 devices with hBN gate insulators.

II. Devices

We examine single-layer MoS_2/SiO_2 and MoS_2/hBN FETs with channel length L=1 μm and widths W=4–8 μm. In our MoS_2/SiO_2 devices (Fig. 1a) a mechanically exfoliated single-layer MoS_2 channel [19] is situated on top of a 90 nm thick SiO_2 layer. In the transistors with hBN, MoS_2 is stacked between two 90 nm thick hBN layers (Fig. 1b) using the method of [20]. In order to allow for a more detailed analysis of hBN vs. SiO_2, we added an additional Ti/Au gate between

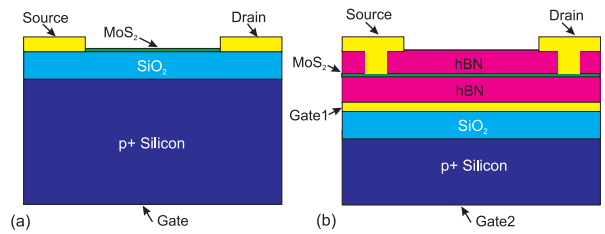

Fig. 1: Schematic configurations of our MoS_2/SiO_2 (a) and MoS_2/hBN (b) transistors. The insulator thickness of both SiO_2 and hBN is around 90 nm. The device with hBN has two gate contacts, one through the highly doped Si substrate and the other through a Ti/Au pad which is situated between the SiO_2 and hBN layers. The drain and source contacts are made of Ti/Au.

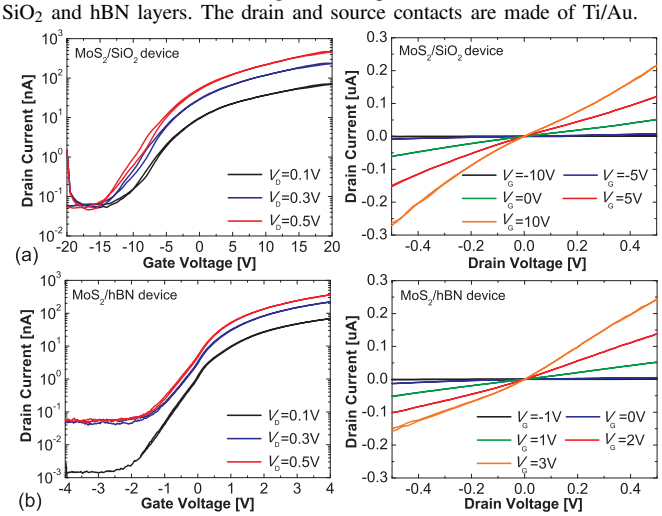

Fig. 2: The gate transfer (I_D-V_G) and output (I_D-V_D) characteristics of our MoS_2 FETs with SiO_2 (a) and pure hBN (b). In agreement with [4, 16], the transfer characteristics show some hysteresis, which is considerably smaller for MoS_2/hBN devices (cf. [16]). The output characteristics show a quasi-linear current increase within the narrow V_D range used.

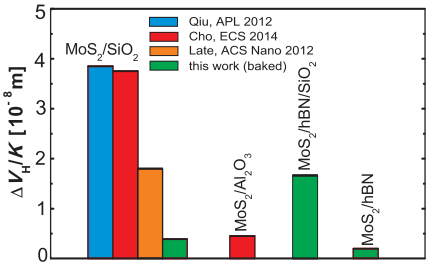

Fig. 3: Comparison of the normalized hysteresis width for our MoS_2 FETs with literature results [3, 4, 15]. In all cases the measurements have been performed in vacuum, because measurements in the ambient show considerably larger ΔV_H [4]. Although the hysteresis strongly depends on the temperature, sweep rate and the sweep range $V_{Gmin} \ldots V_{Gmax}$, the maximum values of ΔV_H measured for our MoS_2/SiO_2 and MoS_2/hBN devices are the smallest reported so far.

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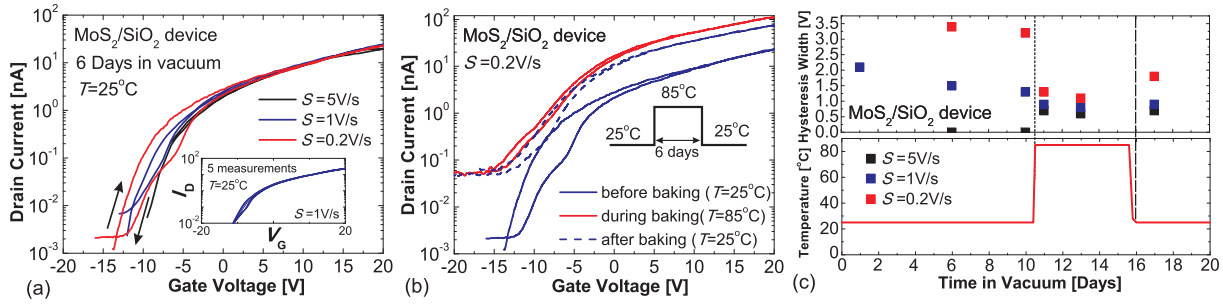

Fig. 4: (a) The I_D-V_G characteristics of our MoS_2/SiO_2 device measured using different sweep rates. While at a constant sweep rate the hysteresis is stable (inset), for smaller S it becomes more pronounced. (b) The I_D-V_G characteristics measured using $S = 0.02$ V/s before, during and after 6 days at $T = 85°C$. Baking of the device at $T = 85°C$ results in a considerably smaller slow sweep hysteresis and also leads to a larger I_D. (c) Evolution of ΔV_H measured for the MoS_2/SiO_2 device versus time in vacuum. During the first 10 days at $T = 25°C$, a large hysteresis was observed for small S, but no significant hysteresis for large S. At $T = 85°C$, ΔV_H measured using slow sweeps was significantly reduced. At the same time, a considerable hysteresis appeared for fast sweeps. Back at $T = 25°C$, some increase in hysteresis width measured with small S is pronounced. However, ΔV_H did not return to its initial values. This implies that baking anneals a significant fraction of slower traps, while making the remaining ones faster.

the hBN and the SiO_2 layer. Thus, we can operate these devices either with a hBN gate insulator by directly contacting the Ti/Au plate or with a hBN/SiO_2 stack through the highly doped Si substrate. In Fig. 2 we show the gate transfer (I_D-V_G) and output (I_D-V_D) characteristics of our devices which are consistent with previous literature reports [4, 16]. The mobility can reach 1 cm^2/Vs for MoS_2/SiO_2 FETs and 3 cm^2/Vs for MoS_2/hBN devices (cf. [3]). At the same time, the I_{on}/I_{off} ratio measured with high current resolution can exceed 10^5. Furthermore, in Fig. 3 we show that the maximum hysteresis width ΔV_H extracted around V_{th} and normalized by $K = (V_{Gmax}$-$V_{Gmin})/d_{ox}$ in our devices is typically lower than what has been reported by other groups [3, 4, 15]. Interestingly, for MoS_2/hBN FETs ΔV_H is considerably smaller than for their counterparts with other insulators. This is in agreement with the results reported in [16].

III. Experiment

The performance of MoS_2 FETs is known to be sensitive to the detrimental impact of the environment [4]. For this reason, all our measurements were performed in a vacuum (5×10^{-6}–10^{-5} torr). The hysteresis was investigated by measuring the I_D-V_G characteristics at $V_D = 0.1$ V, while the gate bias sweep rate S has been varied between 0.04 and 8000 V/s by adjusting the step voltage V_{step} and the sampling time t_{step}. The latter allowed us to detect the contribution of a large fraction of the fast traps responsible for the hysteresis. The BTI behavior was studied using subsequent stress/recovery cycles with either increasing stress time t_s or gate voltage V_G (cf. [21]). In order to check the temperature activation of trapping/detrapping processes, our experiments have been performed at $T = 25°C$ and $T = 85°C$.

IV. Hysteresis Stability

In Fig. 4a we show that the I_D-V_G characteristics of our MoS_2/SiO_2 FETs exhibit some hysteresis even after several days in vacuum at $T = 25°C$. As shown in the inset, this hysteresis is well reproducible at a constant sweep rate. Also, in agreement with [4] it becomes considerably larger when the sweep rate is decreased. This means that the hysteresis in our MoS_2/SiO_2 FETs is dominated by slower traps. At the same time, the temperature increase up to 85°C considerably reduces the hysteresis width measured using a very small $S = 0.02$ V/s (Fig. 4b), while also leading to a larger drain current. However, when the temperature is changed back to 25°C, the device exhibits a better performance in terms of both I_D and ΔV_H. This is most likely associated with evaporation of water molecules [4], which act as the trapping sites, from the non-covered MoS_2 surface. In Fig. 4c we show the evolution of the hysteresis at different sweep rates versus time in vacuum as a function of temperature. During the first days at $T = 25°C$, a hystersis is only observed for slow sweeps and decreases with time. At $T = 85°C$, ΔV_H for small S decreases abruptly. However, the hysteresis suddenly becomes pronounced at larger sweep rates. Finally, when the temperature is returned back to 25°C the slow sweep ΔV_H slightly increases, while nearly no change was seen for fast sweeps. Thus, in our MoS_2/SiO_2 FETs the temperature treatment reduces the amount of slower traps by means of their annealing and transformation into faster traps.

We proceed with a more detailed analysis of the hysteresis by measuring the I_D-V_G characteristics using different t_{step}, V_{step} and gate voltage sweep intervals $V_{Gmin} \ldots V_{Gmax}$. For a more general comparison of the results measured for different gate insulators, we introduce the measurement frequency $f = 1/(Nt_{step})$ with the number of points $N = 2((V_{Gmax}$-$V_{Gmin})/V_{step}+1)$. In Fig. 5 we demonstrate that for all three insulators the hysteresis widths measured using different V_{step} and t_{step} form a universal $\Delta V_H(f)$ dependence. Fig. 5a shows the $\Delta V_H(f)$ dependences measured for MoS_2/SiO_2 FETs at $T = 85°C$ and also at $T = 25°C$ before and after $T = 85°C$ measurements. In all cases ΔV_H becomes larger for lower frequencies, which confirms that the hysteresis in these devices is dominated by slower traps with $f < 0.01$ Hz. At the same time, during and after baking at $T = 85°C$ ΔV_H associated with slower traps is considerably reduced. This most likely means that the corresponding trapping sites (e.g. water molecules) are situated on top of the MoS_2 surface. Hence, annealing of these traps is more efficient than thermal activation of the remaining defects. Conversely, the contribution of faster traps ($0.01\,\text{Hz} < f < 1\,\text{Hz}$) becomes more pronounced at $T = 85°C$. This suggests that the time constants of those traps which have not been annealed become smaller. Interestingly, the

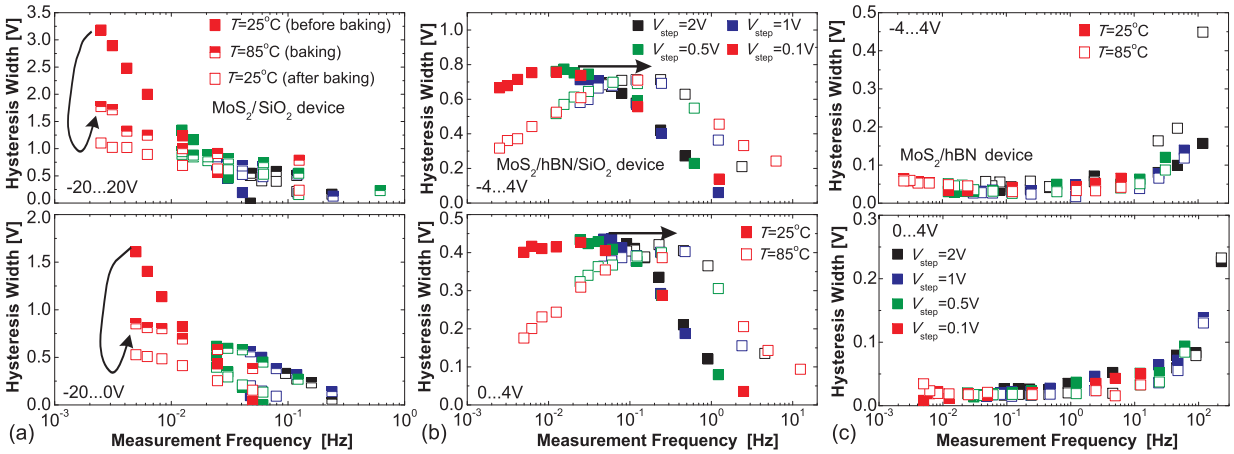

Fig. 5: (a) The frequency dependence of ΔV_H measured for MoS_2/SiO_2 FETs using the gate voltage sweep ranges -20...20 V (top) and -20...0 V (bottom). The three datasets correspond to the results obtained before, during and after 6 days of baking at $T = 85°C$. The hysteresis is dominated by slower traps, which become partially annealed during baking. (b) The frequency dependence of ΔV_H measured for $MoS_2/hBN/SiO_2$ FETs using the sweep ranges $-4\ldots4$ V (top) and $0\ldots4$ V (bottom). In both cases we observe a maximum of ΔV_H, which is reduced for narrower sweep ranges. At $T = 85°C$ the maximum is shifted toward higher f, which means that the time constants of the defects become smaller. (c) The corresponding results for MoS_2/hBN FETs. Contrary to the previous two devices, the fraction of slower traps is negligible, while the hysteresis is dominated by ultra-fast traps. Hence, the maximum of ΔV_H is most likely at even higher frequencies outside our measurements range.

same trends are observed independently of the sweep range, although ΔV_H becomes smaller for narrower sweep ranges (cf. [9]). In Fig. 5b we provide corresponding results for $MoS_2/hBN/SiO_2$ FETs. Similarly to MoS_2/SiO_2 devices, ΔV_H measured using slow sweeps is reduced at higher temperature, while the fast sweep hysteresis becomes significantly larger. However, the resulting frequency dependence contains a maximum of ΔV_H, which shifts towards higher frequencies at $T = 85°C$. As such, we conclude that all traps which contribute to the hysteresis in $MoS_2/hBN/SiO_2$ FETs are thermally accelerated. Interestingly, the amount of slower traps in these devices is limited, which leads to a reduced hysteresis for very low f at $T = 85°C$. The results for MoS_2/hBN devices are shown in Fig. 5c. Contrary to the previous two cases, the hysteresis in MoS_2/hBN FETs is dominated by ultra-fast traps, while the contribution of slower traps is negligible. Also, some increase in ΔV_H at higher temperature is observed.

A comparison of our findings for the different gate insulators allows us to conclude that for MoS_2/SiO_2 FETs the hysteresis is mostly dominated by slower traps, while for their $MoS_2/hBN/SiO_2$ counterparts an increased contribution of faster traps is observed. Finally, in MoS_2/hBN devices the hysteresis is purely related to ultra-fast traps. Interestingly, in all three cases the temperature dependence is similar. Namely, the contribution of slower traps is reduced and the contribution of faster traps is increased at higher temperature, shifting the ΔV_H dependence toward higher f.

V. BTI Analysis

We proceed with the analysis of BTI degradation/recovery dynamics in MoS_2 FETs, which can be expressed by the threshold voltage shift ΔV_{th} versus the relaxation time t_r traces. Fig. 6 shows the evolution of the I_D-V_G characterestics for MoS_2/SiO_2 FETs after subsequent positive BTI (PBTI) stresses with total stress time $t_s = 10$ ks and increasing V_G. While being recoverable, the degradation becomes more pronounced for larger V_G. At the same time, the relative ΔV_{th} remaining after $t_r = 10$ ks decreases from 85 % of the initially measured ΔV_{th} for $V_G = 5$ V towards 60 % for stronger stresses.

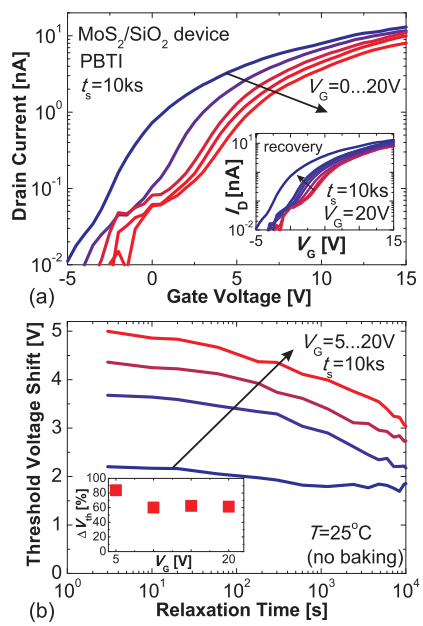

Fig. 6: (a) Degradation of the gate transfer characteristics of the MoS_2/SiO_2 FET after subsequent PBTI stresses with total stress time $t_s = 10$ ks and increasing V_G. The inset shows the time evolution of the I_D-V_G characteristics during recovery. (b) The resulting recovery traces for the threshold voltage shift ΔV_{th}. The degradation is partially recoverable and strongly increases with increasing stress V_G. While for the stress with $V_G = 5$ V the relative ΔV_{th} remaining after a relaxation time $t_r = 10$ ks is around 85% of the initially measured value, for stronger stresses it is close to 60% (inset). Note that the measurements of the full I_D-V_G sweep at each recovery point introduce a delay of about 3 s.

Next we examine the temperature dependence of the BTI degradation/recovery dynamics in MoS_2/SiO_2 FETs. Fig. 7 shows the results obtained using subsequent PBTI

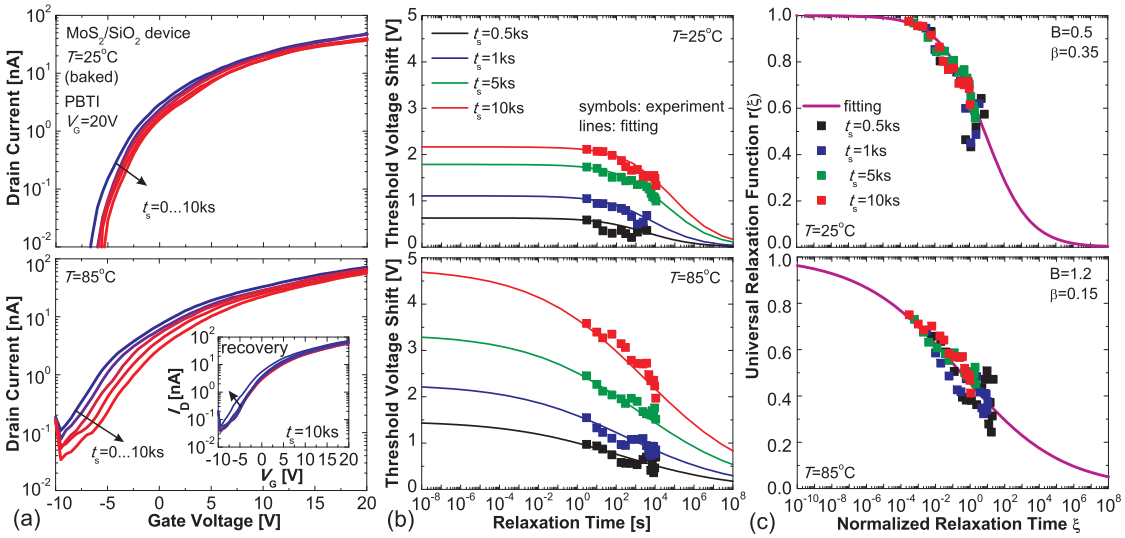

Fig. 7: (a) Degradation of the gate transfer characteristics of the MoS_2/SiO_2 FET after subsequent PBTI stresses with $V_G = 20\,V$ and increasing t_s at $T = 25°C$ (top) and $T = 85°C$ (bottom). (b) The resulting ΔV_{th} recovery traces can be fitted using the universal relaxation model known from Si technologies [17, 18]. (c) Normalized recovery traces follow the universal relaxation relation [17, 18] $r(\xi) = 1/(1+B\xi^{\beta})$ with $\xi = t_r/t_s$ as the normalized relaxation time and empirical fitting parameters B and β. Similarly to Si technologies, at higher temperature the degradation is stronger and the degree of recovery is larger. This agrees with our hysteresis measurements, which show that at higher temperature traps become faster (Figs. 4–5). The parameters B and β are very similar to those obtained from Si data (Fig. 10), which confirms the similarity in the underlying physical degradation processes.

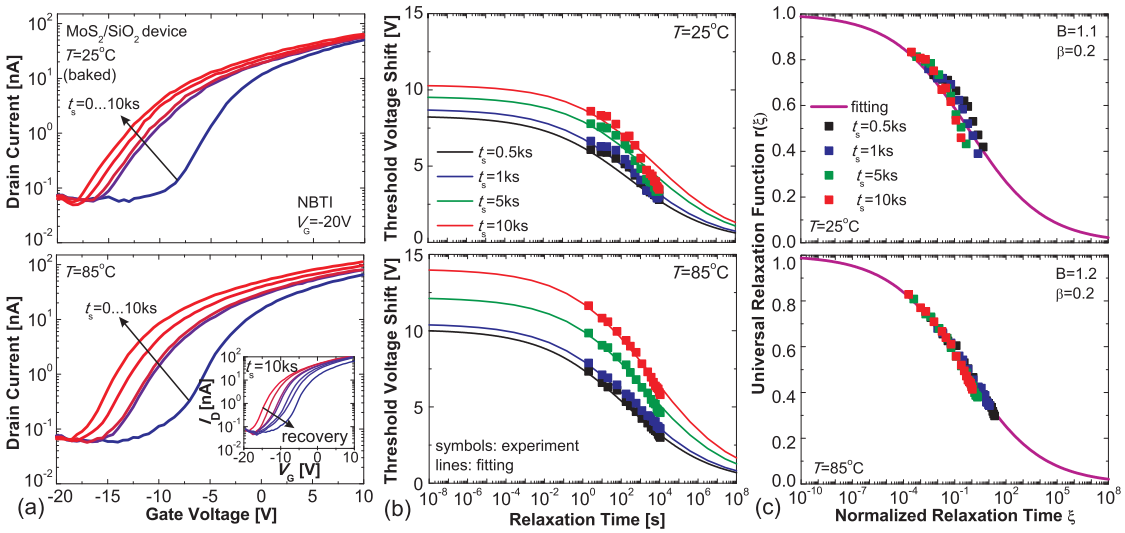

Fig. 8: (a) Degradation of the gate transfer characteristics of the MoS_2/SiO_2 FET after subsequent NBTI stresses with $V_G = -20\,V$ and increasing t_s at $T = 25°C$ (top) and $T = 85°C$ (bottom). The observed threshold voltage shifts are significantly larger than for PBTI, while the recovery is also stronger. This is most likely associated with the difference in the energy levels of the defects involved in the underlying charge trapping processes. (b) Similarly to Fig. 7, the recovery traces for ΔV_{th} can be fitted reasonably well using the universal relaxation model. The temperature dependence of the degradation/recovery dynamics is similar to the case of PBTI. Namely, larger shifts and stronger recovery are observed at higher temperature, which is also the case for Si technologies. (c) The normalized recovery again follows the universal relaxation relation.

stress/recovery cycles with increasing t_s. In order to compare the BTI degradation/recovery dynamics with Si technologies, we use the universal relaxation model [17, 18], which assumes recovery to follow the universal relaxation function $r(\xi) = 1/(1+B\xi^{\beta})$ with the normalized relaxation time $\xi = t_r/t_s$ and empirical fitting parameters B and β. All recovery traces for our MoS_2/SiO_2 devices can be fitted reasonably well (Fig. 7b) and the normalized recovery is universal (Fig. 7c). Just like in Si technologies, stronger degradation and faster recovery are observed at higher T, which is due to the thermally activated nature of carrier trapping [22]. However, MoS_2 FETs exhibit both PBTI and negative BTI (NBTI) on the same device [8, 10]. The related results for negative BTI (NBTI) in MoS_2/SiO_2 FETs are provided in Fig. 8. While V_{th} is shifted in the opposite direction, the observed shifts are larger than for PBTI. This is likely due to a difference in the energetic alignment of the involved traps. In all cases, the recovery traces can be fitted reasonably well by the universal model, which confirms a similarity of the two phenomena. Moreover, the temperature dependence of NBTI degradation is similar to PBTI. Namely, stronger shifts and faster recovery are observed at $T = 85°C$.

Fig. 9 shows the results for PBTI and NBTI in MoS_2/hBN

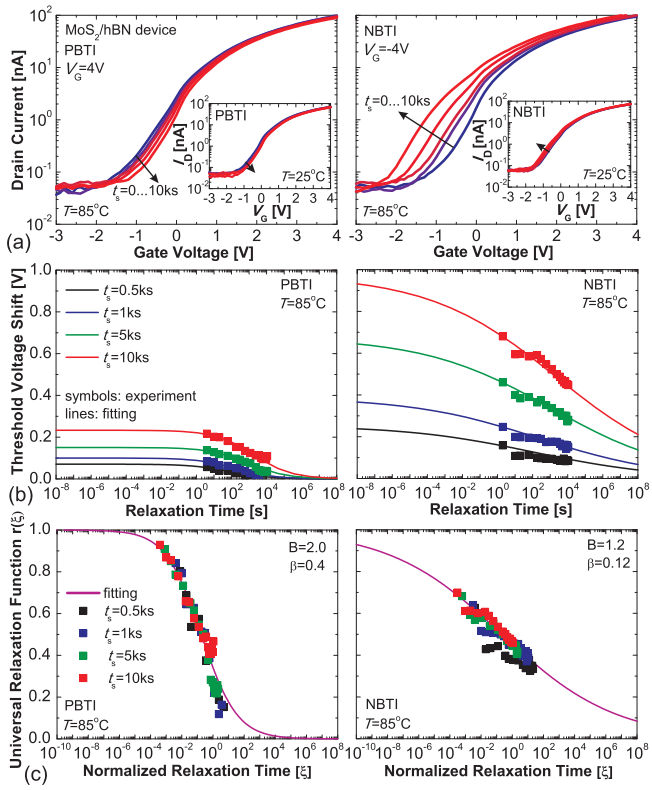

Fig. 9: (a) Degradation of the gate transfer characteristics of the MoS_2/hBN FET after subsequent PBTI (left) and NBTI (right) stresses at $T = 85°C$. The insets show that the degradation observed after both PBTI and NBTI at $T = 25°C$ is significantly smaller. (b) The ΔV_{th} recovery traces at $T = 85°C$ can again be fitted using the universal relaxation model as the normalized recovery is universal (c). Similarly to MoS_2/SiO_2 devices, the threshold voltage shifts are larger for NBTI than for PBTI and more recoverable. Also, the significant increase in the drifts of the MoS_2/hBN devices at higher temperature agrees with the increased hysteresis (Fig. 5c).

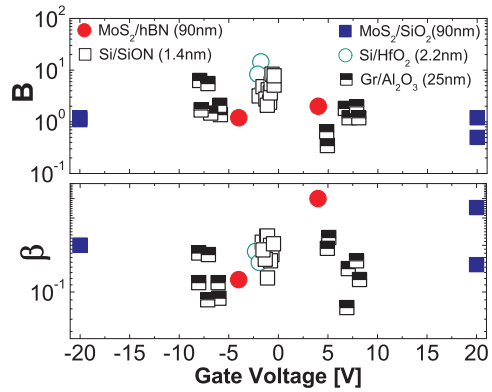

Fig. 10: The empirical parameters B and β which have been used for fitting the recovery traces of our MoS_2/SiO_2 and MoS_2/hBN FETs are very similar to those previously used for Si and graphene FETs [21].

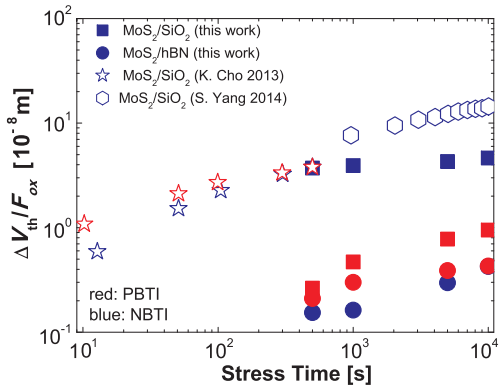

Fig. 11: Comparison of ΔV_{th} normalized by the oxide field F_{ox} for our devices against literature data [8, 10]. While the NBTI shifts are comparable for our MoS_2/SiO_2 FETs, PBTI is significantly weaker in our devices. Finally, our MoS_2/hBN devices show superior reliability with respect to both PBTI and NBTI.

FETs. These devices exhibit a negligible degradation at $T = 25°C$, while at $T = 85°C$ both PBTI and NBTI shifts become more pronounced and agree with the universal relaxation model. Interestingly, NBTI in MoS_2/hBN devices is stronger than PBTI, which is similar to MoS_2/SiO_2 FETs. In Fig. 10 it is shown that the parameters B and β which are used for fitting of the recovery traces of our MoS_2 FETs are very similar to those previously used for Si technologies and graphene FETs [21]. This indicates a similarity in the physical processes underlying the BTI dynamics. In Fig. 11 we compare the normalized ΔV_{th} measured within this work with the results from [8, 10]. Clearly, our MoS_2/SiO_2 FETs show a better stability with respect to PBTI stress, while the V_{th} shifts caused by NBTI are comparable to the previous literature reports. At the same time, hBN devices exhibit superior BTI reliability. This is in agreement with our hysteresis results, showing that the amount of slow traps in MoS_2/hBN FETs is small and that the main reliability issue of these devices is associated with ultra-fast traps.

VI. Conclusions

We have demonstrated that our MoS_2 FETs with SiO_2 and hBN exhibit a smaller hysteresis and better BTI stability than similar devices reported by other groups. Moreover, hBN as a gate insulator reduces the impact of slow traps and improves the BTI reliability. While the main reliability issue in MoS_2/hBN FETs is associated with ultra-fast traps, we show that at higher temperature the BTI reliability of hBN is reduced due to thermally activated charge trapping. Finally, it has been shown that the BTI recovery traces measured for all our MoS_2 FETs follow the universal relaxation relation previously developed for Si technologies. Together with our previous studies performed on graphene FETs [21], this underlines that the BTI degradation/recovery dynamics in next-generation 2D FETs are similar to their counterparts in Si FETs.

VII. Acknowledgements

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