A Systematic Study of Charge Trapping in Single-Layer Double-Gated GFETs


1Institute for Microelectronics (TU Wien), Gusshausstrasse 27–29, 1040 Vienna, Austria
2Ioffe Physical-Technical Institute, Polytechnicheskaya 26, 194021 St-Petersburg, Russia
3University of Siegen, Holderlinstrasse 3, 57076 Siegen, Germany

Email: illarionov@iue.tuwien.ac.at

Introduction: Graphene is a honeycomb carbon material which is now successfully applied as a channel in graphene FETs (GFETs) [1–5]. However, stability of modern GFETs is limited by a considerable hysteresis on the gate transfer characteristics [3]. Although several studies on this issue have been reported [3,6–9], different physical explanations have been put forward. Here we introduce an experimental technique allowing for a systematic study of the hysteresis in GFETs and show that in our devices this issue is dominated by thermally activated charging/discharging of oxide traps.

Devices: In our single-layer double-gated GFETs (L = 3–6 μm) the CVD graphene channel [10] is sandwiched between thermally oxidized SiO2 as a back gate oxide (tox = 85 nm) and e-beam evaporated SiO2 as a top gate oxide (t tox = 12 nm), see Fig. 1. The source/drain pads are made of a thermally evaporated Cr(20 nm)/Au(80 nm) stack and the top gate contact is 120 nm thick Al.

Experiment: In the spirit of [5], our measurements were performed in a vacuum (~5 × 10−6 torr). The hysteresis was investigated by measuring the back gate transfer (I d-V bg) characteristics at V d = 0.1 V. By using different step voltages V step and sampling times t step, we have varied the measurement frequency f = f = (N·t step) with N = 2((V bgmax−V bgmin)/V step +1) = 10−4 and 102 Hz. This allowed us to demonstrate that the dependence of the Dirac point voltage shift ∆V D = V D+−V D− versus f presents a unique fingerprint of the hysteresis dynamics. For a reliable determination of the hysteresis origin, we have measured the ∆V D(f) dependences using different sweep ranges V bgmin...V bgmax at T = 85°C and T = 165°C.

Results and Discussions: The output (I d-V D) characteristics of our GFETs (Fig. 2) show some signs of saturation for larger V D and V bg. At the same time, the I d-V bg characteristics (Fig. 3) exhibit an improvement after the I d-V D sweeps. The latter is attributed to self-annealing of graphene at high Id [11], which allowed us to achieve a better reproducibility of all further measurements. In Fig. 4 we show that the I d-V bg characteristics exhibit a clockwise hysteresis for low and high f, while a counterclockwise hysteresis is observed for moderate f (cf. [6,7]). As shown in Fig. 5, the resulting charged trap density shift ∆N T = C bg∆V D/q versus f is qualitatively similar for different devices. Namely, ∆N T becomes positive and reaches a maximum at f ∼ 10−3–10−2 Hz. In Fig. 6 we demonstrate that at higher T the ∆N T(f) dependence is shifted towards higher f, which is consistent with thermally activated charging/discharging processes. Namely, at low f discharging of back gate oxide defects is dominant, leading to a negative ∆N T, an effect which becomes larger at higher T and decreases for higher f. Although for very fast sweeps ∆N T should simply reach zero, we observe a change of the ∆N T sign while passing through a maximum. This is likely due to thermally activated charging of the defects situated in the top gate oxide, which introduces additional positive charges. Interestingly, in some cases at T = 85°C there is a second reversal of the trend of the hysteresis at very high f, which suggests a charging of the top gate defects with smaller time constants.

In Fig. 7 we show that the ∆V D(f) dependences are affected by the sweep range in their low f branch, especially at T = 165°C. This behaviour can be understood based on Fig. 8. At V bgmin = −40 V the Fermi level E F is close to the back gate oxide valence band. Hence, for low f most of the defects are charged before V bg = V D+ is reached. Then, a significant fraction of them is either discharged when V bgmax = 40 V is reached or continue to discharge during the reversed sweep. As a result, the amount of charged traps at V bg = V D− is much smaller than it was at V bg = V D+ (Fig. 8a), leading to a large clockwise hysteresis. However, if V bgmin = −20 V, the initial E F lies higher and the time spent in the hole conduction region is smaller. Hence, the concentration of charged defects at V bg = V D− is reduced (Fig. 8b). Thus, although sweeping to V bgmax = 40 V and back to V bg = V D− discharges most of them, the observed hysteresis is smaller. Finally, for V bgmin = −40...−20 V (Fig. 8c) the amount of charged defects at V bg = V D− is only insignificantly larger than at V bg = V D+, since a low V bgmax does not allow for efficient discharging. Hence, only a very small hysteresis is visible. Obviously, at lower T both charging and discharging are less efficient, making the difference smaller (Fig. 7a). At the same time, a weak impact of the V bg sweep range on ∆V D(f) right from the maximum further evidences the contribution of top gate defects.

Conclusions: We have suggested an experimental technique allowing for a simple and systematic benchmarking of the hysteresis in GFETs. Using this technique allowed us to demonstrate that in our GFETs the hysteresis is dominated by thermally activated oxide traps.
Fig. 1: Schematic layout of our single-layer double gated GFETs. S/D pads are made of Au/Cr and the top gate contact of Al.

Fig. 2: Output ($I_d-V_d$) characteristics measured at different back gate voltages exhibit a linear region and some signs of saturation for large $V_d$ and $V_{bg}$.

Fig. 3: The back gate transfer ($I_d-V_{bg}$) characteristics dramatically improve after $I_d-V_d$ sweeps. This is due to self-annealing of graphene at high $I_d$.

Fig. 4: The $I_d-V_{bg}$ characteristics exhibit a hysteresis which reverses at moderate measurement frequency $f$. We express the hysteresis width as a Dirac voltage shift $\Delta V_D = V_D^+ - V_D^- = q\Delta N_T/C_{bg}$.

Fig. 5: The hysteresis width versus the measurement frequency $f = 1/(N\cdot t_{step})$ obtained for different devices exhibits a maximum, around which the hysteresis changes sign. This is likely due to charging of top gate defects.

Fig. 6: At higher $T$ the maximum is shifted towards higher $f$, i.e. the time constants of both charging/discharging of traps in the back gate oxide and charging of their counterparts in the top gate oxide become smaller.

Fig. 7: The $\Delta V_D(f)$ dependences measured at $T = 85^\circ$C (a) and $165^\circ$C (b) using different sweep ranges. At higher $T$ the low $f$ part is more sensitive to the sweep range, since charging/discharging of the back gate oxide traps is more efficient.

Fig. 8: The hysteresis dynamics at $T = 165^\circ$C and $f = 10^{-3}$ Hz. (a) For $V_{bg} = -40...40$ V the time constants of most defects are small compared to the total sweep time. Hence, they can be charged/discharged and the hysteresis is large. (b) For $V_{bg} = -20...40$ V only a limited number of traps will be charged in the hole conduction region. Hence, their discharging will lead to a smaller hysteresis. (c) Finally, for $V_{bg} = -40...20$ V the amount of charged traps is large, but most of them will not discharge, leading to the smallest hysteresis.