Abstract: Bias temperature instabilities (BTI) are serious reliability issues in high-k technologies and occur for positive and negative stress voltages in both n- and p-MOSFETs. The cases with the strongest degradation, namely negative BTI (NBTI) in pMOS and positive BTI (PBTI) in nMOSFETs, are typically studied and modeled separately, which led to considerable inconsistencies regarding the distributions of the responsible defects. Here we present the first study which successfully describes all four combinations of BTI in n/p-MOSFETs within a single model. This was achieved by determining the physical properties of the defects in HfO$_2$ and SiO$_2$. Using our extraction method, any ambiguity regarding the location of the defect bands is completely eliminated, allowing for correct physics-based extrapolation of degradation data to use conditions.

Introduction: Bias temperature instabilities (BTI) remain a serious liability concern in high-k FinFETs. Although a number of controversial issues are not yet resolved,\textsuperscript{1,2} BTI is typically considered to be due to two components, one of them recoverable, and the other one more permanent. The recoverable component is often assumed to be due to charge trapping in the gate stack, with PBTI in nMOSFETs being due to electron traps and NBTI in pMOSFETs due to hole traps. Also, the two weaker degradation modes, namely NBTI in nMOSFETs and PBTI in pMOSFETs, are only studied occasionally.\textsuperscript{6,9–11} Here we demonstrate for the first time that the bias and time dependence of the recoverable components of all four combinations of BTI is a direct consequence of the unique position of the defect bands in the gate stack. Most importantly, any deviation in the defect band may go unnoticed for one combination, say NBTI in pMOSFETs, but lead to serious errors in another one.

Measurement setup: The experiments in this work were conducted on a high-k FinFET technology with a 1.2 nm (EOT) gate stack (HfO$_2$ with a SiO$_2$ interface layer), targeting the 14 nm node. In order to separate the recoverable from the more permanent contribution, we employ $V_D$ (V$_G$) ramps from accumulation to inversion,\textsuperscript{12} which remove the majority of the bias-dependent trapped charges, see Fig. 1. As shown in Fig. 2 for an exemplary stress setup, this method allows for reproducible extraction of the recoverable component even after a different stress “history”.

In order to extract the average degradation representative for the investigated technology, PBTI and NBTI on pMOS and nMOS devices were measured on 220 FinFETs connected in parallel for various gate voltages (positive and negative, for PBTI and NBTI, respectively) at 125°C. Also, for further validation, structures with two parallel Fins were measured to study the statistical distribution of the step-heights.

Physical modeling: We base our defect model on our previously developed four-state non-radiative multiphonon model.\textsuperscript{13} This model has already been successfully applied to various aspects of charge trapping in oxides, most importantly RTN, SILC, and BTI.\textsuperscript{8,14–17} For the simulation of $\Delta\nu_{bg}$, a set of microscopic defects was generated assuming that the model parameters, such as relaxation energies and defect levels, are normally distributed, while the traps were uniformly distributed across the SiO$_2$ (hole traps) or the HfO$_2$ (electron traps).

By calibrating our model to the comprehensive experimental data sets which cover all four combinations of BTI, these distributions were determined for HfO$_2$ and SiO$_2$. The distributions of the defect levels $E_T$ (w.r.t. the respective valence band edge), together with the defect concentrations $N_{OT}$ are given in the table below.

<table>
<thead>
<tr>
<th>$E_T$ (eV)</th>
<th>$N_{OT}$ (cm$^{-3}$)</th>
<th>$N_{OT}$ (cm$^{-2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.82 ± 0.43</td>
<td>2.9 × 10$^{20}$</td>
<td>6.4 × 10$^{13}$</td>
</tr>
<tr>
<td>4.44 ± 0.35</td>
<td>0.9 × 10$^{20}$</td>
<td>2.0 × 10$^{13}$</td>
</tr>
</tbody>
</table>

NBTI/PBTI in pMOSFETs: The pronounced degradation during NBTI is a direct consequence of the position of the defect bands as can be seen in the band diagrams in Fig. 3 for equilibrium conditions: Most hole defects in the SiO$_2$ are below the Fermi level of the channel and are thus neutral in the “pristine” device at $V_D = 0$ V. The shift of the trap levels of these defects due to the application of a negative gate voltage during NBTI enables hole capture from the channel. Additionally, some initially occupied electron traps in the HfO$_2$ now tend to emit electrons to the channel as they are far above the channel Fermi level. However, some electron traps will remain occupied because the rate of electrons coming from the gate can be larger than the rate of electron emission into the channel. Naturally, these defects will contribute to trap-assisted tunneling currents. Note that this effect does not necessarily depend on the position of the traps in the oxide but on the configurational details of the traps, for instance their relaxation energy.\textsuperscript{10}

Under application of a positive gate voltage (PBTI), again both, defects in the HfO$_2$ and in the SiO$_2$ cause degradation, but towards positive $V_D$. Since most SiO$_2$ defects are already neutral in the “pristine” device, their effect is much weaker, while the contribution of HfO$_2$ defects is found to be on the same order of magnitude as for NBTI of the same device.

The relative contributions of the electron and hole traps in the HfO$_2$ and SiO$_2$ are shown in Fig. 4 as a function of the stress bias. While electron trapping in the HfO$_2$ does contribute to both NBTI and PBTI, the degradation is mainly caused by hole trapping in the SiO$_2$ at all bias conditions. This is consistent with the observation that NBTI in high-k technologies is often perceived to be very similar to SiO$_2$ and SiON technologies.\textsuperscript{18,19}

NBTI/PBTI in nMOSFETs: Since the oxide materials and therefore the oxide defects are assumed to be the same for pMOS and nMOSFETs, all four degradation modes must be consistent with a single set of defect parameters. This is insofar a challenge to the model as the degradation for nMOSFETs is visibly different from the pMOSFET case. However, this difference is correctly reproduced by our model and can be again traced back to the location of the defect bands in the HfO$_2$ and SiO$_2$. Putting it differently, the peculiar behavior of NBTI/PBTI in n/p-MOSFETs can only be explained by a particular location of the defect bands, which can thus be used for a precise extraction of their location.

As shown in the band diagrams for the nMOS in Fig. 5, hole trapping in the SiO$_2$ during NBTI is less pronounced compared to pMOSFETs because the defects are shifted above the Fermi level of the channel to a smaller extent. This is due to the different work function differences for the nMOS compared to the pMOS (about 0.7 eV). For the same reason, the defects in the HfO$_2$ are shifted further below the Fermi level from the channel for PBTI, hence reducing the barrier for electron capture from the channel dramatically. This shifts the balance for electron emission towards the gate and electron capture from the channel in favor of the latter, resulting in stronger PBTI than NBTI.

As in Fig. 4, Fig. 6 compares the contributions of electron and hole traps to NBTI/PBTI of the nMOSFETs. Curiously, due to the unique position of the defect bands, PBTI is purely due to electron trapping in the high-k, consistent with previous high-k PBTI-only models\textsuperscript{5,20} and also fully consistent with the absence of PBTI in SiON technologies.\textsuperscript{6} The technologically less relevant case of NBTI/pMOS and PBTI/nMOS but spuriously amplify the other two as shown in Fig. 8.

Conclusions: We have demonstrated that all combinations of NBTI/PBTI in n/p-MOSFETs can be accurately understood at the physical level by considering an electron trap band in the HfO$_2$ and a hole trap band in the SiO$_2$ of a high-k gate stack. Correct physical modeling and understanding of all combinations of these instabilities is essential particularly from a circuit perspective where the gate voltages can cover wide ranges of both polarities.
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