Nanoscale Evidence for the Superior Reliability of SiGe High-k pMOSFETs

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***Abstract*— It is commonly accepted that the susceptibility of conventional Si channel pMOSFETs to the negative bias temperature instability (NBTI) is a serious threat to further scaling. One possible solution of this problem is the use of SiGe quantum-well devices, which not only offer high mobilities but also superior NBTI reliability compared to conventional silicon transistors. It has been speculated that the latter is due to the energetically higher valence band edge of the SiGe channel with respect to Si, which increases the energetic separation between the defect bands in the high-k gate stack and the channel. We investigate this claim by comparing the behavior of single-defects in nanoscale devices to the averaged behavior of the large number of defects visible in large-area devices. Using detailed TCAD simulations together with the four-state non-radiative multiphonon model we determine the energetic and spatial locations of the traps in the gate stack and confirm that the previously developed picture correctly explains the significant reliability benefits of SiGe channel devices.**

I. Introduction

The lifetime of nanoscale transistors is seriously affected by bias temperature instabilities (BTI). Single defects located inside the gate dielectrics can capture/emit electrons or holes and as a consequence modulate the surface potential within the conducting channel. The resulting reduction in the drain-source current is harmful to the operation of CMOS circuits. In order to compare charge trapping for different technologies, the impact of charge capture/emission on the drain-source current is commonly converted into an equivalent threshold voltage shift.

The aggressive scaling towards smaller devices has led to metal-oxide-semiconductor transistors (MOSFETs) with geometrical dimensions of several tens of nanometers. In general, the thinner the gate insulator becomes, the larger the gate leakage currents will be. To obtain physical thin gate oxides and at the same time avoid high leakage currents, high-k gate stacks have been introduced [1–4]. In modern devices the gate dielectric often consists of an HfO_2/SiO_2 (HK/IL) stack which is contacted with a metal gate (MG).

Nonetheless, in high-k MOSFETs BTI still remains a severe reliability issue. Recent investigations have shown that the detrimental impact of NBTI on device performance of high-k pMOSFETs can be significantly reduced using SiGe channels [5–8]. The SiGe channel devices have been initially introduced to exploit the higher mobility of the SiGe channel compared to conventional Si channel devices. At the same time, a significantly improved reliability with respect to NBTI has been observed. Apparently counter-intuitively, it was found that devices with a very thin Si cap layer on top of the SiGe channel resulted in the best reliability performance, suggesting that the crucial role of the Si cap is not to act as a tunneling barrier for channel holes, but instead to enable the fabrication of a high-quality SiO_2 interfacial layer [9]. It has been previously speculated that this reliability boost is a result of the favorable energetic alignment of the SiGe channel with respect to the defect band in the high-k gate stack. Compared to Si devices, the valence band in the SiGe channel is energetically higher, resulting in a smaller overlap with the defect states and thus reduced charge trapping.

In nanoscale transistors just a handful of defects are present. Thus the contribution of a single-trap to the threshold voltage shift can be studied individually. For that the time-dependent defect spectroscopy (TDDS) has been recently proposed [10–12]. Although the TDDS has been used to study single defects in SiON MOSFETs [10–13], less focus has been put on HK devices [14–16]. In contrast to nanoscale transistors, in large area devices the average contribution of a large number of defects to the threshold voltage shift can be studied.

To understand and model the observed recovery of pMOSFETs subjected to NBTI stress, the non-radiative multiphonon (NMP) model is often used [17, 18]. So far, the NMP model has been successfully used to explain the complex bias dependence of the capture/emission times of single-traps together with their temperature dependence in SiON MOSFETs [10, 13, 19, 20].

First we use nanoscale SiGe pMOSFETs and extract 19 single-traps by applying the TDDS to devices with two different Si cap layer thicknesses and reference Si transistors. From the recovery traces we calculate the cumulative complementary distribution function (CCDF) of step heights and show that unimodal and bimodal CCDFs are obtained for our SiGe quantum-well transistors, depending on the Si cap thickness. In addition to that we record recovery traces from large area devices using an extended measure-stress-measure (eMSM) scheme [21]. Afterwards we use the NMP model to reproduce the bias and temperature dependent capture/emission time characteristics of our single-traps and the recovery data recorded on the large area devices. All detailed TCAD simulations are performed with our device simulator

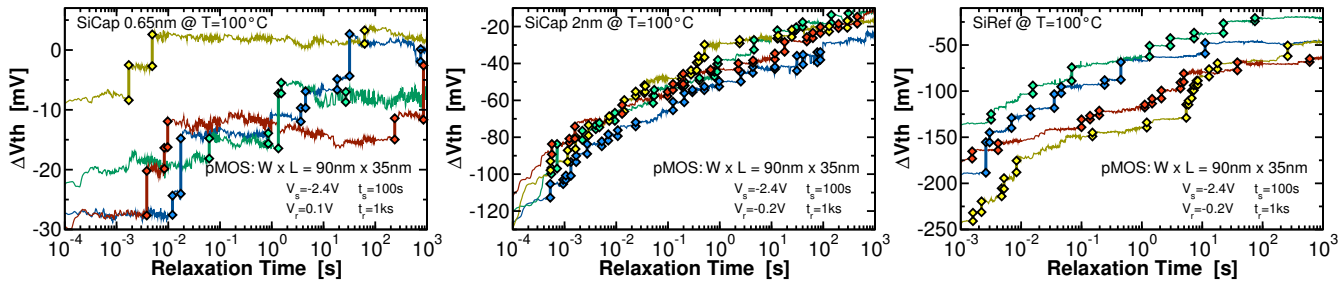

Fig. 1: The emission events of individual defects are clearly visible in the recovery traces of our nanoscale transistors. As can be seen in the recovery traces the number of traps accesible, i.e. the trap density, increases with larger SiCap layer thickness (**left**: $d_{\mathrm{SiCap}} = 0.65\,\mathrm{nm}$ and **middle**: $d_{\mathrm{SiCap}} = 2\,\mathrm{nm}$). The largest threshold voltage shift, however, is observed from the reference device (**right**). First we investigate the devices with the thin Si cap layer where a particularly high stress bias of $V_{\mathrm{G}}^{\mathrm{s}} = -2.4\,\mathrm{V}$ has to be used to observe a measureable degradation (**left**). To achieve comparable results the recovery traces of the two other device variants are recorded after the transistors have been subjected to the same NBTI stress.

MINIMOSNT [22]. Both our experimental data as well as our theoretical analysis clearly demonstrate for the first time that the *energetical favorable alignment of the defect band to the SiGe layer caused by the Si cap layer* is indeed responsible for the superior reliability of SiGe devices.

II. EXPERIMENTAL DETAILS

To study the impact of NBTI on SiGe p-channel transistors we focus on structures with two different Si cap thicknesses of $d_{\mathrm{SiCap}} = 0.65\,\mathrm{nm}$ and $d_{\mathrm{SiCap}} = 2\,\mathrm{nm}$ between the HfO_2/SiO_2 gate stack and the SiGe layer [9]. First we investigate nanoscale pMOSFETs with a gate width of $W = 90\,\mathrm{nm}$ and a gate length of $L = 35\,\mathrm{nm}$. We note that all three device technologies have different threshold voltages. The reference Si devices have the most negative threshold voltage $V_{\mathrm{th}} = -217\,\mathrm{mV}$ and the devices with the thin Si Cap the most positive $V_{\mathrm{th}} = 245\,\mathrm{mV}$ (the devices with the thick Si cap layer have $V_{\mathrm{th}} = 24\,\mathrm{mV}$). To ensure comparable oxide fields during recovery, the recovery gate bias is determined individually for each device in such a way that all devices see the same overdrive voltage during recovery. This is achieved by setting the recovery bias to the gate voltage which causes a drain-source current of $I_{\mathrm{DS}} = -1\,\mu\mathrm{A}$ at $V_{\mathrm{DS}} = -100\,\mathrm{mV}$. Typical recovery traces of all three technologies recorded after NBTI stress with $V_{\mathrm{G}}^{\mathrm{s}} = -2.4\,\mathrm{V}$ are shown in Figure 1. As can be seen, for nanoscale devices the emission events in the recovery traces are visible as discrete steps, i.e. the recovery proceeds in discrete emission events. Each particular step corresponds to a charge exchange with either the substrate or the MG. For each technology an average contribution of a single trap to the total threshold voltage shift η can be extracted. The analysis of the recovery traces reveals that with increasing Si cap layer thickness *the number of active traps increases*, as can be seen when the recovery traces for the device with the thin Si cap layer shown in Figure 1 (left) and the traces from the device with the thick Si cap layer Figure 1 (middle) are compared. The number of defects present for a certain technology is given by the number of traps N_{T}. Among the studied device variants the reference devices without a SiGe channel show the largest number of active traps visible, see Figure 1 (right). From this

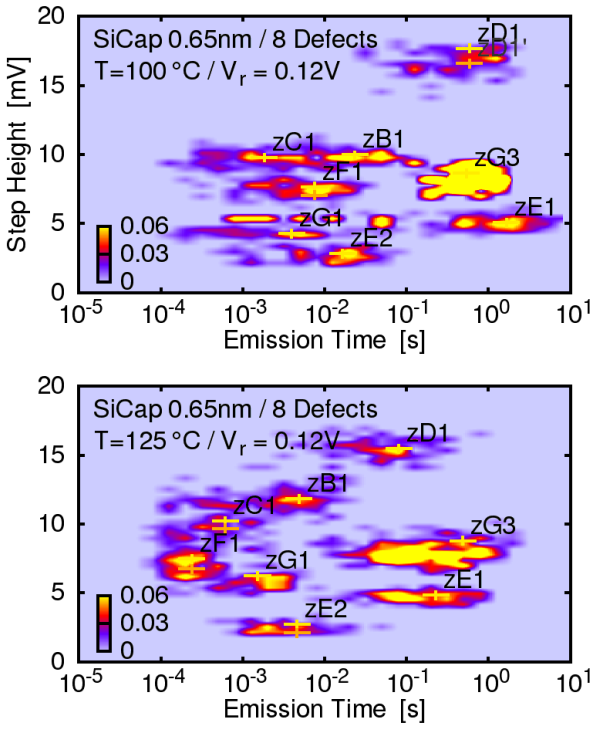

Fig. 2: Employing SiGe pMOSFETs with the thinnest SiCap layer we identified 8 defects at $T = 100°$ (**top**) and $T = 125°$ (**bottom**). The step heights of the defects are found widely distributed from $\Delta V_{\mathrm{th}} \approx 3\,\mathrm{mV}$ up to $\Delta V_{\mathrm{th}} \approx 17\,\mathrm{mV}$. In order to keep the experimental effort for the TDDS within reasonable limits, only fast traps with $\tau_{\mathrm{e}} < 1\,\mathrm{s}$ are studied here. In line with previous single-trap studies of BTI in SiON [10, 11, 13] and high-k devices [16] the defects move towards lower emission times at higher temperatures due to the thermally activated nature of charge trapping.

observation it follows that even with a thick Si cap layer the use of a SiGe channel results in a considerable reliability boost with respect to NBTI. A particularly interesting observation is that although the largest overdrive voltage during stress was applied to the devices with the thinnest Si cap layer (because they have the smallest V_{th}), their absolute ΔV_{th} is still the smallest compared to the other pMOSFETs. Furthermore, a considerable stress bias has to be used to achieve a measurable degradation of the SiGe pMOSFETs.

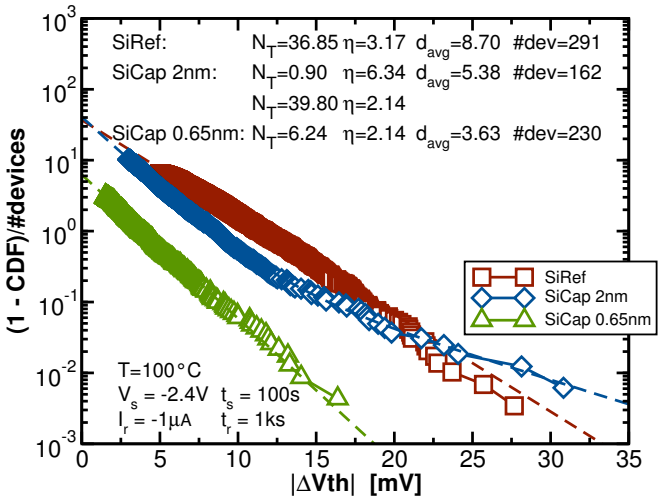

Fig. 3: The recovery traces of more than 600 devices have been analyzed to determine the complementary CDF. A unimodal CCDF is obtained for the devices with the thinnest Si cap layer and for the reference devices. In contrast, the devices with the thick Si cap layer show bimodally distributed step heights. Quite remarkably, the CCDFs obtained from the SiGe pMOSFETs have similar values for the average contribution of a single trap η for step heights smaller than approximately $12\,\mathrm{mV}$. It has to be noted that when the CCDF is normalized to the number of devices the number of traps per single device is directly visible at the ordinate at $|\Delta V_{\mathrm{th}}| = 0\,\mathrm{V}$. As can be seen, the devices with the thin Si cap layer have the smallest N_{T} compared to the other two technologis.

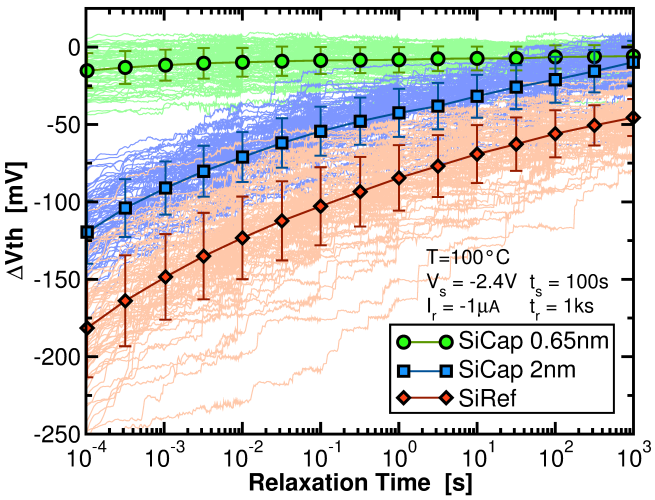

Fig. 4: The average threshold voltage shift ΔV_{th} of the traces used to calculate the CCDF from Figure 3. The largest ΔV_{th} shift is observed for the reference Si transistor. A smaller sensitivity with respect to NBTI stress is found for the devices with $d_{\mathrm{SiCap}} = 2\,\mathrm{nm}$. The transistors with $d_{\mathrm{SiCap}} = 0.65\,\mathrm{nm}$ show the smallest ΔV_{th} shift when subjected to NBTI stress.

Using the TDDS we identified 19 single defects among all our DUTs. To study a certain trap, 100 recovery traces are recorded at the same stress/recovery times and biases and at the same device temperature. Afterwards, the traces are thoroughly analyzed [10, 12, 18, 20] and the discrete steps and emission times are collected in the emission time vs. step height plane (τ_{e}, d), called spectral map. Withing a spectral map the single-traps form clusters, which are the fingerprints of each individual defect. The eight traps we analyzed in detail from the devices with the thin Si cap layer show step heights from $d \approx 3\,\mathrm{mV}$ up to $d \approx 17\,\mathrm{mV}$, see Figure 2. As can be seen from the spectral maps, the single-traps move towards lower emission times with increasing device temperature, an observation which is in agreement with single-trap studies on SiON and high-k MOSFETs [10, 13, 16, 20].

Contrary to their nanoscale counterparts, the large area pMOSFETs ($W = L = 1\,\mu\mathrm{m}$) show a continuous recovery behavior. The average recovery is a result of the contribution of a large number of defects to the net device degradation. Using an eMSM scheme, the impact of different stress times and stress biases has been studied. It has to be noted that for an increasing device area $A = W \times L$ a smaller average contribution of a single charge $\eta_{\mathrm{um}} = \eta_{\mathrm{nm}}/A$ is obtained. In contrast, the trap density increases together with increasing device area $N_{\mathrm{T,um}} = A \times N_{\mathrm{T,nm}}$.

III. Single Defects

The CCDFs in Figure 3 shows unimodally distributed step heights for the reference Si device and the devices with $d_{\mathrm{SiCap}} = 0.65\,\mathrm{nm}$. Quite remarkably, a significant smaller value for the average contribution of a single trap η is observed for devices with the thin Si cap layer compared to the reference pMOSFETs, with $\eta_{0.65\mathrm{nm}} = 2.14 < \eta_{\mathrm{ref}} = 3.14$. On average, the smaller the observed step height, the farther away the trap is located from the channel. In the case of the SiGe pMOSFETs it has to be considered that the conducting channel is located in the SiGe layer which is farther away from the IL due to the additional cap layer with thickness $d_{\mathrm{SiCap}} = 0.65\,\mathrm{nm}$. We thus conclude that the small value for $\eta_{0.65\mathrm{nm}}$ is a consequence of charge trapping between the gate stack and the conducting channel which is dominantly located inside the SiGe layer. This claim is confirmed by our quantum-mechanical simulations. In contrast to the previously mentioned CCDFs, the step heights of the devices with a Si cap of $d_{\mathrm{SiCap}} = 2\,\mathrm{nm}$ appear bimodally distributed. This suggests the presence of *two conducting channels* with the first one located at the SiO_2/SiCap interface and the second one in the SiGe layer. This assumption is supported by the observation that the first part of the bimodal CCDF shows the same value for the average contribution of a single trap η as obtained for the unimodal CCDF for the devices with the thin Si cap layer. Therefore, we link the low η bulk of the bimodal CCDF to traps interacting with the channel in the SiGe. The high η tail of the CCDF is a superposition of step heights from traps interacting with the channel at the SiO_2/SiCap interface and with the channel in the SiGe. When thinning the SiCap layer, the current flow is more dominantly located in the SiGe and thus the bimodal CCDF turns into a unimodal one. The

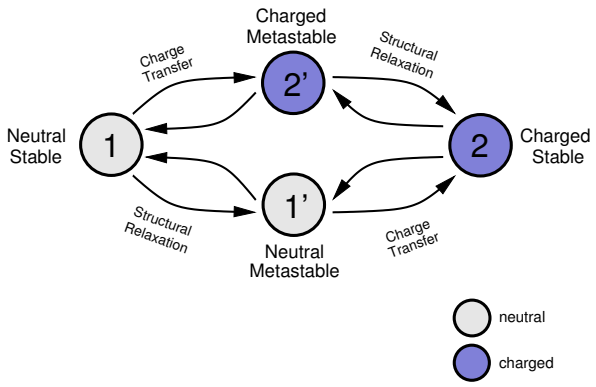

Fig. 5: The four-state NMP model is used to describe the response of the capture and emission times of single defects to varying biases and temperatures. In general, the model considers two stable states 1 (neutral) and 2 (charged) and two meta-stable states $1'$ and $2'$. These states are required for an accurate description of the bias-dependent and bias-indenpendent capture and emission times as well as other features [10]

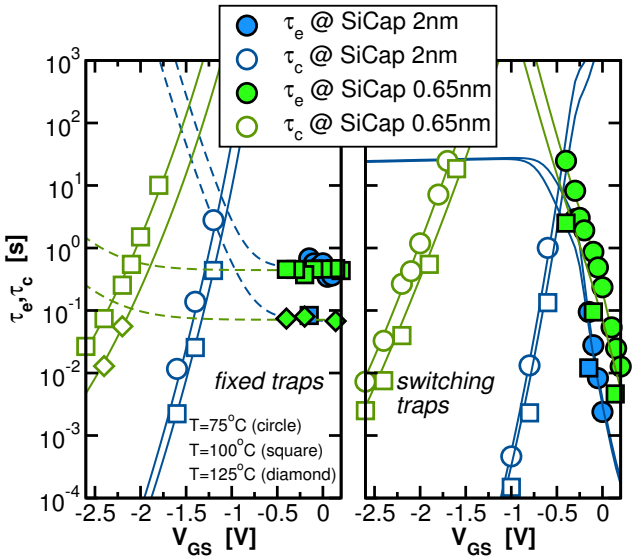

Fig. 6: The capture and emission times of single-traps characterized from our SiGe pMOSFETs plotted versus the stress/recovery biases at different device temperatures. As can be seen, *fixed hole traps* (**left**) with bias independent emission times and *switching traps* (**right**) with their typical bias dependent emission time behavior are found in all device variants. All the observed capture and emission time characteristics and their temperature dependence are well reproduced by our simulations using the four-state NMP model (lines).

extracted number of traps per device N_{T} is in agreement with the recovery traces shown in Figure 1. As can be seen, the devices with the thin Si cap layer have a smaller number of active traps $N_{\mathrm{T,0.65nm}} = 6.24$. Significantly more pronounced charge trapping is obtained for the two other technologies, resulting in a larger number of traps per device.

The average recovery traces from Figure 4 are calculated from the traces recorded to create the CCDF. As can be seen, the reference devices show the largest threshold voltage shift whereas the devices with the thin Si cap layer have the smallest response to NBTI stress. It has to be noted that the threshold voltage shift remaining at the end of the recovery traces ($t_{\mathrm{r}} = 1\,\mathrm{ks}$) strongly depends on the device technology and thus on N_{T}. The larger N_{T}, the larger the remaining threshold voltage shift. A negligible ΔV_{th} remains at the end of the traces for the thin Si cap device a noticeable value for ΔV_{th} is found for the reference devices after $t_{\mathrm{r}} = 1\,\mathrm{ks}$.

IV. Modeling and Simulation

To properly capture the device electrostatics and the carrier concentrations inside the SiGe channel, we calibrate our Schrödinger Poisson solver VSP [23] to experimental $C(V)$ characteristics of all three different device structures [24]. With the geometrical dimensions and dopings obtained from the quantum-mechanical simulations, our device simulator MinimosNT [22] is used to reproduce the corresponding $I_{\mathrm{D}}(V_{\mathrm{G}})$ characteristics. Then the hole capture and emission transition rates are calculated using our four-state NMP model (NMP) [18].

Initially, the NMP model was developed around the oxygen vacancy which is the most prominent defect in silica. Recently, considerably better agreement between DFT and experiment was obtained for the hydroxyl E' center, a variant of this defect [19]. The model uses metastable states to cover the *switching traps* with bias-dependent emission times (via state 1') and the *fixed traps* bias-independent emission times (via state 2'), see Figure 5. To properly reproduce the trapping behavior of our SiGe pMOSFETs, charging and discharging interactions with the channel at the SiO_2/SiCap interface and with the SiGe channel have to be considered.

Among our 19 studied single-traps we found fixed oxide traps and switching oxide traps, both shown in Figure 6. As can be seen, the fixed and switching trap capture/emission time characteristics and their temperature dependence is well explained by our four-state NMP model.

V. Results and Discussion

In addition to nanoscale SiGe pMOSFETs we also characterized the recovery of large area DUTs with $W = L = 1\,\mu\mathrm{m}$. The continuous recovery of these devices reflect the average contribution of a large number of traps with widely distributed capture/emission times and different step heights. Based on the NMP model parameters from the presented single trap investigations, an NMP trap distribution is calculated and utilized to reproduce the recovery. Consistently with our single-trap investigations, the recovery behavior of our large area devices of all three different technologies recorded after NBTI stress with different stress times and stress voltages can be reproduced using the four-state NMP model. Quite remarkably, this was achieved with *the same set of trap parameters* for the recoverable component. As a consequence we interpret the difference in the trapping kinetics and the number of electrically active traps as a consequence of the different energetic alignment of the gate stack with the active channel. The band-diagram from Figure 7 depicted for stress

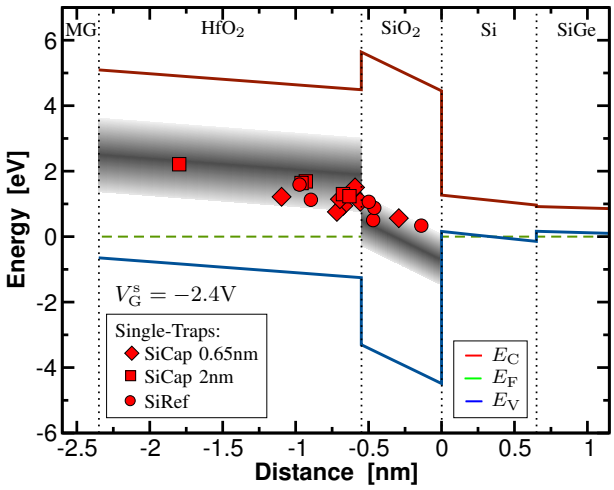

Fig. 7: The band-diagram under stress bias conditions shows the traps identified in the nanoscale devices marked with symbols. The trap bands in the HK and the IL show the energetical distribution of the traps used to to explain the recovery of *all the large-area* devices. Furthermore, this has been achived with just one paramterset.

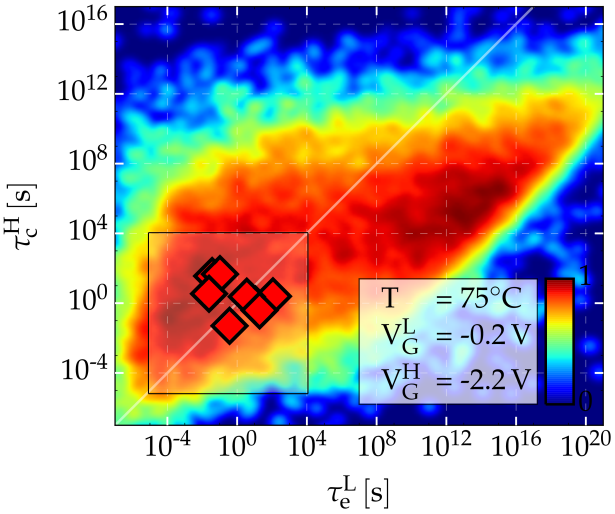

Fig. 8: The CET map is obtained from our simulations and shows the capture/emission time distribution from the defect ensemble from Figure 7 used to reproduce the recovery behavior of the large area devices with the thin Si cap layer. For the capture times the values are calculated at gate stress bias V_G^H (denoted with superscript '^{H}') and the emissions times are extracted at recovery gate bias V_G^L (denoted with superscript '^{L}'). The datapoints are extracted from our single-trap investigation lie well inside the distribution. Also visible is the measurement window with $\tau_e, \tau_c \in [10\,\mu s, 10\,ks]$ which marks the area of capture/emission times which can be accessed by eMSM measurements.

bias conditions shows the trap energy band used to explain the recovery of the large area transistors together with the trap depth and energetic position of the 19 identified individual traps. Performing detailed TCAD simulations we have observed that for large-area devices the recovery behavior is not very sensitive to the energetical position of the trap band in the HK. So the recoverable component is primilary dominated by traps present in the IL. Nonetheless, the mean value of the trap energy band for the HK and the IL used in our simulations are fully consistent with investigations of other groups [25].

As stated above, the recovery of the large area devices can be reproduced for all three different technologies by using the same set of NMP model parameters. From this parameter set we have calculated the capture emission time (CET) map for the devices with the thin Si cap layer, see Figure 8. In addition, the capture and emission times obtained from the eight single traps are also marked in the CET map. As can be seen, the single traps observed have capture/emission times lying well inside the simulated CET distribution.

Finally, the device lifetimes of the SiGe and reference Si devices are extrapolated. Using our calibrated model the dependence of the device lifetimes on the stress voltage is calculated, see Figure 9. *As expected, the SiGe devices with the thinnest Si cap provide a superior lifetime, easily outperforming the Si reference device.*

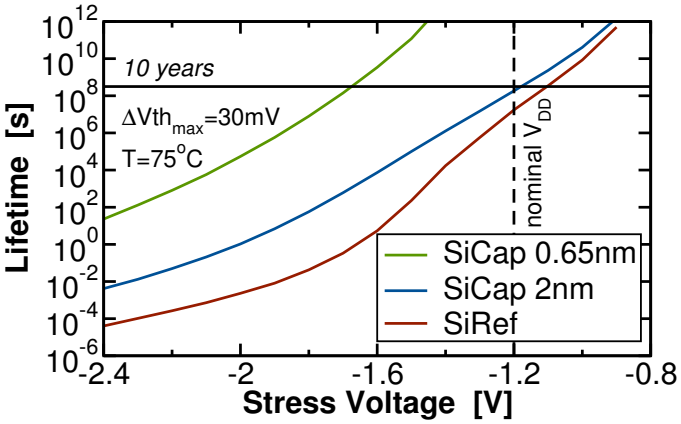

Fig. 9: Based on the unified model the lifetime of all three technologies can be estimated and is shown against the applied gate bias. At the nominal operating voltage of $V_{DD} = -1.2\,V$ a lifetime of more than 10 years is easily achieved for the SiGe devices.

VI. Conclusions

In a detailed study we have compared NBTI in nanoscale and large-area SiGe pMOS transistors. We have characterized 19 single defects and found the trap levels and positions to be independent of the device structure. This implies that the gate stacks are similar in all technologies and that the reliability benefits must be primarily a result of the combination of channel material and gate stack. By comparing the single-defect data with the average response of a large ensemble of defects, both experimentally as well as in TCAD simulations we could therefore demonstrate that the superior lifetime of SiGe devices with a thin Si cap layer is indeed due to the favorable energetic alignment of the defect band in the oxide with the channel.

VII. Acknowledgement

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