Stress Considerations for System-on-Chip Gas Sensor Integration in CMOS Technology

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***Abstract*—For several decades, researchers have aspired to combine all of the necessary components for a gas sensor with microelectronic circuits in order to create an integrated smart gas sensor device. However, these devices will only be embraced by industry and consumers if their cost of production is reduced to about $1 per device. The drive for affordable processing, integrable in complementary metal-oxide semiconductor technology, has lead to the implementation of novel techniques for the deposition of the sensing metal oxide layer and the use of 3D integration with through-silicon vias (TSVs). This paper analyzes, by means of modeling and simulation, the stress generation due to this integration, including the effects of TSV etching and metal-oxide deposition on the stress development in the devices' conducting layers and in the surrounding silicon. Two types of TSVs are investigated: a filled copper TSV and one with an open cavity and tungsten-lined sidewalls. The influence of sidewall scallops, present as a result of the deep reactive ion etching process, on the build-up of stress in the region is also analyzed. The thermal stress resulting from the spray pyrolysis deposition of the metal-oxide sensing layer, performed at 400 °C, is investigated along with the intrinsic stress which builds up during metal growth described with the Volmer-Weber model.**

***Index Terms*—Smart gas sensors, 3D integration, Volmer-Weber model, thermo-mechanical stress, through silicon vias, tin oxide (SnO_2).**

I. Introduction

THE AGGRESSIVE scaling of devices with "more Moore" integration is expected to reach a limit at the 6nm node due to physical constraints as well as increased process equipment and factory costs [1]. Research and development along the "more Moore" path has taken the front stage in the semiconductor industry for many decades. More recently, however, an ongoing demand has been for increasing the functionality of end-user products, which requires ever more complex interconnect structures. The development of integrated devices such as metal oxide gas sensors, stacked using three-dimensional (3D) integration, are examples of "more-than-Moore" development, an attempt to increase the functionality on single chips with applications beyond memory and logic [2].

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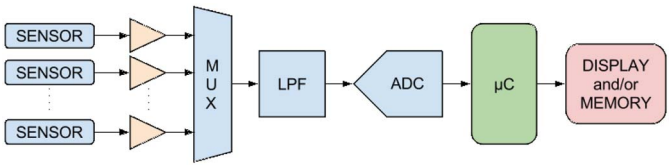


Fig. 1. Sensor array with interface electronics blocks.

A. Integrated Gas Sensor as a System-on-Chip

Various metal oxide gas sensing devices which rely on changes of their electrical conductance in the presence of a desired gas, have been developed over the last two decades [3]–[5]. The potential integration of intelligent gas sensors in smart phones and wrist watches will revolutionize the way in which pollutants and harmful chemicals are detected in our environment. However, before this can be achieved several challenges for sensor fabrication and 3D integration must be overcome:

- Until recently, available gas sensors relied on a bulky architecture whose manufacture was not compatible with that of a conventional CMOS process sequence, which is essential in order to combine the sensor with MEMS and CMOS microelectronics.
- Thin metal-oxide layers act as gas sensors when heated to temperatures between 300°C and 550°C, meaning that a micro-hotplate must accompany each sensor. The integration of the hotplate and sensor to the required analog and digital circuitry as shown in Fig. 1 is essential.
- The usability and attractiveness-to-market of a battery-operated device is strongly affected by its speed, power consumption, and size: all three of these factors can be improved by 3D integration. Through-silicon vias (TSVs) are used to connect the various parts of the sensor circuit while avoiding the signal loss and delay associated with long metal routing. In some circuits, TSVs are also essential in order to connect the signals from the sensor output to the printed circuit board (PCB) [6]. Fig. 2 shows the potential integrated gas sensor as a system-on-chip, where the TSVs are used to carry the signal to the next parts of the circuit, such as the amplifier shown in Fig. 1.

As shown in Fig. 1, in order to create an intelligent gas sensor, which is capable of detecting several different hazardous gases in the environment, multiple sensor circuits are required. The analog signal from these sensors is passed through an

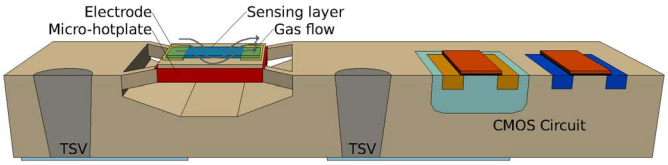


Fig. 2. Setup of the integrated gas sensor as a system-on-chip.

amplifier to a multiplexer. The output from the multiplexer is sent through a low pass filter (LPF) and an analog to digital converter (ADC) before analysis with a microcontroller (μC) and eventual signal display or storage [7]. Although the major part of the electronics consists of analog and digital CMOS circuitry, the most complex component, for integration and manufacturing, is the sensor itself. In Fig. 2 a view of the integrated gas sensor as a system-on-chip is shown.

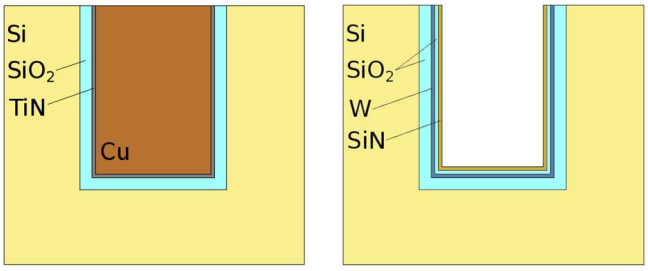
In the sensor circuit there are two critical components which require a close inspection with regard to the processing technique and how it influences the device reliability and stress build-up in the overall device. These components are the metal-oxide sensing layer and the TSV, which will be discussed in further details in the following sections.

Discoveries in the application of metal oxides as gas sensing materials are at the forefront for enabling significant progress in moving away from bulky sensor architectures [7]–[11]. The miniaturization of electronic devices has proven to be essential, while the gas sensor field is still lagging behind the overall progress of CMOS and MEMS devices. Two materials have been substantiated to exhibit all the properties required for a good gas sensing performance, namely zinc oxide (ZnO) [12]–[15] and tin oxide (SnO_2) [16]–[18], while others such as indium tin oxide (ITO), In_2O_3, CdO, $ZnSnO_4$, NiO, etc. have also been widely studied [14]. In our study, a tin oxide sensing device is used in order to examine the sensing layer deposition and stress build-up due to the employed deposition process.

B. 3-D Integration Using TSVs

This study concerns itself with the analysis of the processing, stress build-up, and reliability of several components, which are essential to the fabrication of an intelligent metal oxide gas sensor with a three-dimensional structure, similar to the image sensor integration presented by Kurino *et al.* [19]. The device components examined are a copper-filled TSV, a tungsten-lined open TSV, and a tin oxide thin film, used as the sensing layer, capable of detecting CO, CH_4, H_2, and H_2S.

Several recent works concern themselves with the reliability and performance of copper filled TSVs [20] as well as open TSVs with tungsten lining [52], [53]. The primary difference between the two TSV designs is that the filled version has its entire etched cavity filled with a conducting metal, while the open TSV is lined with a thin layer of a conductive metal. Another difference is in their geometries: the filled TSV usually has a diameter from under 1μm to 20μm, while the open alternative is much larger, with a diameter ranging between 50μm and 100μm [1]. However, open TSVs have much smaller aspect ratios of up to 1:5, while filled TSVs are etched with ratios of up to 1:20. Copper is the most frequent metal option for TSV design, especially in the filled case (Fig. 3(a)), because of its high conductivity; but the copper TSVs have a poor reliability performance due to thermal stress since the coefficient of thermal expansion (CTE) for copper is much higher than that of silicon or SiO_2. In addition, copper is more prone to electromigration failure, when compared to the tungsten alternative, making tungsten a more attractive option when dealing with high-power devices [21], [22].



(a) Copper filled TSV (b) Open TSV with tungsten

Fig. 3. Two types of TSV geometries – (a) Copper filled and (b) Open structure with a tungsten lining.

The use of an open TSV structure, shown in Fig. 3(b), mitigates some of these effects, because the overall amount of material is reduced and the structure offers room for the metal to expand towards the middle vertical axis of the via [23]. Additionally, tungsten has a CTE which is much closer to that of silicon, but because of the increased size, open TSVs are only implemented where filled TSVs are undesirable. The added benefits of open TSVs come with a caveat: the tungsten-lined open TSVs have a higher parasitic resistance and capacitance than their filled copper alternatives, while the open structures also require much more surface area on the wafer [1]. Both TSV structures are useful, depending on their application. Filled copper structures are useful when signal speed is essential, such as for digital circuitry, while the tungsten structures should be used for the transport of the sensor signals, which gives improved reliability at the cost of operating signal frequency.

In this work the stress distribution through two sample TSVs is investigated: a copper-filled TSV with a diameter of 5μm and a 1:10 aspect ratio and an open tungsten-lined TSV with a diameter of 100μm and a 1:2 aspect ratio. A 200nm thick tungsten layer is deposited along the open TSV sidewalls as the main conducting metal. Due to the reliability advantages of the open TSV geometry and its use in the transport of the sensor signal itself, more attention will be given to it in the discussions.

II. Fabrication Techniques

The fabrication of smart sensors and their 3D integration with other circuit elements has been enabled with the advent of novel fabrication techniques. In this section the critical processing steps implemented to fabricate TSVs and to deposit the metal oxide sensing layer are described.

A. TSV Fabrication

TSV-based three-dimensional integration enables the fabrication of systems connecting various technologies, dense device packing, lower power consumption, and reduced resistive-capacitive (RC) delay [24]. A sequence of several sensitive processing steps is required in order to generate a TSV with a desired size and aspect ratio. In addition to the deposition of insulation and conducting materials, a method to etch vertical wells through a silicon wafer is required. The two most common methods to etch the silicon layer for TSV implementation are deep reactive ion etching (DRIE), also known as the Bosch process, and plasma etching [1]. Each silicon etching method has its own peculiarities and reliability concerns. Problems specific to the Bosch process are a rough, scalloped TSV sidewall, notch formation at the TSV bottom, and potential step coverage issues relating to depositing layers on a scalloped wall [25]. The etching of deep trenches using an ion-enhanced plasma, such as SF_6/O_2, results in significant sidewall tapering, making the formation of deep vertical trenches a challenge [26].

B. Deep Reactive Ion Etching of Silicon Substrates

In order to analyze the TSV profiles, an in-house process simulator is used. The simulator is implemented using a level set (LS) framework and is capable of simulating a sequence of processing steps, including etching and deposition [27]. The Bosch process is used to etch deep trenches in silicon using multiple cycles of polymer deposition and polymer/silicon etching.

The first step of a Bosch process cycle involves the deposition of a thin chemically inert polymer layer, usually in a C_xF_x gas environment. The subsequent etching step is performed in an ion-enhanced plasma environment, usually using SF_6 gas. The polymer protects the structure from the chemical etching, while the ions attack the polymer layer at the trench bottom. This results in an exposure of the substrate at the bottom, where chemical etching can then proceed, while the sidewalls are still protected. The first few steps of a DRIE process are shown in Fig. 4, where the resulting sidewall scallops are evident. This process is used to etch deep trenches in silicon, such as those required for high aspect ratio and deep trenches.

C. Metal Oxide Layer Deposition

Tin oxide is an essential material in gas sensing devices, since it is the tin oxide's changing conductivity in the presence of certain gases, which is the main component of the sensor's functionality. In this section the deposition process of this material is examined. Currently, the deposition of metal oxide materials is performed using several techniques such as chemical vapor deposition [28], sputtering [29], pulsed-laser deposition [30], sol-gel process [31], and spray pyrolysis [16]. Spray pyrolysis has recently gained traction due to its cost-effectiveness and integrability into a standard CMOS processing sequence [32].

During spray pyrolysis deposition, a gas pressure nozzle is used to atomize a $SnCl_4{+}H_2O$ solution. The nozzle generates very small droplets which are directed towards the substrate, where SnO_2 is deposited on top of a heated wafer. Using this method, substrates with complex geometries can be coated using CMOS-compatible temperatures at and below 400°C. The nozzle is placed about 30cm away from the substrate, ensuring that the droplets have no horizontal velocity when reaching the vicinity of the substrate. The long distance between nozzle and wafer also ensures that all large, liquid droplets will be eliminated prior to reaching the substrate, ensuring a uniformity in the droplet size distribution and thereby a uniformity in the deposited film [32].

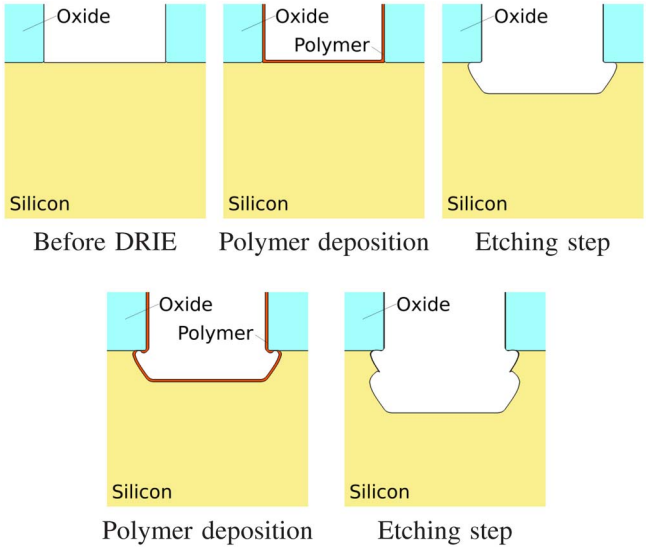


Fig. 4. Process of deep reactive ion etching of silicon using oxide as a mask. The process is represented by a sequence of repeating steps, which include a polymer deposition step and a combined physical and chemical etching step. The polymer serves to protect the trench sidewalls from lateral etching during the chemical etch, resulting in highly vertical walls.

The steps which describe the processes taking place during spray pyrolysis deposition are [33]:

1) Atomization of the precursor solution,
2) Aerosol transport of the droplet, and
3) Decomposition of the precursor to initiate film growth.

III. Simulation Environment

This work concerns itself with an analysis of TSVs and metal oxide layers for gas sensor applications through a combination of simulation tools and methodologies. In this section the tools used are described and their features and implementation are outlined. Three types of simulations must be performed for a complete analysis are further outlined in the sections which follow:

- Process simulations,
- Intrinsic stress simulations, and
- Thermo-mechanical stress simulations.

A. TSV Process Simulations

To perform the process simulations, necessary for the analysis of TSV fabrication, as well as metal oxide deposition, an in-house process simulator ViennaTS [34] is employed. The simulator is implemented using the LS framework and it is

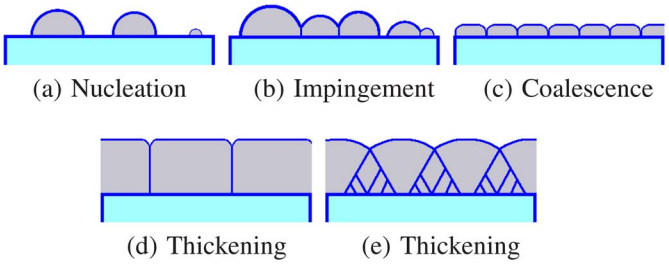


Fig. 5. Steps during film formation using the Volmer-Weber growth mode.

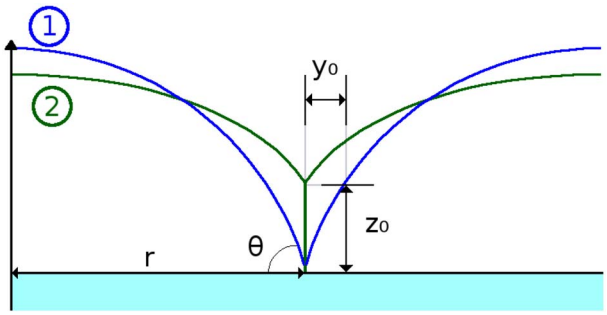


Fig. 6. From position 1 to position 2, two islands impinge, resulting in a grain boundary with height z_0.

capable of simulating a sequence of processing steps, including etching and deposition [27]. The LS method describes a movable surface S as the zero LS of a continuous function, defined on the entire simulation domain,

$$S(t) = \{\vec{x} : \Phi(\vec{x}, t) = 0\}. \tag{1}$$

The implicitly defined surface S describes a surface evolution, driven by a scalar velocity $V(x)$, using the LS equation

$$\frac{\partial \Phi}{\partial t} + V(\vec{x})\|\nabla \Phi\| = 0, \tag{2}$$

where $\Phi = 0$ denotes the location of the surface S on the entire simulation domain. In order to find the velocities $V(\vec{x})$ the relevant physical etching or deposition model is applied and the velocities along the entire surface are calculated. A detailed description of ViennaTS can be found in [34] and [35].

B. Intrinsic Stress Simulations

During the deposition of metals on oxidized silicon surfaces, the metal film is deposited in the form of islands which coalesce and then grow to form larger grains, a process known as Volmer-Weber growth mode. An enhanced version of the code presented by Seel in [36] has been used in order to compute the intrinsic stress in a flat rectangular section of the wafer surface. The simulation calculates the compressive stress during island growth and the tensile stress during island impingement, as described in further details in this section. The intrinsic stress simulator computes the biaxial stress which is identical to the von Mises stress, when dealing with the given rotationally-symmetrical structures. The intrinsic stress generated during thin film growth develops during deposition and can go through stages of compressive and tensile stresses depending on the film properties. Fig. 5 summarizes the main steps involved in the film growth, as characterized in [36].

The initial stage is the island nucleation or the formation of small islands on the surface. As the islands grow, they impinge on each other, which generates tensile stress in the islands. When all the islands on the surface are connected, a film is said to have coalesced. The next stage of growth is the film thickening, which can be either columnar or polycrystalline. The columnar thickening mode shown in Fig. 5(d) refers to the growth of films which have a high adatom mobility or low melting temperatures, such as silver (Ag), copper (Cu), and aluminum (Al). The polycrystalline growth shown in Fig. 5(e) refers to the growth of films which have a low adatom mobility or high melting temperatures, such as tungsten (W), chromium (Cr), or tantalum (Ta) [36]. Before film coalescence, there are two main stress components which must be considered: the compressive stress which is generated due to the island nucleation and the tensile stress generated in the thin film due to island impingement.

During island formation and subsequent increase in island radius during deposition a compressive stress builds up in the island due to excess surface energy. The model which governs the build-up of compressive stress in relation to the grain growth is given in [36] as

$$\sigma_{compressive} = -\frac{2(\gamma_{gb} - 2\gamma_s)}{r} \cdot \frac{sin\theta}{(1 - cos\theta)(2 + cos\theta)}, \tag{3}$$

where γ_{gb} is the grain boundary energy, γ_s is the surface energy, r is the island radius, and θ is the contact angle between the island surface and the substrate. Upon island impingement a grain boundary is formed between two islands, which results in a part of the free surface of each island being eliminated and in a significant energy reduction. This process of *zipping* at the grain boundary to a specific height generates tensile stress in the grains. Fig. 6 shows the process of two islands impinging on each other and the formation of a grain boundary. When two islands approach each other and each attempts to increase its radius, a grain boundary forms. The generated tensile stress depends on the resulting geometry of that process, described in [36] as

$$\sigma_{tensile} = \frac{1}{2} \cdot \frac{E}{1 - r^2} \left(\frac{y_o}{r}\right)^{1.3892}, \tag{4}$$

where E is the Young's modulus, and r and y_0 are geometric parameters depicted in Fig. 6.

The tensile stress described with (4) can relax through the transport of matter to the strained region within the grain boundary. An equation which governs this mechanism is given in [36] and more details regarding the relaxation process can be found there

$$\dot{\sigma} = -\frac{C_o}{t} \cdot \sigma_{tensile} \cdot e^{-Q/kT}, \tag{5}$$

where C_o is a material-dependent parameter, h is the film thickness, Q is the activation energy for the material diffusion, k is the Boltzmann constant, and T is temperature. For simplicity, the relaxation phenomena will, for the most part, be neglected here. The material properties required for the simulation of the generated intrinsic stress for metals of interest are

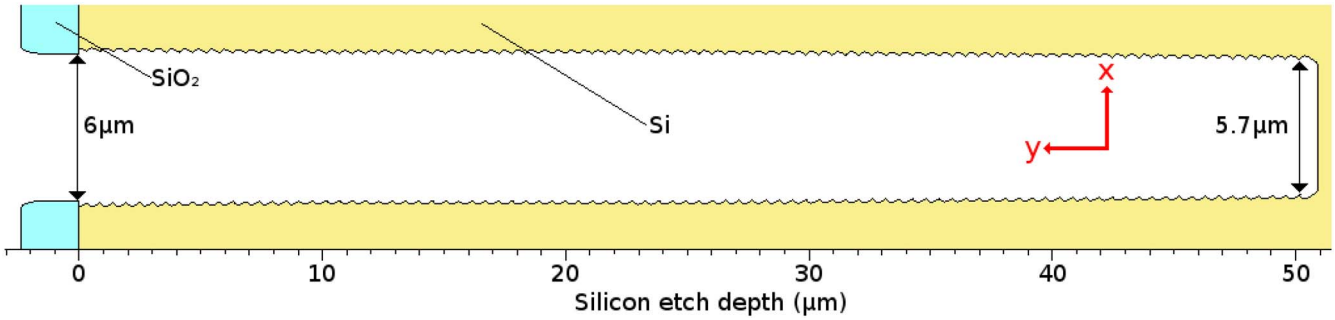


Fig. 7. Cross-section of the etched silicon required for a copper-filled TSV is shown, with sidewall roughness evident.

TABLE I
MATERIAL PROPERTIES OF AL, CU, AND W AT ROOM TEMPERATURE, REQUIRED FOR THE SIMULATION OF STRESS EVOLUTION DURING VOLMER-WEBER GROWTH AND GRAIN COALESCENCE. THE VALUES HAVE BEEN FOUND IN [36]–[40]

	Al	Cu	W	SnO_2
Young's Modulus E (GPa)	87.3	127.7	400	253
Poisson Ratio v	0.354	0.340	0.290	0.293
Surface Energy γ_s (J/m^2)	1.02	2.23	1.85	1.20
Grain Boundary Energy γ_{tb} (J/m^2)	0.324	0.715	0.900	0.710
Melting Temperature T_{melt} (K)	1358	933	3695	1900

TABLE II
COEFFICIENTS OF THERMAL EXPANSION FOR THE MATERIALS USED IN THIS STUDY

Material	Copper	Tungsten	TiN	SiO_2
CTE (10^{-6}/K)	16.5	4.5	9.35	0.5

Silicon	Si_3N_4	SnO_2	Aluminum
2.6	2.3	4.0	23

given in Table I. The material properties have been collected from a literature survey of [36]–[40].

C. Thermo-Mechanical Stress Simulations

In contrast to the calculation of the intrinsic stress, which is performed on a flat rectangular sample, thermo-mechanical simulations are performed directly on the desired geometry using the commercial finite element simulator Comsol Multiphysics [41]. The geometries, generated during the process simulation step are imported into the finite element tool, where they are meshed for further simulations. The source of stress is the thermal expansion of the materials used in the device, where the relationship between the thermal strain ϵ_{th} and temperature is given by

$$\epsilon_{th} = \alpha\big(T - T_{ref}\big), \tag{6}$$

where α is the CTE, T is the simulated temperature, and T_{ref} is the stress-free reference temperature. The stress-free temperature refers to the temperature at which the metal deposition takes place, meaning that only intrinsic stress is present in the metal, while the thermal stress is zero. A summary of CTEs for the relevant materials are given in Table II. Simulations are performed in order to calculate the stress in the structure after a cool-down to room temperature following a processing step at 400°C.

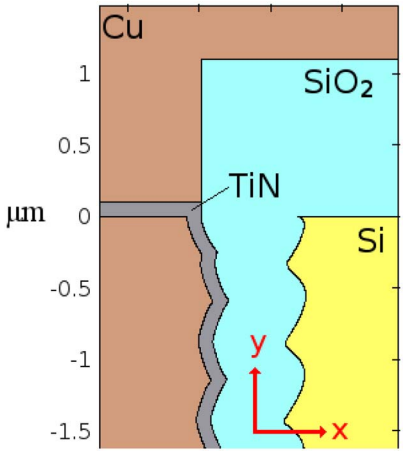


Fig. 8. Two-dimensional profile of the copper-filled TSV examined in this study. The materials at the top of the TSV are given.

IV. PROCESS SIMULATION

In this section the generation through process simulation of three structures is described: the copper-filed TSV, the tungsten-lined open TSV, and the metal oxide gas sensing layer. The generated structures will then be used in Section V and Section VI in order to determine the impact of fabrication on the devices' stress development.

A. Copper-Filled TSV

A copper-filled TSV is frequently used for 3D integration and chip package interaction. A TSV which is filled with a metal such as copper can be thinner with higher aspect ratios than its open counterpart [1]. However, the structure and the surrounding silicon can be exposed to high stresses when operating in a high-temperature environment or when a high current is required to flow through the structure. Problems such as copper pumping and barrier/liner integrity are issues which still need addressing. The copper-filled TSV is essential for applications where fast switching is needed such as for digital circuitry which does not need to operate under increased thermal stresses.

A sample copper-filled TSV with a diameter of 5μm and aspect ratio of 1:10 is shown in Fig. 7 and Fig. 8. The simulation parameters used to perform the etching step and the resulting scallop dimensions are given in Table III. The simulation for the deposition of oxide and TiN liner are performed

TABLE III
SIMULATION ETCH PARAMETERS—PROCESS TO GENERATE THE COPPER-FILLED TSV

	Rate	Etch ratio		Cycle time
Polymer deposition	10nm/sec	—	—	4sec
Silicon etch (isotropic)	40nm/sec	Si:mask Si:polymer	80:1 13:1	5.5sec
Silicon etch (directional)	24nm/sec	Si:mask Si:polymer	80:1 2:1	
Total number of deposition/etch cycles:				93
Resulting scallop height:				530nm
Resulting scallop width:				250nm

using isotropic rates and result in a 500nm thick oxide isolation layer and a 100nm thick TiN liner. The simulation of the electrochemical deposition of copper in the TSV trench goes beyond this study, but a previously published work ensures that this step can be performed without the formation of seam voids using a sputtered TiW/Cu seed layer [42].

As noted in Table III, the simulation requires 93 deposition/etch cycles in order to etch the required depth of 50μm. Each cycle results in a scallop along the TSV sidewall with a height of 530nm and a width of 250nm. In order to simulate the performance of the generated device and its thermal stress response, the geometry from Fig. 8 is meshed for analysis with the finite element tool Comsol Multiphysics [41].

B. Open TSV With Tungsten Lining

In order to reduce the stress accumulation in filled TSVs, a polymer barrier can be inserted between the via and silicon [23]. An alternative approach is the use of an unfilled via with a metal lining. The choice of metal to line the sidewalls is also an important design decision. Although copper is most common due to its good electrical properties, tungsten is studied here because of its low CTE and acceptable electrical properties. For an integrated gas sensor, such as the one depicted in Fig. 2, an open TSV with tungsten lining is more suited to carry the signal required to activate the micro-hotplate and the analog sensor signal. The thicknesses of the tungsten, liner oxide, and silicon nitride layers are 200nm, while the average thickness of the isolation oxide is about 500nm.

In Fig. 9 the two-dimensional profile of an open TSV with tungsten lining is shown and in Table IV, the processing parameters which were used to generate the structure are given. The resulting scallops along the TSV sidewall have a height of 2.2μm while their width is 500nm. Once again, in order to simulate the performance of the device depicted in Fig. 9 and its thermal stress response, the geometry is meshed for analysis with a finite element tool.

C. Tin Oxide Gas Sensing Layer

Experimental data from [43] show a linear dependence on spray time and a logarithmic dependence on wafer temperature for the growth rate of the deposited SnO_2 layer when the spray pyrolysis technique is implemented. A good agreement for the deposited SnO_2 thickness, in μm, is given by

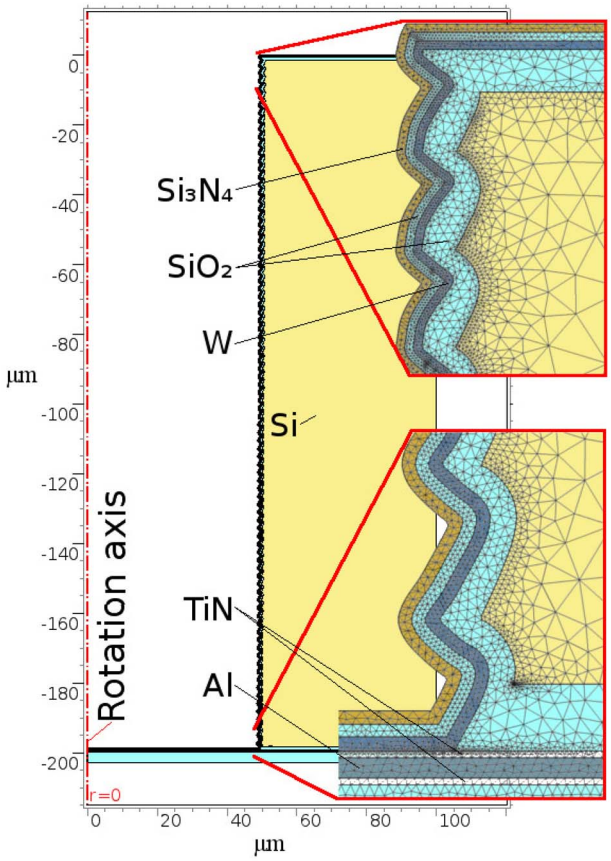


Fig. 9. TSV profile which clearly shows the scalloped nature of the structure sidewalls is given.

TABLE IV
SIMULATION ETCH PARAMETERS FOR THE DRIE PROCESS REQUIRED TO ETCH THE TUNGSTEN-LINED OPEN TSV

	Rate	Etch ratio		Cycle time
Polymer deposition	12nm/sec	—	—	3.5sec
Silicon etch (isotropic)	500nm/sec	Si:mask Si:polymer	80:1 100:1	5.5sec
Silicon etch (directional)	534nm/sec	Si:mask Si:polymer	80:1 100:1	
Total number of deposition/etch cycles:				91
Resulting scallop height:				2.2μm
Resulting scallop width:				500nm
Resulting TSV resistance:				374mΩ
Resulting TSV capacitance:				6.527pF
Resulting TSV inductance:				5.307pH

the Arrhenius expression

$$d_{SnO_2}(t,T) = A_1\, t\, e^{(-E/k_B T)}, \tag{7}$$

where $A_1 = 3.1\,\mu$m/sec, t is the time in seconds, T is the temperature in Kelvin, and E is $0.427eV$ and a sample simulation result is shown in Fig. 10. The growth model given in (7) relates the thickness of the deposited material to the applied time and temperature. However, this representation is only valid, when no complex geometries such as deep wells, trenches, and step structures are present. In order to model deposition on a deep well structure, a simulation which considers more than a single deposition rate is required. Since the droplets fully evaporate prior to depositing on the surface,

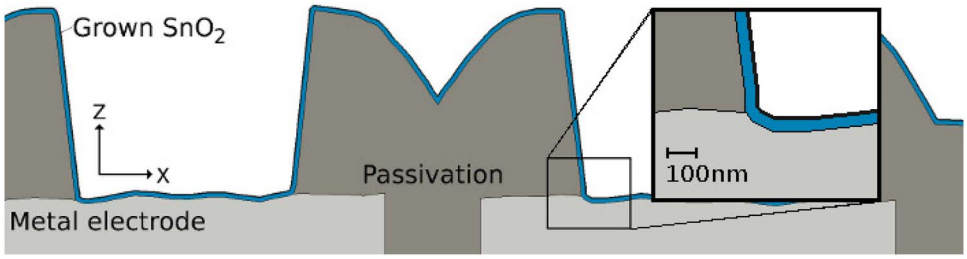


Fig. 10. Image showing the simulated deposited SnO_2 film as a results of spray pyrolysis deposition. The deposition is performed with the heated substrate at a temperature T=400°C for a time t=30s.

a non-linear simulation model analogous to chemical vapor deposition (CVD) is used. The details of the implemented model can be found in [43], while only a short descriptive summary of the implementation is given here.

The model implementation requires the combination of Monte Carlo methods within the LS framework. A single-particle species is considered during deposition. As the simulation is initiated, multiple particles are generated in the simulation space with an average direction perpendicular to and moving towards the wafer. For the spray pyrolysis deposition process it was found that a sticking coefficient of 0.01 gives the best fit to experimental data and was therefore used for the model. The motion of reflected or re-emitted particles is then tracked with their sticking probability reduced after each surface impact. The tracking of a single particle is deemed concluded, when its sticking probability reaches 0.1% of the original coefficient.

Using the given equation and presented model, a simulation was performed for 30sec at 400°C on the full geometry of a gas sensing electrode with the result shown in Fig. 10. The resulting film has an evenly distributed thickness of approximately 50nm, as expected from the measured thickness noted in experimental observations [43].

V. Intrinsic Stress Simulations

In this section the intrinsic stress build-up in relevant structures and materials is simulated. During metal and metal oxide deposition, the two main stress components which must be considered are intrinsic, as described in Section III-B and thermo-mechanical, as described in Section III-C. The total stress σ_{total} in the metal is then given by the sum of the two stress components.

$$\sigma_{total} = \sigma_{intrinsic} + \sigma_{thermal} \tag{8}$$

The stress which is found in the conducting metal of TSVs can give rise to cracking and delamination failure, while the stress in the surrounding silicon affects the electron and hole mobilities in the transistor devices which are placed in the TSVs' vicinity.

A. Intrinsic Stress in Thin Tungsten Films

Tungsten is a material with a low adatom mobility and therefore the stress build-up in a thin tungsten film will be tensile, meaning only equation (4) is of concern. The intrinsic stress build-up during tungsten deposition is shown in Fig. 11.

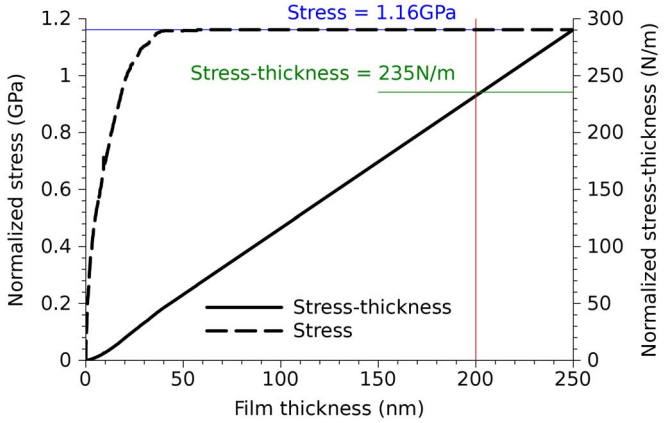


Fig. 11. Intrinsic stress build-up during tungsten deposition.

The stress-thickness ($\sigma \cdot h$) product is often called the "force/width" and is frequently used in measurements of stresses through thin films in order to highlight that the stress can have a through-the-thickness variation that cannot be determined solely by post-deposition curvature measurement [44]. The $\sigma \cdot h$ product is also a convenient way to observe stress in films before coalescence, where there is no uniform stress which can be attributed to the entire thickness of the deposited metal. From these results it is evident that after coalescence the average stress through the film remains static. Coalescence of the film occurs at a thickness of approximately 50nm, where the average stress reaches its peak of 1.16GPa.

B. Intrinsic Stress in the SnO_2 Layer

In order to estimate the intrinsic stress build-up in tin oxide thin films using (3), (4), and (5) the values for several material coefficients must be known. The average surface energy and grain boundary energy used in this study are $1.20 J/m^2$ and $0.71 J/m^2$, respectively [45]. There are various ranges of Young's modulus reported for SnO_2, from 150GPa [46] to 253GPa [47]. In this study the value 253GPa is used, together with a Poisson ratio of 0.293. This value tends to be better suited to very thin films, while lower Young's modulus values are usually reported for films with thicknesses in the micrometer range.

Another point of contention in SnO_2 films is whether the intrinsic stress is tensile or compressive, which is also a discussion on whether the film has low or high adatom mobility. The melting temperature of tin oxide at 1900K is higher than that

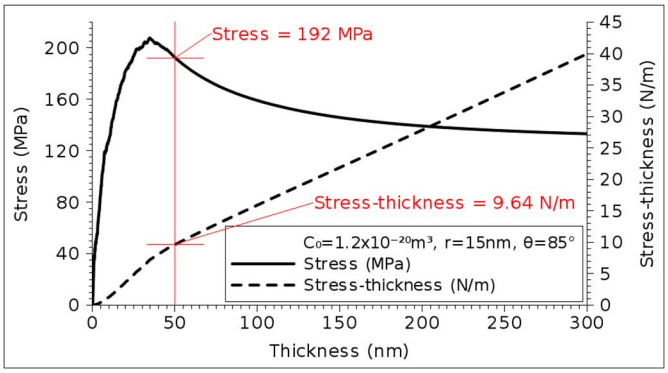


Fig. 12. Intrinsic tensile stress development in the SnO_2 thin film using (4) and (5).

of traditionally high-adatom mobility metals such as aluminum (1358K), copper (933K), and silver (1235K), but lower than of traditionally low-adatom mobility metals such as chromium (2180K), tungsten (3695K), and tantalum (3290K). In fact, it was previously reported in [48] that the intrinsic stress is related to the amount of oxygen content during deposition for sputtered films. A tensile stress of 200MPa is noted for undoped films, while an increasing oxygen content leads to a stress decrease to a compressive 200MPa. In this study, the tensile stress is examined and the amount of relaxation required to reach an intrinsic stress of 200MPa is observed. Intrinsic stress simulations, according to the procedure outlined in Section III-B, were performed for SnO_2, with the results shown in Fig. 12. A tensile stress is noted, while some relaxation occurs after coalescence, when the film thickness is about 45nm. At a thickness of 50nm, which is the desired thickness for the sensor application, a tensile stress of 192MPa is found in the thin film.

A two-dimensional top view of the typical grain growth and stress formation through the depositing tin oxide is given in Fig. 13. As the coverage is increased and more islands impinge on each other forming grain boundaries, the stress is increased. The peak stress is reached at coalescence, when the film coverage is 1.00, meaning that the surface area is completely covered. It is also evident that high stress values are found in the islands as they collide with neighboring islands, forming grains. The final image in Fig. 13 shows the islands formed into grains at the point of film coalescence.

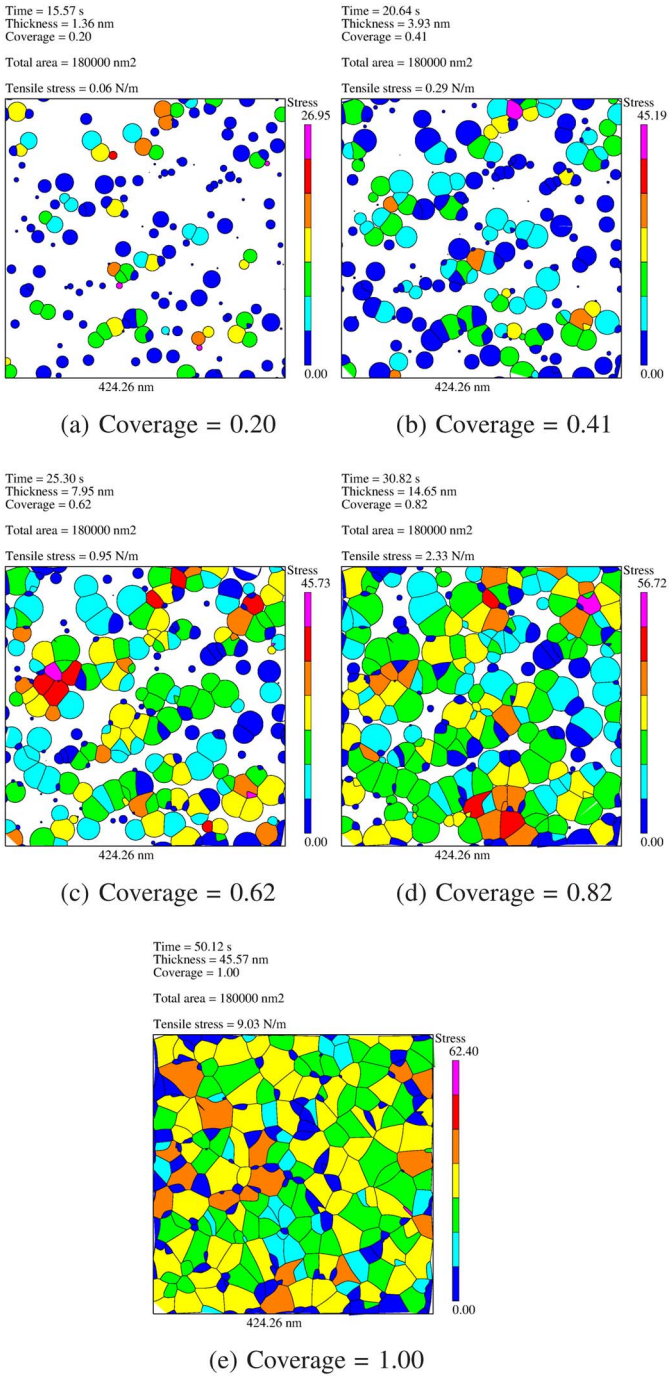


Fig. 13. Steps during film formation using the Volmer-Weber growth mode.

VI. Thermo-Mechanical Simulations

The thermo-mechanical stress accumulated after the deposition of metals and metal oxides and their subsequent cooling to room temperature are analyzed in this section. The structures studied are those generated in Section IV.

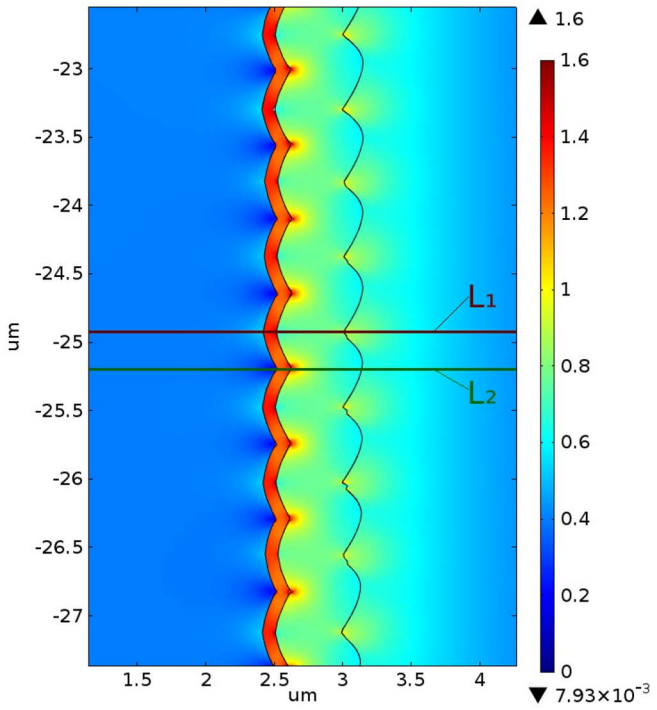
A (100) silicon wafer is considered in this study and when analyzing the effects of the generated stress on FETs, the x and y components of the principal stress tensors σ_{xx} and σ_{yy}, respectively are considered. The transistor channel is assumed to be oriented in the [-110] direction and the equation which governs the stress-induced current change is given by

$$\frac{\Delta I_d}{I_d} = -\left(\pi_{11}\sigma_{xx} + \pi_{12}\sigma_{yy}\right), \tag{9}$$

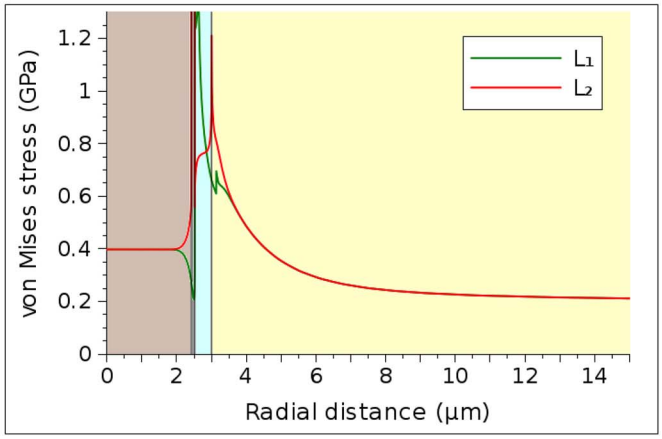
where π_{11} and π_{12} are technology-dependent piezo-coefficients for the transistor devices.

A. Thermo-Mechanical Stress in the Cu-Filled TSV

Due to copper's high CTE a high stress builds up in the metal layer as well as in the surrounding oxide and silicon layers. The structure described in Section IV-A and the relevant process parameters listed in Table III were imported into the finite element simulation tool Comsol Multiphysics [41] for the thermo-mechanical stress simulations. The bottom center of the TSV is fixed, while the rest of the boundaries are free.



(a) Stress (GPa) through a two-dimensional slice



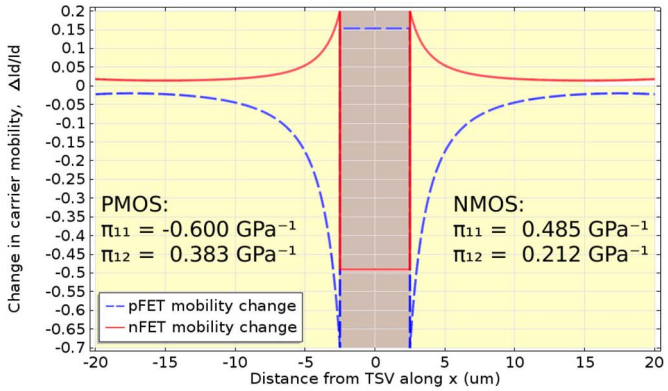
(b) Stress through L_1 and L_2 from (a)

Fig. 14. Thermo-mechanical stress through the middle of the copper-filled TSV viewed in the radial direction.

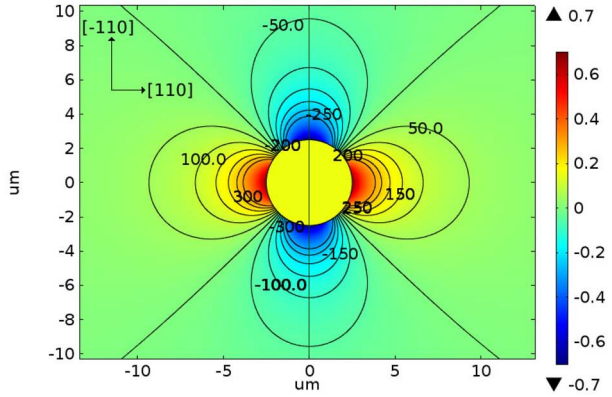
The results of the simulation, after cooling from 400°C to room temperature are summarized in Fig. 14 and Fig. 15.

In Fig. 14(a) the thermo-mechanical stress distribution through the two-dimensional radial cut of the structure can be observed. It is clear that the stress through the metal peaks at the scallop peaks, while the stress in the silicon and silicon dioxide peaks at locations, where two scallops meet. Fig. 14(b) shows the von Mises stress in the radial direction through the copper and silicon layers. The stress through the copper reaches about 240MPa, while the silicon stress peaks at about 800MPa at the interface with silicon dioxide. The simulations take into account copper plasticity using dislocation creep strain [49], [50]

$$\frac{d\epsilon}{dt} = A(\Delta\sigma)^n e^{\frac{-Q}{kT}}, \tag{10}$$



(a) Stress effects on nFET and pFET mobility



(b) pFET change in mobility ($\Delta I_d/I_d$)

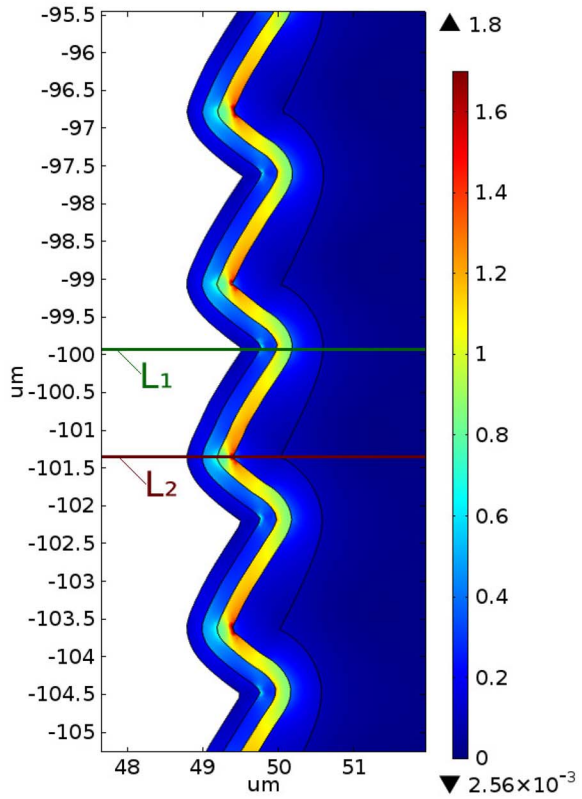
Fig. 15. The effect of the thermo-mechanical stress through the silicon from Fig. 14 on the mobility of 130nm devices. The contour lines show the x component of the stress tensor (MPa).

where $A = 45.13s^{-1}$ is the creep rate coefficient, $n = 2.5$ is the stress exponent, and $Q = 1J/mol$ is the creep activation energy [49].

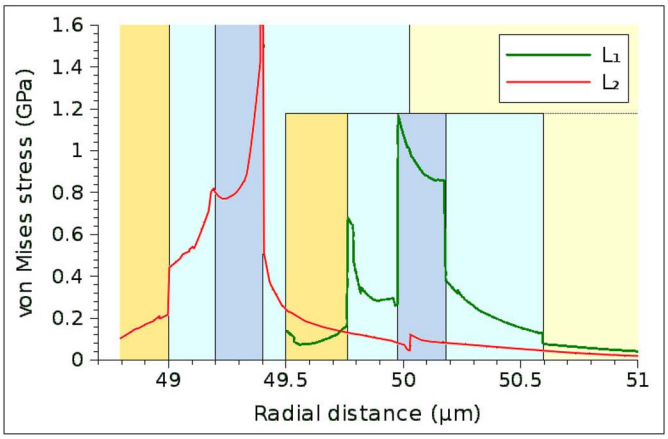
In addition to stress in the copper filling, the thermal variation has an effect on the stress in the silicon wafer in the vicinity of the TSV. In Fig. 15 the effect of the stress on the mobility of nFET and pFET devices are shown. The values of the piezo-coefficients are obtained from literature, in particular, from sample 130nm devices given in [51]. In Fig. 15(a) it is evident that the pFET mobility is impacted more than the nFET mobility. Therefore, a closer look into the stress effects on the pFET mobility is shown in a two-dimensional top view in Fig. 15(b). The contour lines show the x component of the stress tensor (MPa), which is the main stress component governing the mobility in pFETs.

B. Thermo-Mechanical Stress in the W-Lined TSV

A thermo-mechanical simulation similar to the one performed for the copper-filled structure was performed for the tungsten-lined TSV from Fig. 9. All boundaries are free except for the bottom left - or the bottom center of the TSV- which is fixed for the simulation. The resulting stress distribution is shown in Fig. 16, where the stress in the radial cross-section of the TSV is shown (Fig. 16(a)) in addition to



(a) Stress (GPa) through a two-dimensional slice

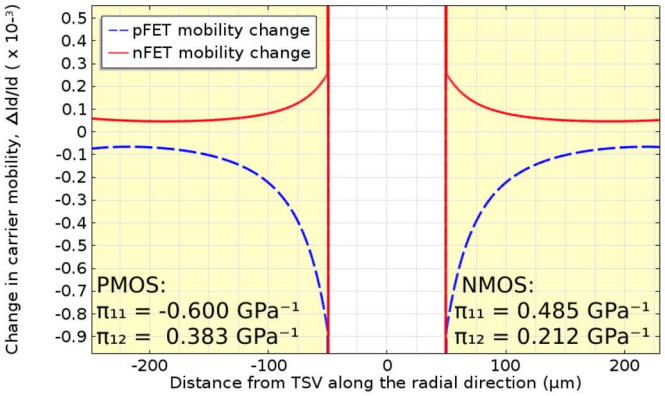


(b) Stress through L_1 and L_2 from (a)

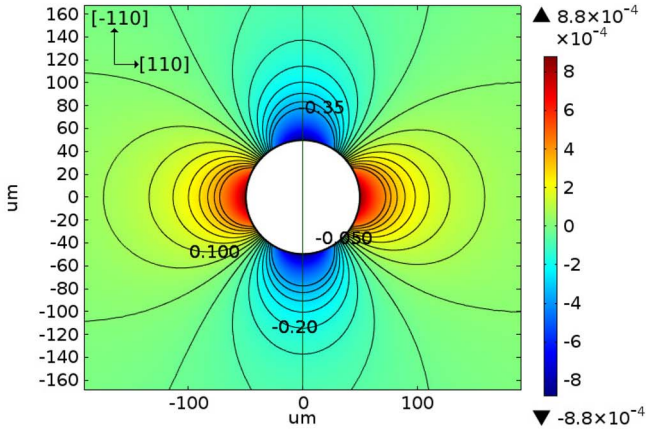
Fig. 16. Thermo-mechanical stress through the middle of the TSV viewed in the radial direction.

one-dimensional stress lines through the scallop peaks and valleys (Fig. 16(b)). From these results it is evident that the stress once again peaks at the points of contact between adjoining scallops.

It can be observed that the stress inside the tungsten lining peaks at about 1.6GPa, while the stress at the silicon/SiO_2 interface is at about 100MPa, much lower than the 800MPa observed for the Cu-filled TSV. The maximum displacement for the tungsten in the scalloped open TSV from Fig. 16 is found to be 450nm, while the minimum displacement is about 150nm. This is approximately 4 times more than the displacement which is experienced by an equivalent TSV without scallops along the sidewalls [52].



(a) Stress effects on nFET and pFET mobility



(b) pFET change in mobility ($\Delta I_d/I_d$)

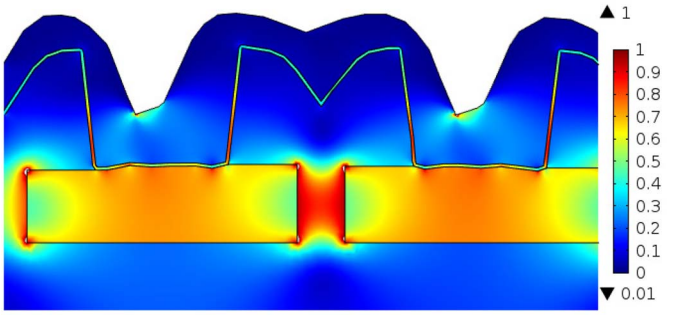
Fig. 17. The effect of the thermo-mechanical stress through the silicon from Fig. 16 on the mobility of 130nm devices. The contour lines show the x component of the stress tensor (MPa).

In Fig. 17 the effect of the stress on the mobility of nFET and pFET devices from [51] is shown. In Fig. 17(a) it is once again evident that the pFET mobility, shown in a two-dimensional top view in Fig. 17(b), is impacted more than the nFET mobility. Once again, the contour lines show the x component of the stress tensor (MPa).

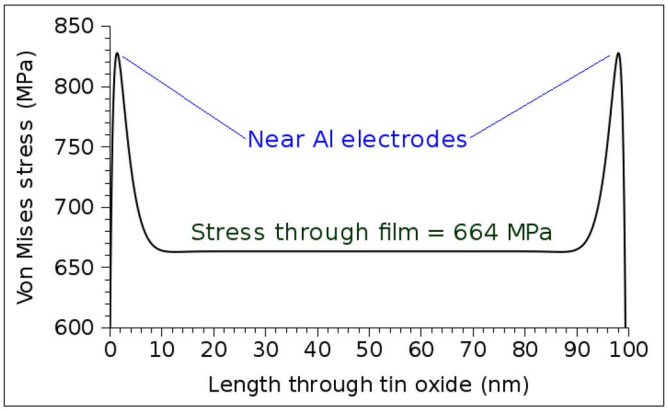
C. Thermo-Mechanical Stress in the SnO_2 Layer

After spray pyrolysis deposition and annealing are performed at 400°C, the sensor structure shown in Fig. 2 is cooled to room temperature. Similar to the case of filled and open TSVs, this temperature difference causes stresses between the passivation and the tin oxide material. For the simulation, the bottom border of the geometry from Fig. 18(a) is fixed, while the rest of the boundaries is free.

Fig. 18(a) shows the stress distribution through a two-dimensional slice of the sensor, where the electrodes, SiO_2, and the SnO_2 layers are present. The highest stress is noted in the SiO_2 layer between the two aluminum electrodes and in the tin oxide layer near the aluminum electrodes. This is not surprising, since aluminum has the a very high CTE compared to the oxide's very low CTE, as shown in Table II. The generated stress can lead to material cracking



(a) Von Mises stress (GPa) after cooling from 400°C to 20°C



(b) Stress through the tin oxide layer

Fig. 18. The von Mises stress distribution through the sensor structure including electrodes.

and delamination, when the tin oxide does not stick to the passivation layer properly. The stress through the SnO_2 layer shown in Fig. 18(b) is about 664MPa with slight peaks near the aluminum electrodes. When the intrinsic stress is added, this amounts to a total stress in the material of approximately 856MPa.

VII. Discussion

The stress build-up during fabrication of multiple components necessary for the 3D integration of metal oxide gas sensors have been examined using several simulation techniques. When performing this type of analysis using simulations, it is essential that processing models are included. The devices analyzed herein include a copper-filled TSV, a tungsten-lined open TSV, and a thin film of tin oxide, used as the sensing layer. For each structure the proper processing technique is analyzed and the appropriate stress growth is simulated and quantified. Further experimental and simulation studies are required in order to examine the effect of the stress on the electrical operation and sensitivity of the integrated sensor.

A. Copper-Filled TSV

The cylindrical hole necessary for the fabrication of a filled TSV is etched using DRIE. A sample TSV with a 5μm diameter and 50μm depth was generated using an in-house simulator. The geometry was then meshed and post-processed using the finite element method, where the thermal stress and its effect on nearby transistors was further analyzed. After the wafer etching, scallops with a height of 530nm and a width of 250nm were evident along the sidewall.

The main stress component in filled copper TSV structures is thermal. With the copper deposition performed at 400°C, the cooling to room temperature results in a stress of about 400MPa in the metal filling. However, the presence of the scallops causes the stress at the copper/TiN interface to vary between 300MPa and 500MPa. In addition, the stress at the SiO_2/Si interface is about 800MPa.

The high stress through the Silicon wafer affects the mobility of transistors located in the TSV's vicinity. The change in mobility results in the determination of a keep-out-zone (KOZ) around the TSV. If we consider a 5% variation in the transistor mobility as the reliability criterion, then a 9.4μm and a 5.5μm KOZ around the TSV is required for pFET and nFET devices, respectively.

B. Tungsten-Lined Open TSV

Just as in the copper-filled TSV, the cylindrical hole required to generate the tungsten-lined open TSV is etched using the DRIE process. The sample TSV generated using in-house simulation tools has a diameter of 100μm and a 200μm depth with scallop heights and widths of 2.2μm and 500nm, respectively. On top of the scalloped sidewalls a 500nm thick SiO_2 isolation layer was deposited, followed by three 200nm-thick films of tungsten (W), SiO_2, and Si_3N_4.

The deposition of thin tungsten films can be described using the Volmer-Weber growth mode, which introduces a tensile intrinsic stress of about 1.16GPa. In addition, a thermo-mechanical stress is introduced after cooling from the 400°C deposition temperature to room temperature. The scallops have a significant influence on the thermal stress in the tungsten, where it peaks at about 1.6GPa at locations where two scallops intersect, while an average of about 800MPa is observed inside the metal lining.

The thermal stress at the SiO_2/Si interface is about 100MPa, resulting in a change in mobility of about 0.089% and 0.026% for pFET and nFET devices directly at the interface, respectively. This means that no extra precautions need be made for a KOZ around the W-lined open TSV. Although no KOZ is required, the sheer fact that the TSV has a diameter of 100μm means that it requires much more space than the filled TSV with KOZ included. Therefore, the decision to use an open TSV in a design does not rest in the small KOZ, but in other benefits, such as the tungsten's improved electromigration behavior when compared to copper [21], [22].

The electrical performance of the open TSV was also analyzed, showing that the structure has a parasitic resistance, capacitance, and inductance on the order of 375mΩ, 6.527pF, and 5.307pH, respectively. These values are acceptable for structures of this size and desired functionality [53].

C. Tin Oxide Thin Film

The spray pyrolysis deposition technique is used to deposit a thin tin oxide film which acts as a gas sensing layer, when heated to temperatures between 300°C and 550°C. A 50nm

film is deposited on a substrate with 4 aluminum electrodes, when an intrinsic stress of 192MPa is reached. In addition, a thermo-mechanical stress of 664MPa is present in the film due to the cooling to room temperature after deposition at 400°C.

A build-up of mechanical stress in a metal or metal oxide film can have adverse effects on the electrical behavior of the manufactured device. For metal oxide gas sensors, this means that the presence of stresses and strains in the structure affects its sensitivity [4]. There are no studies which address the electrical sensitivity-strain relationship in metal oxide sensors and no information can be found in literature.

In addition to the stress in the tin oxide, a very high stress, on the order of 1GPa, builds-up in the silicon dioxide layer between two aluminum electrodes. This stress can lead to stress-induced voiding, cracking, or delamination at the electrode sites. Since the tin oxide film acts as a gas sensing device only when heated, the aluminum electrodes and the tin oxide film are placed on top of a microheater. The constant heating and cooling of the electrodes must be further investigated in order to have a true picture of all reliability concerns in the given structure.

VIII. Conclusion

Stress build-up in key components necessary for the 3D integration of a smart gas sensor device in CMOS technology has been examined. The three-dimensional integration of a MEMS manufactured sensor device and essential analog and digital CMOS circuitry has been analyzed through a simulation study of several TSV structures. A copper-filled TSV is examined for thermo-mechanical stress while the intrinsic and thermo-mechanical stress of a tungsten-lined open TSV has been explored by means of simulation. Due to the DRIE process required to generate the TSV structures, a scalloped sidewall lines the trenches of the TSVs. These scallops can significantly influence the thermal stress in the metal layers at the Si/SiO_2 and metal/liner interfaces. The change in carrier mobility due to the presence of the thermal stress around the TSVs has also been analyzed, showing that a keep-out-zone is necessary for copper-filled TSVs. The tungsten-lined TSVs do not require a keep-out-zone, but one must take into account the fact that the open TSVs are, due to fabrication limitations, already much wider than filled TSVs.

In addition, the deposition of tin oxide, which serves as the gas sensing surface, has been analyzed and the stress generated through the deposition has been examined. A 192MPa intrinsic stress through the material is simulated, along with a 664MPa thermo-mechanical stress generated after cooling the structure down to room temperature from a deposition temperature of 400°C. Further studies are desired in order to link the stress levels to the sensitivity and operation of the sensor device.

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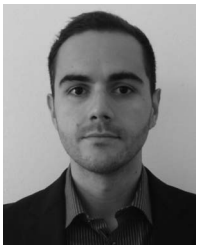

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