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REGULAR PAPER

Bias-temperature instability on the back gate of single-layer double-gated graphene field-effect transistors

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We study the positive and negative bias-temperature instabilities (PBTI and NBTI) on the back gate of single-layer double-gated graphene field-effect transistors (GFETs). By analyzing the resulting degradation at different stress times and oxide fields we show that there is a significant asymmetry between PBTI and NBTI with respect to their dependences on these parameters. Finally, we compare the results obtained on the high-*k* top gate and SiO_2 back gate of the same device and show that SiO_2 gate is more stable with respect to BTI.
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1. Introduction

Graphene is a superior two-dimensional (2D) material which is characterized by unique physical and electrical properties, such as an extremely high room-temperature carrier mobility[1,2] and high saturation velocity.[3] A nice compatibility of this material with standard CMOS technology[4] is especially crucial for enhancement of the performance and functionality of advanced microelectronic devices and, consequently, silicon integrated circuits. Therefore, in the meantime graphene is considered a promising candidate for various industrial applications. In particular, different groups have recently succeeded in fabricating graphene field effect transistors (GFETs)[5–10] and related electronic devices.[11,12] These achievements create a demand for characterization of the reliability of these devices. Nevertheless, only a few attempts to study the reliability of GFETs with respect to bias-temperature instabilities (BTI) have been undertaken by other groups.[13–16] At the same time, we have reported several studies for both BTI and hot-carrier degradation (HCD) in single-layer double-gated GFETs.[17–20] However, only the reliability of high-*k* top gate oxide has been examined in our previous works.

Here we study the bias-temperature instability resulting from a voltage applied on the SiO_2 back gate of double-gated GFET. We show that there is an asymmetry between positive and negative BTI (PBTI and NBTI) in terms of the degradation magnitude and its dependence on the stress oxide field. Finally, we compare the results obtained on the SiO_2 back gate and high-*k* top gate of the same device.

2. Devices

We perform our study on single-layer double-gated GFETs fabricated on a thermally oxidized silicon substrate using a standard lithography process.[4] An isometric view and a schematic cross-section of these devices are given in Fig. 1. Contrary to our previous works,[17–20] the thickness of the SiO_2 layer in these devices is 92 nm rather than 1800 nm. This allowed us to observe back gate BTI at reasonable stress voltages. The top gate insulator is a 25 nm thick Al_2O_3 layer, while the channel has a length of 4 μm and a width of 80 μm. Also, in order to reduce the device-to-device variability, the devices have been baked at $T = 300\,°C$ for 5 h before the experiments.

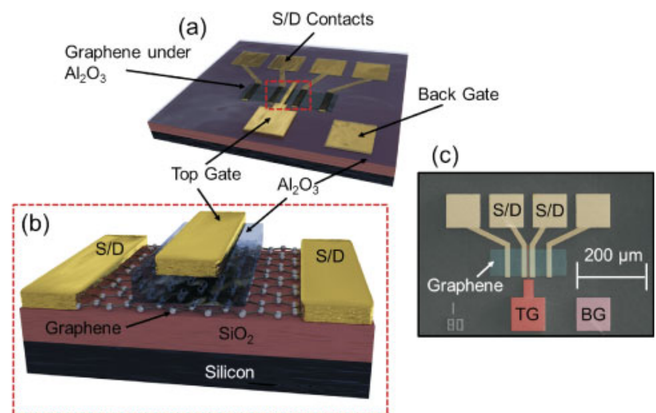

Fig. 1. (Color online) (a) Schematic layout of the double-gated single-layer GFET. (b) A cross-section of the channel region. The graphene channel is sandwiched between Al_2O_3 as a top gate insulator and SiO_2 as a back gate insulator. (c) Top view of the investigated double-gated GFET obtained using scanning-electron microscopy (SEM). The top gates and source/drain pads are made of Ti/Au and the back gates of Al.

3. Experiment

All our experiments were performed in vacuum ($\sim 10^{-5}$ Torr), in order to avoid the detrimental impact of the environment.[21] The BTI dynamics were examined as follows: after measuring the reference gate transfer characteristics, the subsequent stresses with increasing $V_{BG} - V_D$ (back gate voltage minus Dirac point voltage) and top gate voltage $V_{TG} = 0$ were applied. The resulting gate transfer characteristics were measured after each stress using $V_d = 20\,mV$, while in some cases the recovery of the stressed device was monitored as well. This allowed us to capture the degradation magnitude versus the stress oxide field F_{ox}. A similar technique with increasing $V_{TG} - V_D$ and $V_{BG} = 0$ was applied for the top gate BTI measurements.

4. Back gate BTI: Stress oxide field dependence and recovery

In Fig. 2(a) we show the measured evolution of the back gate

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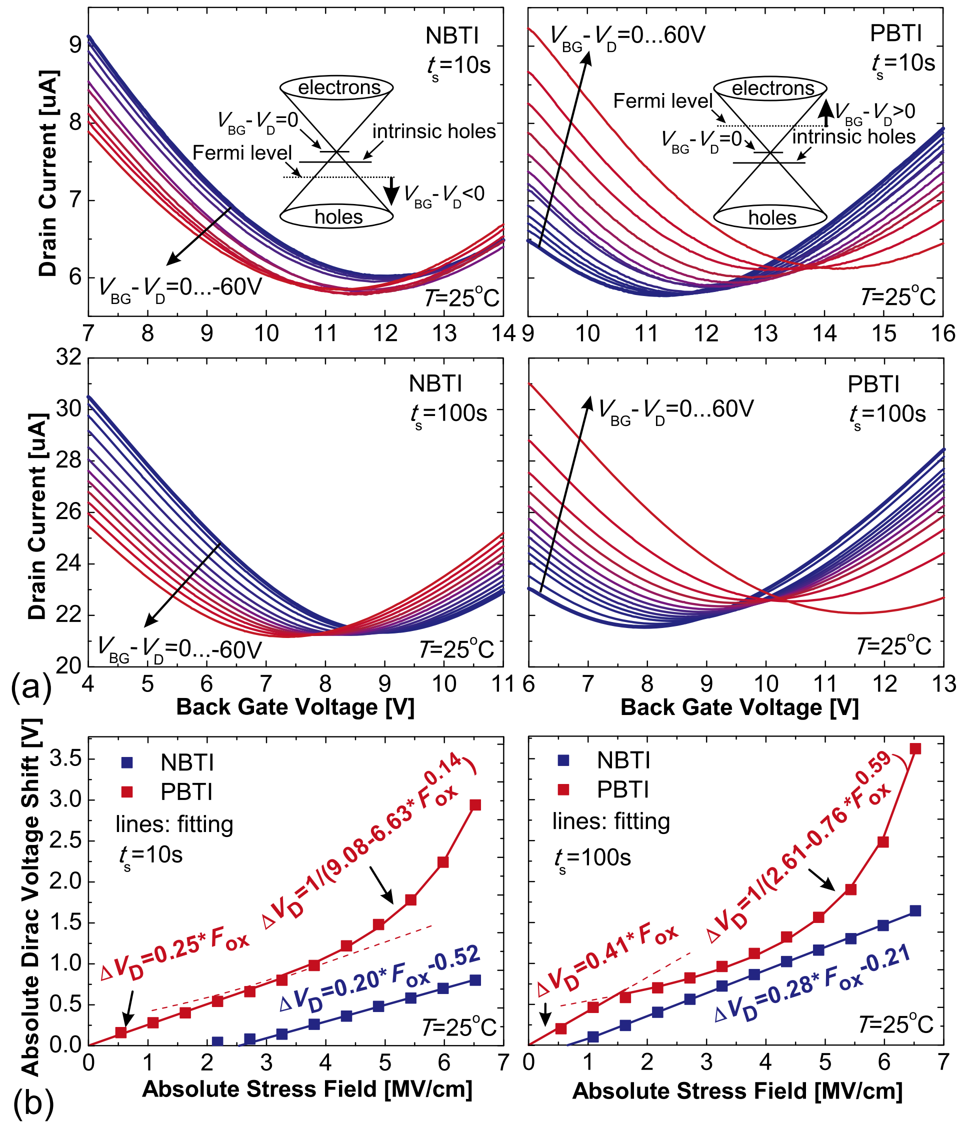

Fig. 2. (Color online) (a) Evolution of the back gate transfer characteristics after subsequent stresses with increasing $V_{BG} - V_D$ and two different stress times for NBTI (left) and PBTI (right). (b) The resulting V_D shift versus stress oxide field for $t_s = 10\,s$ (left) and $t_s = 100\,s$ (right).

transfer characteristics after the subsequent NBTI and PBTI stresses with $V_{BG} - V_D$ varied from 0 to ± 60 V in ± 5 V steps. As was suggested in Refs. 17 and 18, we express the degradation magnitude in terms of a Dirac point voltage shift ΔV_D. This quantity is directly linked to the charged trap density shift $\Delta N_T = \Delta V_D C_{ox}/q$ with C_{ox} being the oxide capacitance. The resulting dependences of ΔV_D on the stress oxide field $F_{ox} = (V_{BG} - V_D)/d_{ox}$ are plotted in Fig. 2(b) for the stress times $t_s = 10$ and 100 s. Contrary to Si technologies, in both cases PBTI degradation is stronger than its NBTI counterpart. Moreover, there is a significant difference between PBTI and NBTI with respect to the dependence of the observed Dirac voltage shifts on the stress oxide field. While the NBTI shift linearly increases versus F_{ox}, growth of PBTI shift is linear only at small F_{ox} and can be fitted with a Langmuir power law $f(x) = 1/(a - bx^c)$ at larger oxide fields. At the same time, for both NBTI and PBTI the slopes in the linear regions increase versus t_s. This is because the probability of carrier trapping becomes larger for longer stresses.

Interestingly, transition of PBTI curves to a Langmuir-like behavior takes place at smaller F_{ox} if t_s is larger. This leads to a smaller difference between PBTI and NBTI shifts at moderate t_s, although PBTI still remains stronger than NBTI [Fig. 2(b), right]. Since in GFETs PBTI is associated with electron trapping and NBTI is due to hole trapping, we assume that the main reason for the observed behavior is the difference in the kinetics of the two processes, as well as the energetic alignment of the trap bands with the Fermi level in the graphene channel. Another issue which contributes the asymmetry between NBTI and PBTI is the positive initial values of V_D, which are typical for all our GFETs. This means that our graphene is p-doped, i.e., some intrinsic holes are present even if $V_{BG} = 0$. Most likely, trapping of these intrinsic holes is less efficient, especially if the stress time is small. Therefore, NBTI degradation is weakly pronounced at small F_{ox}, when $-V_D < V_{BG} - V_D < 0$, i.e., the applied voltage is not enough to shift the Fermi level below the intrinsic level [Fig. 2(a), inset].

Contrary to NBTI, PBTI is independent of the intrinsic hole level position, since any stress with $V_{BG} - V_D > 0$ introduces extrinsic electrons and shifts the Fermi level into the conduction band. That is why some PBTI degradation is clearly visible even after a stress with $t_s = 1$ s and $F_{ox} < 1$ MV/cm [Fig. 3(a)]. However, the dependence of the

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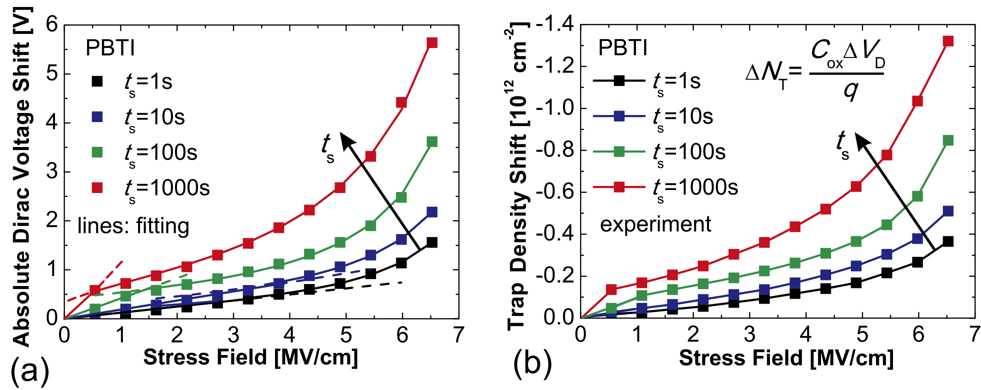

Fig. 3. (Color online) Stress field dependence of the ΔV_D (a) and ΔN_T (b) after PBTI stresses with different t_s. $\Delta N_T < 0$ means electron trapping.

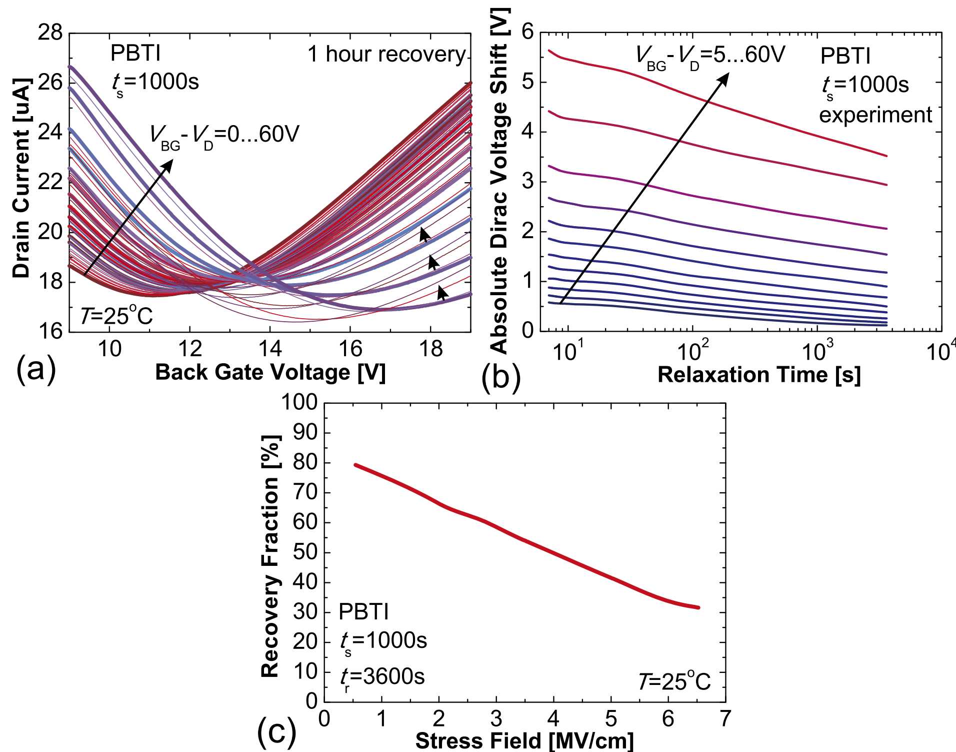

Fig. 4. (Color online) (a) Time evolution of the back gate transfer characteristics after subsequent PBTI stress/recovery rounds with increasing $V_{BG} - V_D$. (b) The corresponding $\Delta V_D(t_r)$ recovery traces. (c) The recovery fraction measured 1 h after the stress decreases versus the stress oxide field.

magnitude of the PBTI shifts on the stress oxide field is strongly correlated with the stress time. For example, if t_s is small, the PBTI shift moderately increases in a linear manner up to quite large F_{ox}. Conversely, in the case of long stresses a strong linear dependence of ΔV_D on F_{ox} is observed only in a very narrow range of small F_{ox}, being immediately substituted by a Langmuir-like behavior. Obviously, the same type of oxide field dependence is typical for the charged trap density shift ΔN_T, which is proportional to ΔV_D [Fig. 3(b)]. However, the values of ΔN_T observed for GFETs are 10^{11}–10^{12} cm^{-2}, which is significantly larger than for Si technologies (10^{10}–10^{11} cm^{-2}).[22]

Next we examine the time evolution of the back gate transfer characteristics after the BTI stress. In order to do this, we fix a comparably large $t_s = 1000$ s and monitor the recovery during 1 h after the end of stress with a certain $V_{BG} - V_D$. This allows to express the recovery dynamics in terms of the traces ΔV_D versus the relaxation time t_r. The results obtained for PBTI are shown in Fig. 4. Clearly, the back gate BTI degradation in GFETs is recoverable, similarly to its counterpart observed on the high-k top gate[17,18] and also to Si technologies.[23–28] Remarkably, after the stress with smaller oxide field the recovery is faster, while the fraction of recovered degradation is larger [Fig. 4(c)]. The latter observation is also similar to Si technologies.[28] At the same time, the distances between the recovery traces increase versus $V_{BG} - V_D$, following the Langmuir-like dependence which is typical for PBTI with $t_s = 1000$ s [cf. Fig. 3(a)].

5. Comparison with top gate BTI

Finally, we measured the oxide field dependences of the Dirac point voltage shift after the PBTI stress applied on the high-k top gate. The results for PBTI degradation obtained on the SiO_2 back gate and Al_2O_3 top gate of the same GFET are

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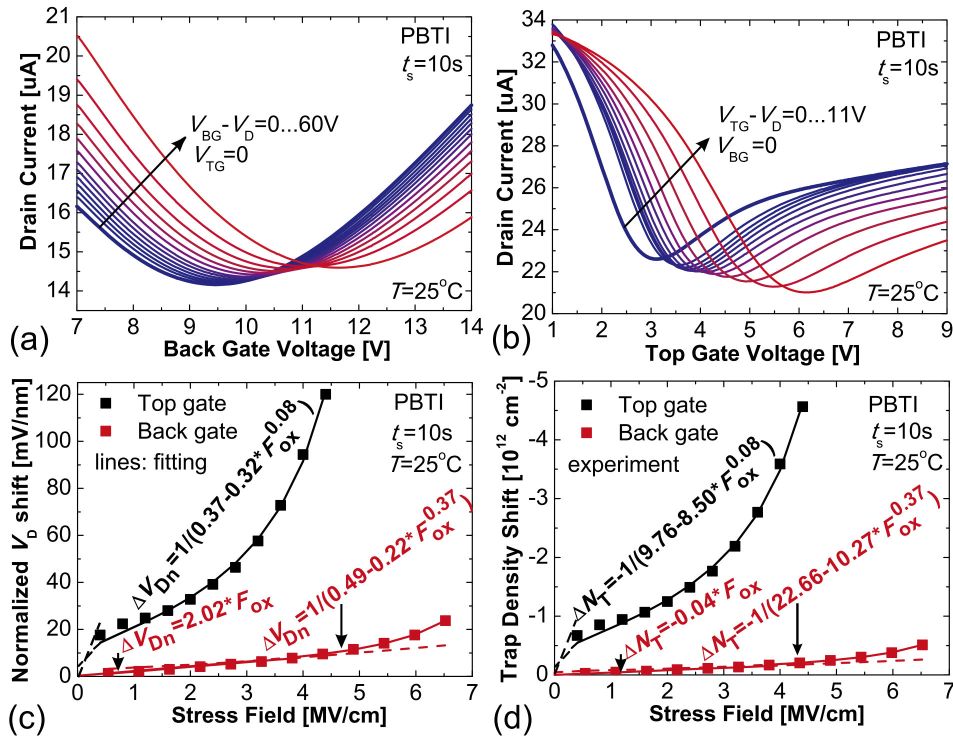

Fig. 5. (Color online) Evolution of the back gate (a) and top gate (b) transfer characteristics after the subsequent PBTI stresses with increasing oxide field. Comparison of the resulting ΔV_{Dn} (c) and ΔN_T (d).

compared in Fig. 5. One can see that the direction of the Dirac point voltage shift is the same [Figs. 5(a) and 5(b)], which means that an electron trapping takes place independently of whether the PBTI stress is applied on the top or back gate of GFET. At the same time, the Dirac point current is shifted in opposite directions, which is most likely because the negatively charged traps situated in SiO_2 and Al_2O_3 interfacial layers impact the carrier mobility in a different manner.

However, a significant difference in the oxide thicknesses requires us to operate with a normalized Dirac point voltage shift $\Delta V_{Dn} = \Delta V_D/d_{ox}$ (cf. Ref. 29) when making a quantitative comparison of the degradation magnitudes on the top and back gates. The $\Delta V_{Dn}(F_{ox})$ dependences obtained for the two cases are shown in Fig. 5(c). Clearly, the magnitude of PBTI degradation on the top gate is considerably larger. This is similar to Si technologies, where the reliability of high-k oxides also presents an important issue.[30] At the same time, the dependence on F_{ox} in the case of top gate PBTI is purely Langmuir-like, while an abrupt linear increase is expected only close to $F_{ox} = 0$, to maintain zero degradation at zero oxide field. This is despite $t_s = 10$ s, which leads to a significant linear region in the case of back gate PBTI. In other words, the behaviour of the top gate PBTI degradation versus F_{ox} observed using $t_s = 10$ s is similar to those which has been measured on the back gate with significantly larger stress times (Fig. 3). Also, it is clear that the resulting charged trap density shift is larger for the top gate PBTI [Fig. 5(d)]. Therefore, we can conclude that the high-k top gate is considerably less stable with respect to BTI than the SiO_2 back gate.

6. Conclusions

We have performed an experimental study of BTI on the back gate of double-gated GFETs. It has been found that there is a considerable asymmetry between NBTI and PBTI in terms of degradation magnitude and its dependence on the stress parameters. At the same time, the recovery of the back gate BTI has been shown to be similar to those previously reported for Si technologies and for the high-k top gate BTI in GFETs. Finally, the back gate BTI degradation dynamics is similar to the one observed on the high-k top gate, although the magnitude in the latter case is significantly larger. Therefore, we can conclude that the BTI stability of the SiO_2 back gate is better compared to the high-k top gate, which is similar to Si technologies.

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