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Long-Term Stability and Reliability of Black Phosphorus Field-Effect Transistors

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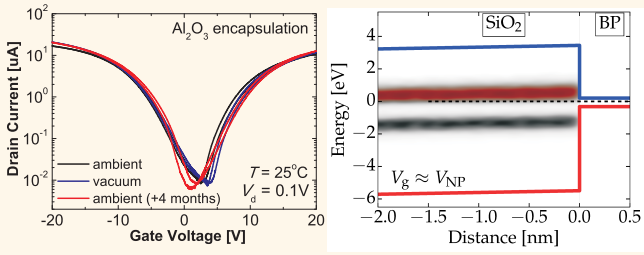
Supporting Information

ABSTRACT: **Black phosphorus has been recently suggested as a very promising material for use in 2D field-effect transistors. However, due to its poor stability under ambient conditions, this material has not yet received as much attention as for instance MoS_2. We show that the recently demonstrated Al_2O_3 encapsulation leads to highly stable devices. In particular, we report our long-term study on highly stable black phosphorus field-effect transistors, which show stable device characteristics for at least eight months. This high stability allows us to perform a detailed analysis of their reliability with respect to hysteresis as well as the arguably most important reliability issue in silicon technologies, the bias-temperature instability. We find that the hysteresis in these transistors depends strongly on the sweep rate and temperature. Moreover, the hysteresis dynamics in our devices are reproducible over a long time, which underlines their high reliability. Also, by using detailed physical models for oxide traps developed for Si technologies, we are able to capture the channel electrostatics of the black phosphorus FETs and determine the position of the defect energy band. Finally, we demonstrate that both hysteresis and bias-temperature instabilities are due to thermally activated charge trapping/detrapping by oxide traps and can be reduced if the device is covered by Teflon-AF.**



KEYWORDS: *stability of black phosphorus, phosphorene, transistor, oxide defects, hysteresis, bias-temperature instabilities*

Black phosphorus (BP), also known as phosphorene in the single-layer limit,[1−3] is a crystalline semiconductor that is formed by 2D atomic layers stacked together by van der Waals interactions. The calculations[1] have shown that this material has a direct band gap ranging from 0.3 eV in bulk to >1 eV in the single-layer limit.[4] Therefore, BP is now considered a promising material capable of outperforming graphene[5,6] in digital device applications. At the same time, the comparatively high hole mobility (286 $cm^2/(V\,s)$ in ref 1 and up to 1000 $cm^2/(V\,s)$ in ref 3) makes BP a promising candidate as a channel material in p-FETs, which are required for low-power integrated complementary MOS (CMOS) and thin-film transistor (TFT) circuits. Thereby, BP would nicely complement MoS_2, which appears more suitable for n-channel devices.[7−12]

Since the discovery of phosphorene,[1,3] a few successful attempts at fabricating field-effect transistors with a few-layer black phosphorus channel (BPFETs) have been reported.[1,3,13−15] However, most studies are limited to the description of fabrication details and the investigation of basic device characteristics such as on/off current ratios and mobilities. Furthermore, the poor air stability of BP is a serious concern, and various capping schemes have been proposed.[15,16] However, for any material system that is to acquire some technological significance, its long-term stability and reliability must be understood. Apparently, the reliability of all 2D transistors investigated so far is reduced by charge trapping due to oxide traps.[17−19] In its most obvious form, this charge trapping results in the ubiquitous hysteresis observed in all these devices. These oxide traps typically have a very broad distribution of time constants, ranging from microseconds and below to weeks, months, and years.[20] As a consequence, at longer times, charge trapping results in slow drifts of the transistor characteristics,[21−25] known as bias-temperature instabilities (BTI), arguably the most important reliability issue in Si technologies.[26] While it may be hoped that some of these traps are a result of nascent processing conditions and can likely be removed by process optimization, we argue that possibly a sizable contribution comes from unavoidable traps that are simply a natural consequence of pairing certain

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insulator and channel materials. This is because every insulator studied so far has certain defect bands that should be energetically far from the conduction/valence bands in the n/p-FET channels, respectively. For example, it has been shown that the same gate stack shows considerably less charge trapping in p-MOSFETs when a SiGe channel is used instead of Si, since the valence band in SiGe is higher than that of Si.[27] As a consequence, charge-trapping investigations must be an integral part of the search for a suitable material system for future field-effect transistors. With respect to BP, however, no analysis of the hysteresis and BTI has been reported so far. Given the poor stability of BP in air, such studies have only become possible now due to the recent introduction of suitable capping schemes.[15,16]

In the following, we report the presence of a hysteresis in BPFETs and perform the systematic study of this phenomenon. We demonstrate that the hysteresis is well reproducible and remains almost unaffected by aging and electrical stressing, although the hysteresis of our BPFETs increases significantly at higher temperatures. Furthermore, we report the presence of positive and negative BTI (PBTI and NBTI) in BPFETs and show that the related trapping/detrapping processes are thermally activated. All these observations are consistent with the existence of a broad distribution of oxide traps, with the faster ones contributing to the hysteresis and the slower ones to BTI. Therefore, we have made an attempt to evaluate the defect energy bands present in these transistors.

RESULTS AND DISCUSSION

We examine back-gated BPFETs with 80-nm-thick SiO_2 as a gate insulator and contact pads made of Ti/Au. The schematic configuration of our devices is shown in Figure 1a. In order to prevent severe degradation of black phosphorus films through reactions with water molecules in ambient air and thereby achieve high stability,[15,16,28] our BPFETs have been encapsulated with either a 25-nm-thick Al_2O_3 layer (referred to as Al_2O_3 encapsulation in the following) or a double Al_2O_3/Teflon-AF layer (double-layer encapsulation in the following). As previously reported,[15] atomic-layer deposition (ALD) of an Al_2O_3 layer with a thickness greater than the flake thickness provides good encapsulation of BPFETs with conformal coverage. At the same time, the double-layer encapsulation further improves both the electrical properties and the air stability of BPFETs due to the highly hydrophobic property of the Teflon-AF layer,[29] which inhibits long-term diffusion of water molecules into the Al_2O_3 layer and/or possible pinholes (see more details in the Supporting Information (SI), Figure S1).

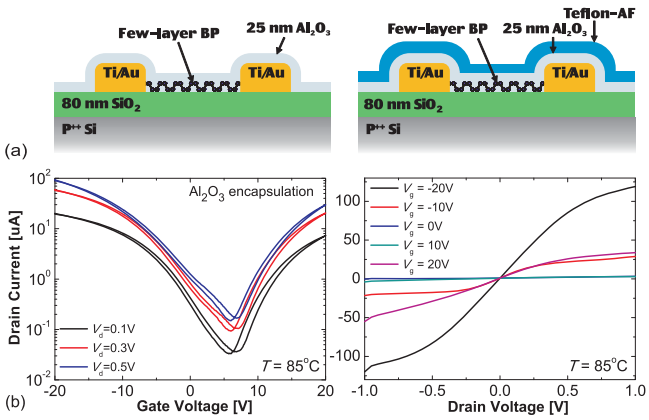

Figure 1. (a) Schematic layout of our back-gated BPFETs with Al_2O_3 encapsulation (left) and Al_2O_3/Teflon-AF double-layer encapsulation (right). In both structures, a bottom P++ gate with a 80 nm SiO_2 gate insulator and a 4/40 nm layer of Ti/Au contact electrodes were used. The channel lengths for the Al_2O_3 and double-layer encapsulated devices are 500 and 250 nm, respectively. Few-layer phosphorene flakes were mechanically exfoliated directly onto the Si/SiO_2 substrate and selected according to optical contrast to have a thickness of <15 nm. (b) Left: Gate transfer (I_d−V_g) characteristics of our devices contain both p- and n-conduction regions with the charge neutrality point in between them. Also, a small hysteresis due to charging/discharging of fast traps is present. Right: The output (I_d−V_d) characteristics of the BP channel transistors exhibit some saturation.

We initially assumed that some aging of our BPFETs would take place in ambient conditions even after encapsulation[15] and therefore measured the electrical characteristics in a vacuum (5×10^{-6}−10^{-5} Torr). However, when the experiments were periodically repeated under ambient conditions over an interval of eight months, we found that our results could be reproduced, which means that the encapsulation layer makes our devices extremely stable. Initially, the general behavior of the BPFET transfer (drain current as a function of top gate voltage, I_d−V_g) and output (drain current as a function of source−drain voltage, I_d−V_d) characteristics was analyzed. Our results shown in Figure 1b are very similar to those published previously.[1,3,13−15] In particular, the I_d−V_g characteristics of our devices exhibit ambipolar behavior and contain a hysteresis related to charging/discharging of fast oxide traps. The output characteristics measured at different V_g show a linear behavior at smaller drain voltage V_d and some signs of saturation at larger V_d.

The hysteresis was investigated by measuring the I_d−V_g characteristics at V_d = 0.1 V using different sweep rates S and sweep ranges V_{gmin} to V_{gmax}. In order to capture the full frequency range of the fast traps responsible for the hysteresis, $S = V_{step}/t_{step}$ was varied between 0.02 and 10 000 V/s by adjusting the step voltage V_{step} and the sampling time t_{step}. The measurements were performed at four different temperatures (T = −193, 25, 85, and 165 °C). As for the BTI measurements, they have been conducted using subsequent stress/recovery rounds[17] with stress times t_s = 10, 100, 1000, and 10000 s at T = 25 and 165 °C. Also, since BPFETs are ambipolar devices, in the spirit of our previous work for graphene FETs[17] we expect some dependence of the BTI shifts on the I_d−V_g sweep direction. Thus, the measurements of I_d−V_g characteristics at different stress/recovery stages have been performed by sweeping either from more negative toward more positive V_g (*i.e.*, V^+ sweep mode) or *vice versa* (*i.e.*, V^- sweep mode). This is in contrast to our work on unipolar MoS_2 FETs,[30] where only the V^+ sweep mode has been used. Furthermore, in order to avoid artifacts due to the more or less arbitrary definition of the threshold voltage for ambipolar devices, we express the BTI degradation/recovery dynamics in terms of the charge neutrality point voltage shift, ΔV_{NP}.

First we have verified the impact of aging on the performance of our BPFETs at T = 25 °C. As shown in Figure 2a, several months of intensive measurements followed by storage of the devices under ambient conditions only marginally affected the I_d−V_g characteristics of our BPFETs. While our experiments at different temperatures performed within the first four months

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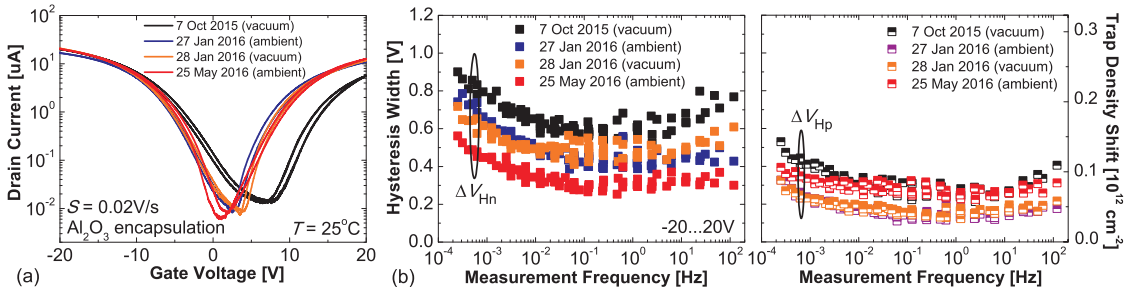

Figure 2. (a) Transfer characteristics measured in a vacuum and in ambient conditions over a period of almost eight months. (b) Hysteresis widths ΔV_{Hn} (left) and ΔV_{Hp} (right) *versus* measurement frequency extracted close to the threshold voltages defined using a constant current criterion. The good reproducibility of the results confirms that the Al_2O_3 encapsulation conserves the main properties of our devices.

have caused some visible transformation of the transfer characteristics, storage of the device under ambient conditions during the following four months did not affect the device performance. As such, our BPFETs are stable for at least eight months, which is considerably larger than what has been ever reported so far.[15,31−33] Remarkably, the measurements under ambient conditions and in a vacuum performed within 2 days gave nearly identical results. We also note that in all four cases the I_d−V_g characteristics contain some hysteresis in both the electron and hole conduction regions, which can be described by the widths ΔV_{Hn} and ΔV_{Hp}, respectively. In Figure 2b we show that ΔV_{Hn} and ΔV_{Hp} extracted closely to the threshold voltages depend on the measurement frequency, $f = 1/(Nt_{step})$, with $N = 2((V_{gmax} - V_{gmin})/V_{step} + 1)$ being the number of points. Although some hysteresis is present within the whole range of measurement frequencies, it becomes more pronounced when slower sweeps are used. At the same time, the hysteresis width ΔV_{Hn} is considerably larger than ΔV_{Hp}, which means that the device is more stable in the hole conduction region. This is an interesting coincidence, since BP has been often suggested for p-channel applications. Interestingly, the dependences of ΔV_{Hn} and ΔV_{Hp} on f are well reproducible and remain almost independent of aging of the device; that is, the corresponding charge trap density shift for the electron and hole conduction regions, $\Delta N_{Hnlp} = \Delta V_{Hnlp} C_{ox}/q$, remains stable. This further confirms that the Al_2O_3 encapsulation effeciently protects the devices from the detrimental impact of the environment and considerably improves their stability. More results on the device stability can be found in the SI (Figures S2−S4).

After verification of the stability of our BPFETs up to at least T = 165 °C (see Figure S4 in the SI), we analyzed the temperature dependence of the hysteresis in BPFETs with Al_2O_3 encapsulation. In Figure 3a the transfer characteristics measured using S = 0.02 V/s and 10 V/s at four different temperatures are shown. Clearly, at higher temperatures the hysteresis becomes larger, especially for smaller sweep rates. At the same time, the charge neutrality point current increases. In Figure 3b we provide the dependences of the hysteresis width *versus* the measurement frequency and the gate voltage dependence of the corresponding charge trap density shift. While at T = −193 °C the hysteresis is mostly dominated by faster traps, which can respond at f > 1 Hz, the temperature increase leads to a strong thermal activation of slower traps responding only at f < 0.01 Hz. Hence, at T = 165 °C the hysteresis stability of our BPFETs is dramatically reduced by a strong impact of slower traps (for a more detailed interpretation see Figures S5 and S6 in the SI). This is similar to Si technologies, where charging/discharging of slow oxide

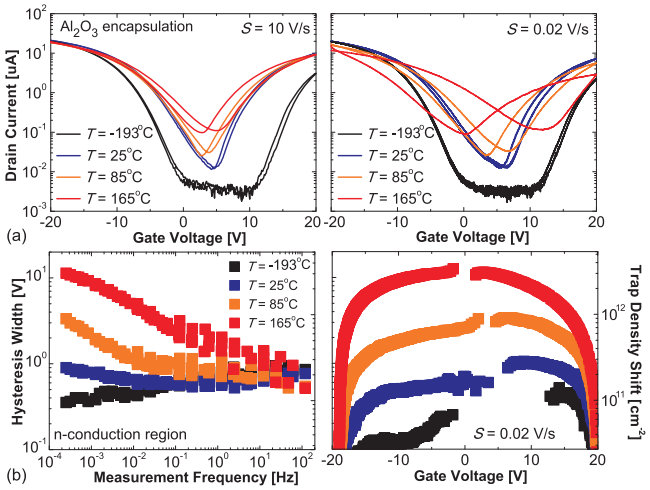

Figure 3. (a) The gate transfer characteristics of our BPFETs measured using S = 10 V/s (left) and S = 0.02 V/s (right) at different temperatures. At higher temperature the hysteresis is more pronounced, especially for very small S. (b) Hysteresis width measured near the threshold voltage for different measurement frequencies (left) and the gate voltage dependence of the hysteresis width and the corresponding charge trap density shift obtained using a slow sweep rate (right). The contribution of slower traps in BPFETs is strongly activated by temperature.

traps responsible for BTI is also known to be thermally activated.[26] At the same time, the difference between ΔV_{Hp} and ΔV_{Hn} is less pronounced at higher temperatures, while at T = 165 °C ΔV_{Hp} becomes slightly larger than ΔV_{Hn}.

Next we analyze the bias-temperature instabilities in our BPFETs with Al_2O_3 encapsulation. In Figure 4 we show that at T = 165 °C PBTI degradation becomes considerably stronger than it was at T = 25 °C. This agrees with our hysteresis results (Figure 3), which confirms that a strong thermal activation of charge trapping is present. At the same time, at higher temperature the recovery is considerably faster, which is similar to Si technologies[26] and graphene FETs (GFETs).[17] Furthermore, the recovery traces for PBTI are well reproducible and do not depend on the sweep direction, which is also similar to GFETs.[17] Conversely, thermally activated NBTI degradation strongly depends on the sweep direction, just like it has been previously noticed for GFETs[17] (see Figures S7 and S8 in the SI for more details).

In order to understand the origin of PBTI and NBTI degradation in BPFETs, we have performed technology computer-aided design (TCAD) simulations[34] with the barrier parameters of the BP/SiO_2 interface taken from the literature

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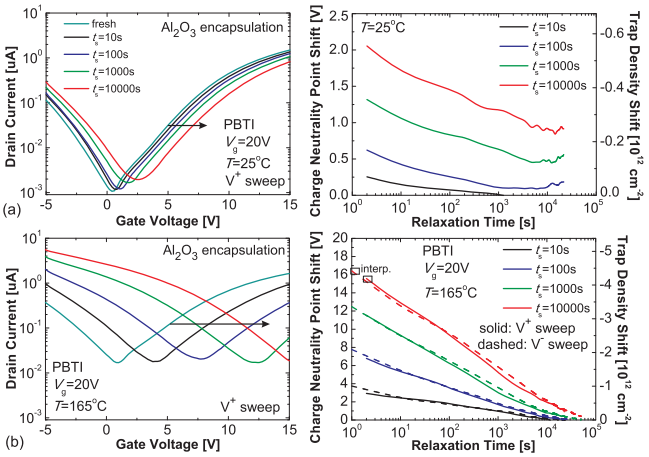

Figure 4. Evolution of the transfer characteristics of our BPFETs after subsequent PBTI stresses with increasing stress times (left) and the recovery traces for the charge neutrality point voltage shift (right). (a) T = 25 °C. (b) T = 165 °C. Similarly to GFETs[17] and Si technologies,[26] at higher temperature the degradation is stronger and the recovery is faster. Interestingly, a complete recovery can be observed at higher T, while there is no dependence on the sweep direction.

(E_g = 0.6 eV for the band gap and χ = 4.13 eV for the electron affinity of few-layer black phosphorus).[35−37] Although the BP/SiO_2 system is not as well parametrized as the Si/SiO_2 interface, we could obtain reasonable fits for the measured transfer characteristics (see Figure S9 in the SI), which means that the device electrostatics can be reliably reproduced. This allowed us to simulate the band diagrams of the channel cross-section of our BPFETs and determine the defect level position, which would lead to the measured PBTI and NBTI on the same device (Figure 5). We have identified two distinct hole defect bands in SiO_2, one with a trap level E_T^l = 4.44 ± 0.35 eV and another with E_T^u = 6.25 ± 0.40 eV above the oxide valence band. The former was extracted in our previous work[38] for Si devices, where it considerably contributes to charge-trapping issues. However, in the case of BPFETs this band is far below the valence band of BP and thus does not have a considerable impact on charge trapping. At the same time, due its energetic alignment, the upper defect band can cause severe degradation. The trap level of this band was extracted using TCAD simulations. This confirms that charge trapping is mainly due to the energetic alignment between the defect band in the oxide and the energy bands in BP, thereby confirming the validity of our physics-based model. Our simulations show that around the flat band voltage $V_g \approx V_{NP}$ those defects in the upper band that are above E_F are positively charged, while the others are neutral (Figure 5a). During PBTI stress (Figure 5b), the Fermi level is shifted toward the conduction band, while band bending allows positively charged defects to emit holes and become neutral. Conversely, during NBTI stress, the number of positively charged defects becomes larger, since holes are captured from the valence band (Figure 5c). However, as was shown above, in the case of NBTI, the charge neutrality voltage shift measured using the full I_d−V_g sweeps is affected not only by the number of defects that have changed their charge state during stress but also by the sweep direction used. Therefore, since this issue is not accounted for in our TCAD simulations, the fits obtained for the PBTI recovery traces are considerably better than their counterparts for the NBTI traces (Figure 5d). A detailed qualitative interpretation of PBTI and NBTI for both sweep directions can be found in the SI (Figures S10 and S11). Also, since in our TCAD simulations we did not account for the high-k encapsulation of our BPFETs, the reasonable agreement with the measured BTI characteristics allows us to conclude that the properties of the Al_2O_3/BP interface do not have a considerable impact on our results.

Finally, we compare the hysteresis and BTI dynamics observed for our BPFETs with Al_2O_3 and double-layer (Al_2O_3/Teflon-AF) encapsulation. As shown in Figure 6a, the transfer characteristic of the device with double-layer encapsulation exhibits a considerably smaller hysteresis, especially in the hole conduction region. Moreover, the charge neutrality point voltage of this device is close to zero, which means that the additional Teflon-AF capping layer leads to a reduced number of charged defects (see Figure S1 in the SI). At

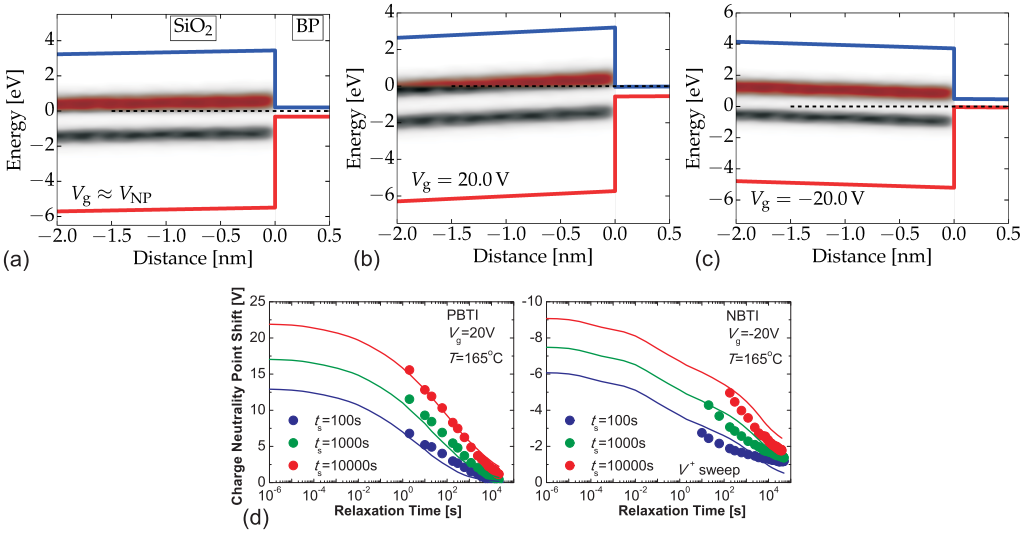

Figure 5. Simulated band diagrams for the channel cross-section of our BPFETs and the defect level allignment for (a) $V_g \approx V_{NP}$, (b) PBTI at V_g = 20 V, and (c) NBTI at V_g = −20 V. (d) Resulting fits of the recovery traces (lines express the results of our TCAD simulations, and symbols are for the experimental data) for PBTI (left) and NBTI (right).

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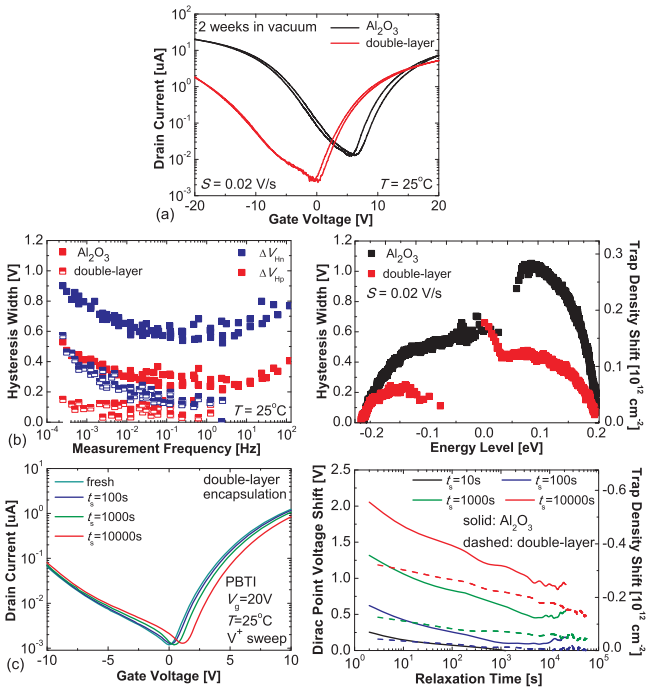

Figure 6. (a) Gate transfer characteristics of our BPFETs with Al_2O_3 and double-layer encapsulation. The charge neutrality point voltage of the device with double-layer encapsulation is close to zero. (b) Hysteresis width and the corresponding charge trap density shift measured for the device with double-layer encapsulation are considerably smaller. (c) The PBTI degradation observed for the device with double-layer encapsulation at T = 25 °C is smaller than for its counterpart with Al_2O_3 encapsulation.

the same time, the dependence of the hysteresis width *versus* the measurement frequency and energy distribution of the charge trap density shift (Figure 6b) exhibit similar trends for both devices, which allows us to ascribe this behavior to the properties of the BP/SiO_2 system rather than encapsulation. Namely, we observe a larger hysteresis when using slower sweeps, while ΔV_{Hp} is smaller compared to ΔV_{Hn}. However, the most essential finding is that the device with double-layer encapsulation exhibits an improved hysteresis stability within the whole range of measurement frequencies. Furthermore, the device with double-layer encapsulation exhibits smaller degradation under PBTI stress (Figure 6c) than its counterpart with Al_2O_3 encapsulation. Therefore, the use of Teflon-AF as an additional capping layer improves the overall reliability of BPFETs. We stipulate that this is due to Teflon-AF being an extremely hydrophobic fluoropolymer with a water contact angle exceeding 90°. Hence, it can protect Al_2O_3 layers from the diffusion of water molecules, which are known to act as trapping centers contributing to the hysteresis in MoS_2/SiO_2 FETs.[39] Additionally, Teflon-AF is understood to form a strongly polarized layer at the interface with 2D materials,[40,41] which may reduce the density of intrinsic impurities. This is in agreement with ref 15, where it has been shown that double-layer encapsulation improves the air stability of BPFETs.

CONCLUSIONS

In summary, we have performed the detailed analysis of the hysteresis stability of ambipolar BPFETs and reported the presence of both PBTI and NBTI in these devices. By using our experimental technique to benchmark the impact of fast traps on the device performance, we found that our encapsulated BPFETs are highly stable. The observed hysteresis behavior is well reproducible and remains almost independent of device aging and stressing. Furthermore, using Teflon-AF as an additional encapsulation layer considerably improves the device reliability with respect to hysteresis and BTI. However, at higher temperature both the hysteresis and BTI in our BPFETs become larger, due to the thermally activated nature of charge trapping. Of particular practical interest is the observation that in the p-conduction region of BPFETs the hysteresis is smaller, which can afford highly stable BP p-FETs to complement MoS_2 n-FETs in low-power circuits.

METHODS

Few-layer phosphorene samples were mechanically exfoliated onto 80 nm SiO_2/Si from bulk black phosphorus purchased from HQ Graphene. PMMA A4 was spin-coated and baked at 180 °C immediately after the exfoliation, in order to minimize air contact and degradation, as well as to serve as e-beam lithography resist. Target phosphorene flakes were selected to have a thickness of roughly <15 nm, according to color contrast under an optical microscope. A Carl Zeiss FENEON 40 SEM system was used for e-beam lithography to open the source/drain electrode area, followed by metal evaporation of a 4 nm Ti adhesion promoter layer and 40 nm Au. Right after lift-off in acetone for 2 h, 25-nm-thick Al_2O_3 was deposited by ALD at 150 °C, for both the Al_2O_3 and the double-layer encapsulation structure. For double-layer encapsulation, a 100-nm-thick DuPont Teflon-AF encapsulation layer was deposited on top of the Al_2O_3 layer by spin coating and annealing at 250 °C for 30 min in a nitrogen atmosphere. We note that bare BP samples were exposed to ambient air no longer than 1 h during the entire fabrication process, before deposition of the encapsulation layers.

All our measurements have been performed using a Keithley-2636A in a vacuum chamber at a pressure of 5×10^{-6}–10^{-5} Torr and at four different temperatures (T = −193, 25, 85, and 165 °C). In order to study the hysteresis in detail, we have measured the transfer characteristics of our BPFETs in both sweep directions using the sweep ranges −20 to 20 V, −20 to 0, and 0 to 20 V. At the same time, the sampling time t_{step} has been varied within the range of 0.2 and 500 ms and the step voltage V_{step} within 0.01 and 2 V, which corresponds to the sweep rates $S = V_{step}/t_{step}$ from as low as 0.02 V/s up to 10 000 V/s. For each of the measured I_d–V_g characteristics we extracted the hysteresis widths ΔV_{Hn} and ΔV_{Hp} around the threshold voltages in the electron and hole conduction regions, respectively. For a detailed understanding of the contribution of different traps to the hysteresis behavior, the dependences of these quantities on the measurement frequency $f = 1/(Nt_{step})$ with the number of voltage step points $N = 2((V_{gmax} - V_{gmin})/V_{step} + 1)$ has been analyzed at different temperatures. Also, we have studied the hysteresis widths extracted at different gate voltages.

The BTI degradation/recovery dynamics have been studied using subsequent stress/recovery rounds with increasing stress times at T = 25 and 165 °C. For a more reliable analysis, all our BTI experiments have been repeated using both V^+ and V^- sweep modes. Also, in accordance with our previous studies on GFETs, we express the BTI degradation magnitude in terms of the charge neutrality point voltage shift.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.6b04814.

Transfer characteristics of the same BPFET before and after encapsulation with Teflon-AF; reproducibility of the transfer characteristics at T = 165 °C; some details on the impact of aging and stressing on the hysteresis width and detailed results for NBTI degradation; qualitative

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interpretation of the experimental results for hysteresis, PBTI, and NBTI; simulated transfer characteristics (PDF)

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Notes

The authors declare no competing financial interest.

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