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Fabrication of scalable and ultra low power photodetectors with high light/dark current ratios using polycrystalline monolayer MoS_2 sheets

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ABSTRACT

During the last decade an unprecedented amount of funding has been invested on the study of the fundamental properties of two dimensional (2D) materials. Most of these studies have been mainly developed using research oriented techniques, such as mechanical exfoliation and electron beam lithography. Despite the large amount of information gained, these methods are not scalable, which impedes the mass production of electronic devices. The raising pressure for recovering the investment has shifted the global interest towards scalable routes of growing and manipulating the 2D materials, aiming to build up devices with realistic possibilities of commercialization. Here we show the fabrication of MoS_2 photodetectors using an entirely scalable process, which is based on chemical vapor deposition (CVD), photolithography, electron beam evaporator and plasma ion etching. The devices show strikingly low power consumption (3.25×10^{-9} W under illumination) and high light/dark current ratios (up to 170) which, to the best of our knowledge, are the best ever reported in the literature for MoS_2 phototransistors. These performances are related to the small domain size of the polycrystalline monolayer MoS_2 sheets (164 ± 54 nm in diameter). We also successfully minimized the hysteresis by introducing an annealing step during the fabrication process. The different parameters to be selected during the CVD growth process (precursor, gas carrier, pressure, temperature and time) offer a unique framework for tuning the properties of these devices. These results should be of interest to the entire community working on 2D materials based electronic devices.

1. Introduction

Two dimensional (2D) transition metal dichalcogenides (TMDs) have become very popular in many fields of science due to their superior physical and chemical properties [1,2]. In electronic device technology, 2D/TMD materials are interesting due to their semiconducting properties, and also because their large chemical stability allows withstanding large electrical stresses, enhancing the overall performance, reliability and lifetime [3,4]. Many combinations of transition metals and chalcogens can yield the three-atom-layer arrangement of a monolayer TMD, being the Mo and W families those that attracted most expectations, specially MoS_2. In the last years many exciting device prototypes based on atomically thin nanosheets of MoS_2 have been developed. Among them, field effect transistors (FET) [5], non-volatile memories [6], radio frequency circuits [4], prospective valleytronic devices [7], and photodetectors have attracted a lot of attention. Unfortunately, in most of these prototypes the 2D material has been obtained via mechanical exfoliation (probably because it is simple and ensures the largest quality), and the device electrodes have been patterned using electron beam lithography (EBL). While these methodologies provide a good path for scientific investigations, they are not suitable for wafer scale industrial production, as they are not scalable, i.e. the mechanical exfoliation method can only isolate flakes of hundreds of nanometers with inhomogeneous thicknesses, and EBL is too slow and costly for patterning an entire wafer. Therefore, establishing scalable processes to simultaneously fabricate large groups of 2D/TMD based devices with homogeneous size, structure and chemical composition is of utmost interest for this technology, not only form the scalability point of view, but also to ensure a low device-to-device variability.

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The most promising scalable methodology to produce large-area MoS_2 sheets is chemical vapor deposition (CVD). Different strategies have been developed to fabricate MoS_2 via CVD. For example, Zhan et al. [8] coated a wafer of SiO_2 with 1–5 nm of Mo, and introduced it in a tube furnace with a sulfur source. When the system was heated to 750 °C and a flow of 150–200 sccm N_2 gas was introduced in the furnace, the vaporized sulfur could react with the Mo film, forming MoS_2. Similarly, Jeon et al. [9] introduced a sulfur and a MoO_3 sources into a tube furnace, which could react together on the bare surface of the target substrate. The use of SiO_2 or sapphire substrates leads to a better quality of the MoS_2 sheets because their lattice constants match better than with other materials [10]. Integrated devices and circuits based on large area monolayer MoS_2 grown by CVD were fabricated by Wang et al. [11], who reported FETs with high mobility up to 40 $cm^2 V^{-1} s^{-1}$. Recent developments even achieved the growth of decent MoS_2 on other two dimensional materials, such as graphene [12,13] and hexagonal boron nitride [13], which makes the CVD technique even more attractive for scalable and fully 2D device development.

It should be highlighted that when using CVD processes the resulting MoS_2 sheets are normally polycrystalline, which introduces large amounts of defects at the grain boundaries (GBs), i.e. missing atoms and pentagonal/heptagonal lattices, reducing the overall carriers mobility. The grain size depends on the growth parameters, i.e. type of precursor [14], gas flow [15] (which tunes the amount of precursor seeds transferred to the target sample), temperature and substrate used [10,16,17]. For example, in reference [9] the authors present the growth of large-area (continuous) monolayer MoS_2 sheets with grain sizes ranging between 50 nm and 20 μm (in diameter). Moreover, the number of layers in the CVD-grown MoS_2 stack (which also has a remarkable effect on the material properties) can also be controlled by changing these parameters. Therefore, despite in several device applications (including FETs operating at high frequencies) single-crystalline sheets with high mobility are preferred [11], the CVD method provides a unique path for fabricating devices with tunable characteristics, which may be very interesting for several devices, including photodetectors and low power applications. Here we demonstrate the development of an array of MoS_2 photodetectors using only scalable techniques, that is, CVD for material growth, photolithography plus electron beam evaporator for the deposition of electrodes, and plasma ion etching for patterning the channels. The devices show high light/dark current ratios up to 170 and ultra low power consumption (3.25×10^{-9} W under illumination). We achieve to reduce the currents (and therefore the power consumption) by growing monolayer MoS_2 sheets with small grain sizes of 164 ± 54 nm. To the best of our knowledge, the performances of these devices are the best found in the literature [18–20], with the added advantage that we used cheaper, faster and scalable fabrication techniques. These results may serve as a reference for the design of low power photodetectors made of 2D/TMDs materials.

2. Device fabrication

The device configuration selected to carry out the photodetection has been that of a single back-gate FET with a MoS_2 channel, which can change the output current when exposed to illumination. Our fabrication process is described in Fig. 1. A continuous monolayer of MoS_2 has been grown by CVD on a 300 nm SiO_2/Si wafer at the laboratories of Gelanfeng Ltd. using the parameters previously employed by Yu et al. [21]. The good quality of the MoS_2 sheets grown using this process has been previously demonstrated using a transmission electron microscope, which shows good hexagonal lattice [21], as well as by atomic force microscopy (AFM) and Raman spectroscopy images, as it will be discussed later. We recall that the MoS_2 sheets grown using this method are polycrystalline with an average grain size of 164 ± 54 nm in diameter, as will be discussed later.

After the CVD growth, matrixes of squared 100 μm×100 μm top electrodes consisting of 10 nm Ti and 50 nm Au stacks have been evaporated on the MoS_2 sheet via photolithography (Fig. 1b), electron beam evaporation (Fig. 1c) and lift-off (Figs. 1d and 2a). Before patterning the channels of the transistors, the conductivity of the MoS_2 sheet has been evaluated in a Cascade probestation connected to a Keithley 4200 semiconductor parameter analyzer (SPA). All the electrical measurements during the fabrication process have been performed under air atmosphere and room light. When measuring between two electrodes of the sample, the distance between them and the electrode width could be roughly considered as the effective channel length (L_{eff}) and width (W_{eff}) (respectively) [21]. Fig. 2b shows the output characteristic (drain-source current vs. drain-source voltage, I_{DS}–V_{DS}) measured between two electrodes separated by a length of 40 μm (numbers 1 and 5 in Fig. 2a). As it can be observed, the currents measured are very low, reaching a maximum of 1 nA when the potential difference applied is around 9 V. This is a consequence of the small grain sizes of the MoS_2 sheets used in this investigation, and we discard that the low currents are related to problems during the fabrication process because our values are comparable to those reported previously by others using similar MoS_2 samples [21]. Fig. 2b also shows the currents measured in reference [21] using larger electrodes (W_{eff}=230 μm) separated by a smaller distance (L_{eff}=30 μm). As it can be seen, the currents are of the same order of magnitude, with the differences being consistent with the different geometries of the devices. Fig. 2c shows the transfer characteristics (drain-source current vs. gate voltage, I_{DS}–V_G) measured between the same two electrodes at different voltages, in which a large hysteresis can be observed.

A second photolithography step has been used to pattern the MoS_2 channels between each pair of electrodes within the matrix; the pair of electrodes connected by a channel are 1 and 5, 2 and 6, 3 and 7, and 4 and 8 of Fig. 2a. Therefore, the conductivity between electrodes 1 and 2 (for example), should be negligible. In order to ensure the correct removal of the unwanted MoS_2 (out of the channel region) a mask that keeps the center of the electrodes exposed has been used (i.e. the photoresist has been deposited on top of the channel and on the edges of the electrodes, but the center of the electrodes could still be electrically contacted with the tips of the probestation, see Fig. 1e). After that the sample has been exposed to O_2/Ar plasma for 5 s with the aim of etching the MoS_2 out of the channel region (not protected by the photoresist), and the conductivity between electrodes 1 and 2 (in Fig. 2a) has been measured under room light without removing the photoresist. After only 5 s of etching we observed that the current flowing between them was not negligible (see Fig. 3a), indicating that the MoS_2 out of the channel region was not fully removed. Then, the sample has been exposed to an O_2/Ar plasma etching step for 5 additional seconds, and the current has been measured again. This process has been repeated several times until the current between electrodes 1 and 2 was negligible, proving the correct isolation of each transistor (see Fig. 1f). Fig. 3a clearly shows that the currents decrease with increasing plasma etching time and also that the necessary time for complete MoS_2 removal using the O_2/Ar plasma was 25 s, as after that time an increase of the time did not result in a further reduction of the current. By changing the speed of the current vs. voltage (*I-V*) curve we prove that the remaining currents are related to the displacement current of the probe station setup (Fig. 3b). In contrast, when the same ramped voltage stress (RVS) has been applied between two electrodes connected by a channel (electrodes 1 and 5 in Fig. 2a), larger currents of hundreds of picoamperes have been detected (see Fig. 3c), corroborating the correct fabrication of the devices. After that, the photoresist was removed in an acetone bath (see Fig. 1g and h). The novel strategy used here to determine the exact etching time of the MoS_2 is of utmost importance because the use of too long times would damage the edges of the MoS_2 channel (even if protected by the photoresist), while too short times may lead to short circuits between different devices.

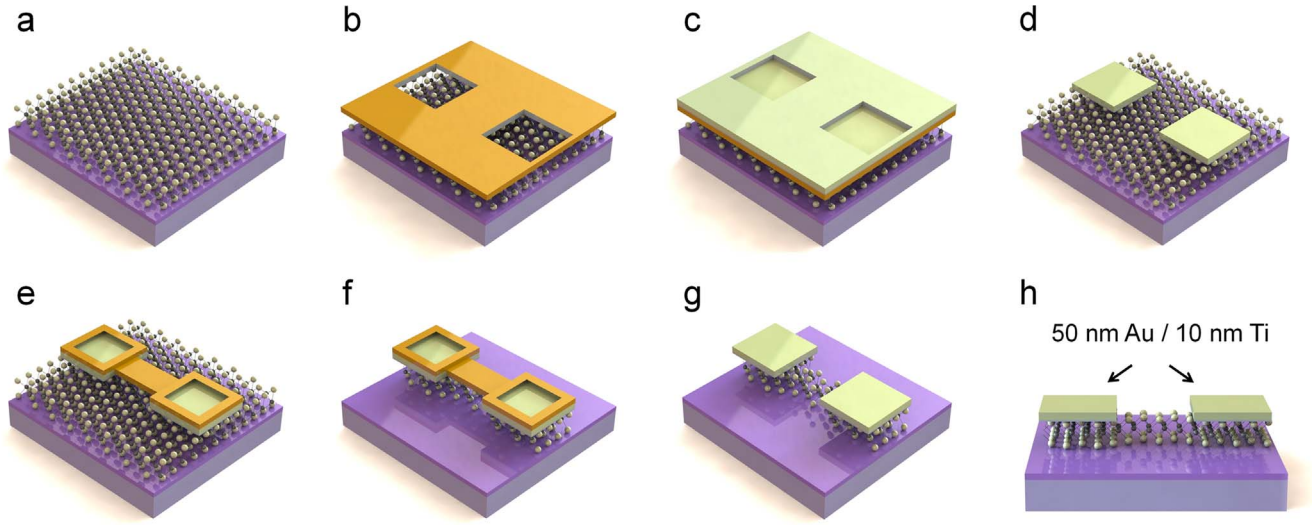

Fig. 1. Schematics depicting the fabrication process of a MoS_2 photodetector: (a) CVD grown MoS_2 on the SiO_2/Si substrate; (b) after first photolithography; (c) after deposited 10 nm Ti/50 nm Au by e-beam evaporation; (d) after lift-off; (e) after second photolithography; (f) after plasma etching; (g–h) after removal of the photoresist.

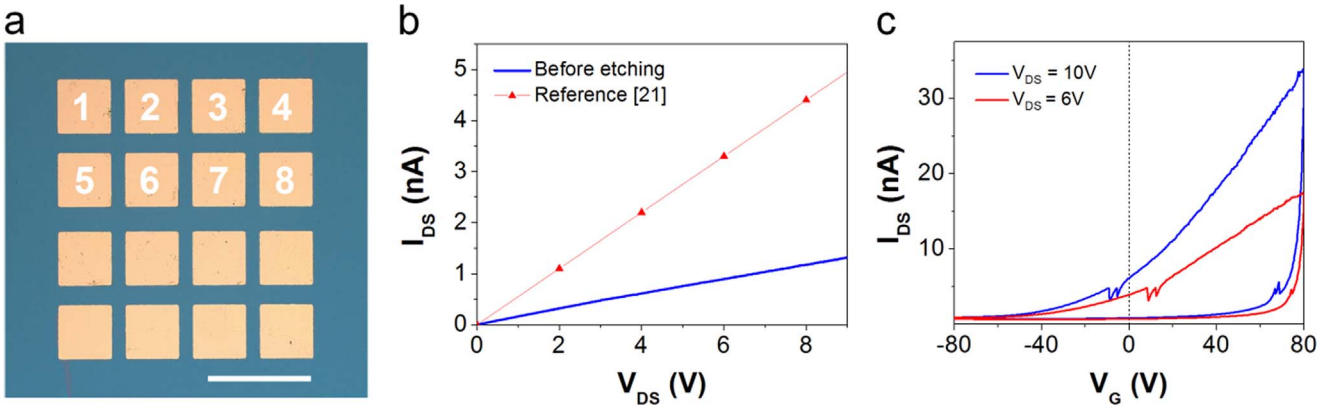

Fig. 2. (a) Optical image of the surface of the MoS_2/SiO_2 sample after patterning the electrodes (step shown in Fig. 1b). The scale bar is 200 μm. (b) Output characteristics before patterning the channels measured in: *i)* between electrodes 1 and 5 of (a), using devices with L_{eff}=40 μm and W_{eff}=100 μm, and *ii)* Ref. [21], using a similar MoS_2 and electrodes that form transistors with L_{eff}=30 μm and W_{eff}=230 μm. (c) Transfer characteristic measured between electrodes 1 and 5 of (a). V_{DS} and I_{DS} refer to the voltage applied and current measured between electrodes 1 and 5 (respectively), and V_G is the voltage applied to the bottom of the sample.

The channel length of all the devices fabricated was the same (40 μm), but three different widths of 5 μm, 10 μm and 20 μm were used (see Fig. 4a, b and c). The thickness of the MoS_2 channel was corroborated by AFM (Fig. 4d), which shows a typical value of ~ 0.85 nm. This value is in line with previous observations and corresponds to the thickness of the MoS_2 sheet (~0.65 nm) plus the separation to the SiO_2 substrate [22,23]. The morphology of the samples was analyzed by scanning electron microscopy (SEM) and Raman spectroscopy. Fig. 4c and d show that the channels are continuous, and the Raman map of the A_{1g} peak (centered between 403 and 410 cm^{-1}) further corroborates the good quality of the MoS_2, as well as the successful pattern of the channel.

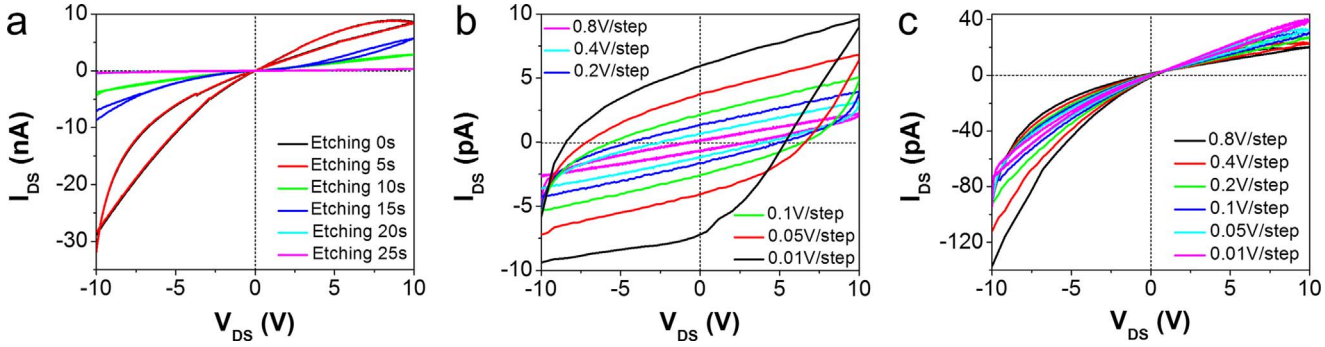

Fig. 3. (a) Currents measured between electrodes that will belong to different transistors (electrodes 1 and 2 in Fig. 2a) after different etching times. The reduction of current between them indicates that the transistors are correctly isolated from each other after 25 s of etching. (b) Currents measured between electrodes that will belong to different transistors (electrodes 1 and 2 in Fig. 2a) after 25 s of etching and using different step sizes (speed) for the voltage bias sweep. (c) Currents measured between electrodes that will belong to same transistors (electrodes 1 and 5 in Fig. 2a) after 25 s of etching and using different step sizes (speed) for the voltage bias sweep.

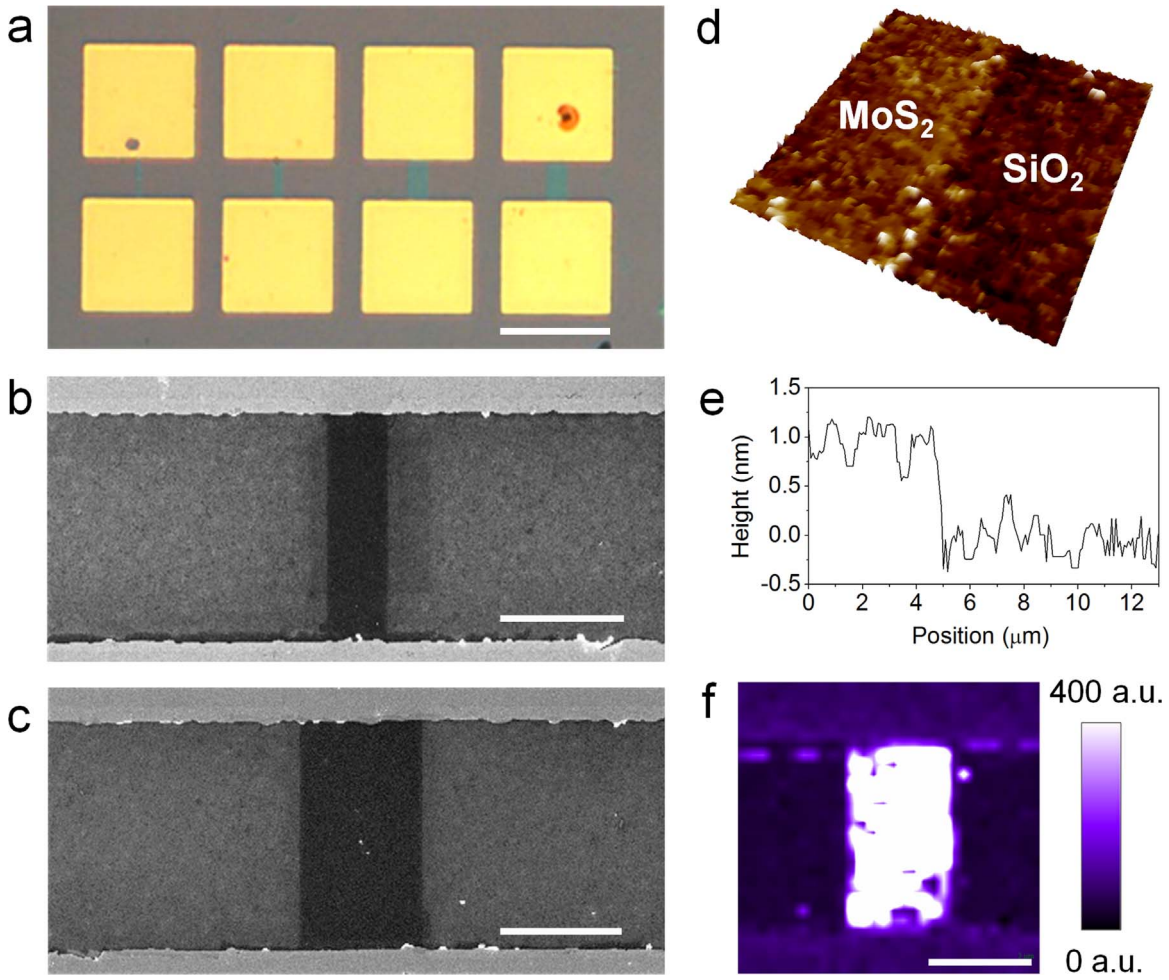

Fig. 4. (a) Optical microscope images of photodetectors after fabrication. (b) and (c) show the SEM images of channels with widths of 10 μm and 20 μm (respectively). (d) and (e) show the 8 μm×8 μm AFM map and cross-section collected at the edge of the MoS_2 channel (respectively), demonstrating that the MoS_2 sheet is a monolayer (e) Raman map of the A_{1g} peak (centered between 403 and 410 cm^{-1}). The scale bars are 100 μm in (a), 20 μm in (b), (c) and (f).

3. Electrical characterization

After fabrication, the performance of the devices when operated as photodetectors has been evaluated under artificial room light illumination. The output characteristic of all devices has been obtained using different back-gate voltage biases (V_G) ranging from −80 to 80 V in steps of 20 V (see Fig. 5). Remarkably, an almost linear dependence between I_{DS} and V_{DS} as well as a quasi-symmetry has been observed for all the devices. For the devices with a 20 μm channel width, the output characteristics for positive and negative voltages are perfectly symmetric with respect to the origin of the coordinate system, which leads to the assumption that decent ohmic contacts between the electrodes and the MoS_2 channels have been formed [5,21,24–26]. The symmetric shape of the I_{DS}–V_{DS} curves, as well as the increasing nature of I_{DS} with V_G (shown in Fig. 5) are very similar to those previously reported for single back-gate devices fabricated using *i)* mechanically exfoliated MoS_2 nanosheets (both monolayer and multilayer) with electrodes patterned by EBL [5,24], *ii)* CVD-grown MoS_2 sheets and electrodes patterned by EBL [18] and *iii)* CVD-grown MoS_2 sheets and electrodes patterned by photolithography [17], confirming the correct fabrication of our FETs. The only remarkable difference between all these works is the magnitude of I_{DS}, which is strictly related to the MoS_2 synthesis process.

Using the same setup and measurement parameters (voltage sweep step and speed) the transfer characteristics of each device have been collected at nine different V_{DS} (−5 V, −3.5 V, −2 V, −0.5 V, 0 V, 0.5 V, 2 V, 3.5 V, 5 V). Fig. 6 left and right columns show the obtained plots for the devices with channels of 10 μm and 20 μm (respectively) under illumination (top row) and in the dark (bottom row). The gate voltage was ramped from −80 V to +80 V, and both forward and backward curves have been plotted. As it can be seen, for all the devices the currents are much larger under illumination, thus confirming the photodetection capability of our MoS_2 devices. It should be highlighted that all the plots show *n*-type transistor behavior, as the drain current increases exponentially when positive voltage is applied to the back gate (under positive V_{DS}) [5,27]. At the same time, a large hysteresis between the forward (V_G from −80 to 80 V) and backward (V_G from 80 V to −80 V) sweeps can be observed, which is larger when the measurements are collected in the dark, i.e. the area (*A*) enclosed between the forward and backward curves is larger in the dark. This large hysteresis, which has been previously reported by Li et al. [24], is likely related to the effect of oxygen and water molecules absorbed on the MoS_2 channel of the FETs [18,28–30].

As the hysteresis is an unwanted effect which may disturb the correct functioning of the devices, we annealed the samples at 300 °C for 2 h under vacuum atmosphere (0.57 Torr) in order to reduce/remove the environmental moisture. After that, the devices have been immediately characterized in the dark and under flash light illumination (3 mW/cm^2) using a shielded Lakeshore probe station working under a vacuum of ~10^{-5} Torr (also using the Keithley 4200 SPA). Fig. 7a and b show the transfer characteristics for the devices with channel widths of 20 μm before and after annealing. Despite the currents under illumination cannot be compared due to the different light sources, the measurements in the dark reveal that after annealing

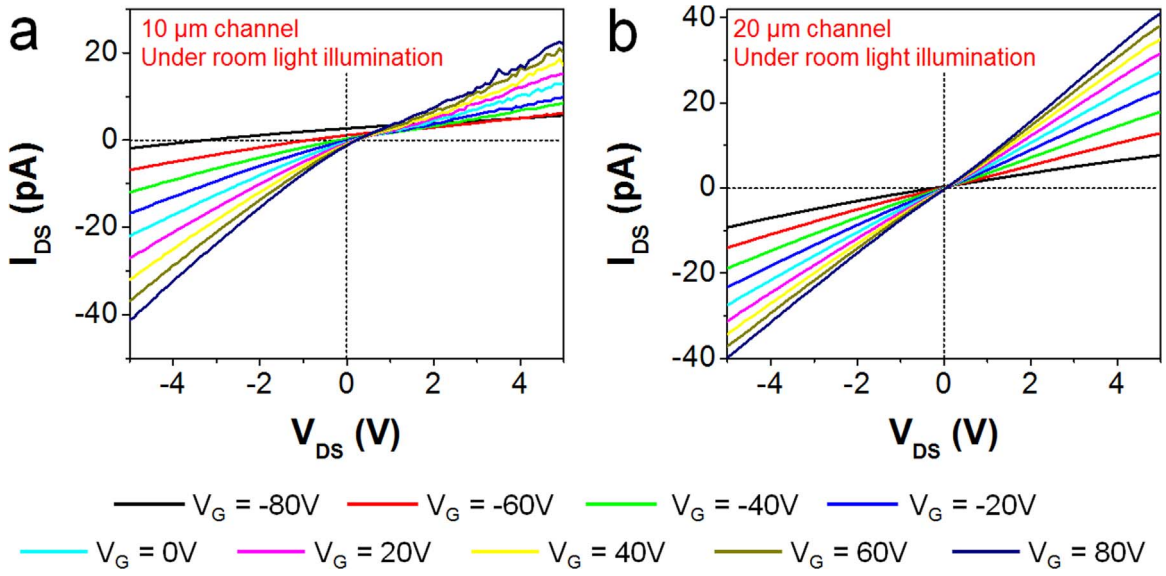

Fig. 5. Output characteristic at different back-gate voltages for the MoS_2 transistors with channel widths of 10 μm (a) and 20 μm (b).

the hysteresis in the system is remarkably reduced, and the currents increased by a factor of 3.3, probably due to the lower scattering at the channel region after moisture removal. The annealing favors the removal of adsorbates, which has been proved to change the doping of the MoS_2 by shifting the Fermi level towards the conduction band [31]; moreover; the anneal also significantly reduces the contact resistance with the electrodes [31]. The hysteresis observed in the dark after the anneal (black curve in Fig. 7b) is strikingly small. This

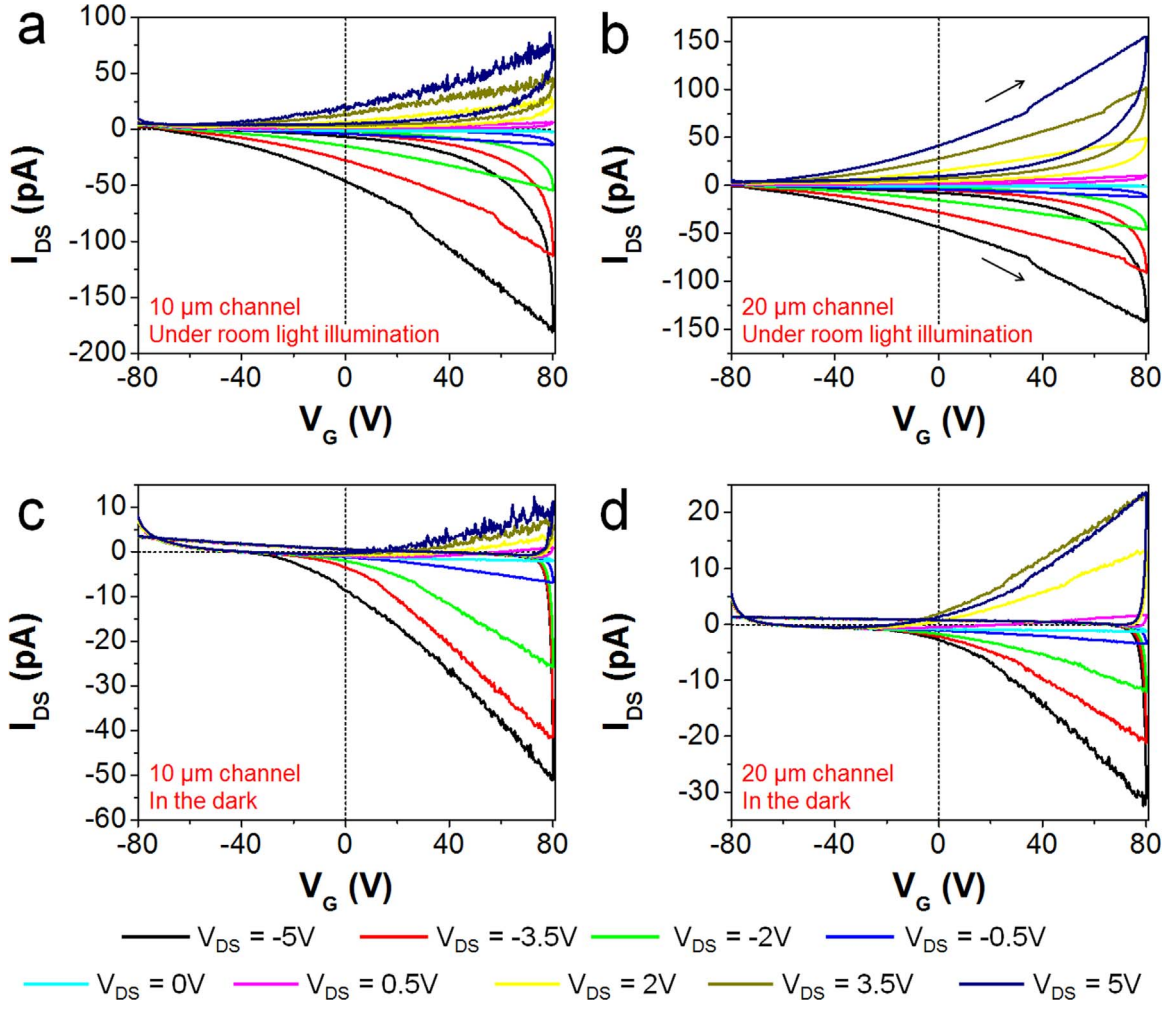

Fig. 6. Transfer characteristics for the MoS_2 photodetectors with channel widths of 10 μm (a and c) and 20 μm (b and d). The top (a and b) and bottom (c and d) rows show the transfer characteristics under illumination and in the dark (respectively). For each test, V_G was ramped from −80 V to +80 V, and the forward and backward curves are displayed.

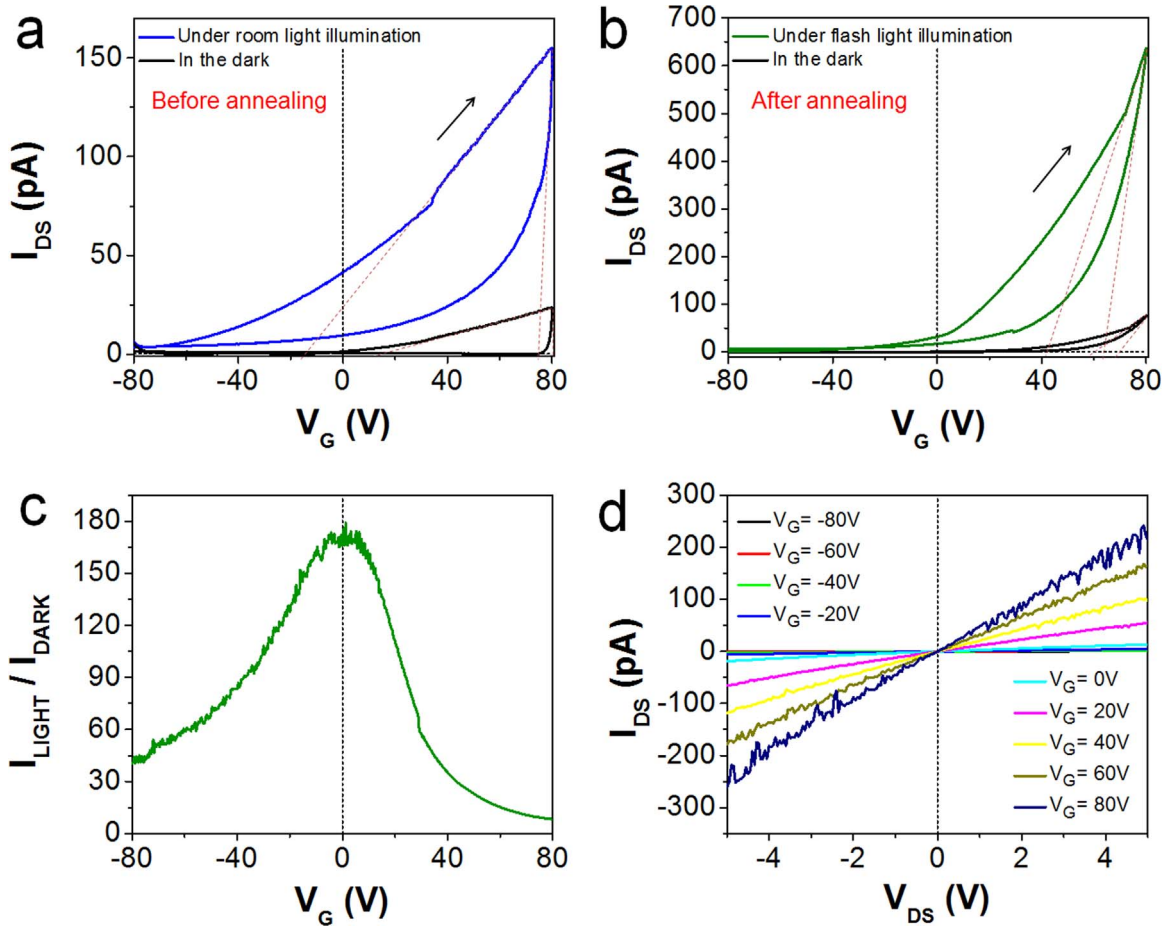

Fig. 7. Transfer characteristics measured at V_{DS}=5 V for the device with a 20 μm wide MoS_2 channel (a) before annealing (in the dark and under room illumination) and (b) after annealing (in the dark and under 3 mW/cm^2 flash light illumination); (c) Voltage dependent light/dark current ratio calculated for the device shown in panel (b), using the backward curves. (d) Output characteristics measured under illumination for the device with a 20 μm wide MoS_2 channel after annealing.

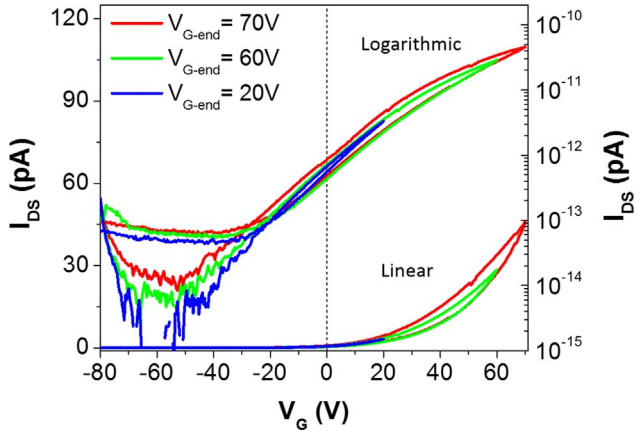

Fig. 8. Transfer characteristics measured in the dark for the device with a 20 μm wide MoS_2 channel after annealing, using different $V_{G\text{-}end}$=70 V, 60 V, 20 V. The V_{DS} used is 0.6 V.

behavior has been analyzed more deeply by varying the end voltage of the ramp applied to the gate ($V_{G\text{-}end}$). Fig. 8 shows the transfer characteristics of a MoS_2 device with a channel width of 20 μm, using $V_{G\text{-}end}$ values of 70, 60 and 20 V, where both forward and backward curves are plotted. As it can be observed, despite the different voltage sweeps applied, the devices show a very small hysteresis, which is similar for all the tests. Thus, these results confirm the almost complete removal of the scaling behavior of hysteresis previously observed in other works [24]. On the other hand, by comparing Figs. 7d and 5b it can be concluded that the currents measured after annealing are one order of magnitude lager than before and that the symmetry of the plot is also significantly improved.

As shown in Fig. 7a and b, the hysteretic behaviors of the as-fabricated and annealed samples are different depending on the illumination conditions. Before the annealing, the hysteresis is larger in the dark, while after the annealing a larger hysteresis is detected under illumination. Nevertheless, in both cases our MoS_2 devices show a significant photosensitivity. A typical current light/dark ratio (I_{LIGHT}/I_{DARK}) after annealing is plotted in Fig. 7c. As can be observed, the plot is nearly symmetric, reaching a maximum of 170 at V_G=0 V. To the best of our knowledge, this is the highest value ever reported in the literature (see Table 1 in the Supplementary Information, SI).

Another advantage of our devices compared to previous prototypes is the ultra low power consumption, which can be observed by the sub-nanoampere values of I_{DS}. From the transfer characteristic (Fig. 7b) the maximum I_{DS} (637 pA) is obtained at the maximum V_G (+80 V), and when multiplied by the V_{DS} applied (5 V), a maximum power consumption of 3.25×10^{-9} W under illumination is obtained. This value is strikingly smaller than those previously reported (see Table 1 in SI). The reason behind this behavior may be the small size of the domains in the MoS_2 sheets, which could lead to several GBs that reduce the total current in the channel. It is known that GBs in MoS_2 can contain sulfur vacancies [32] and lattice disorder form adsorbates [26,31,33–35], which will serve as traps for the charge carriers and reduce the overall current along the FET channel. Sangwan et al. [36] recently reported that the conductivity along the MoS_2 channel of a

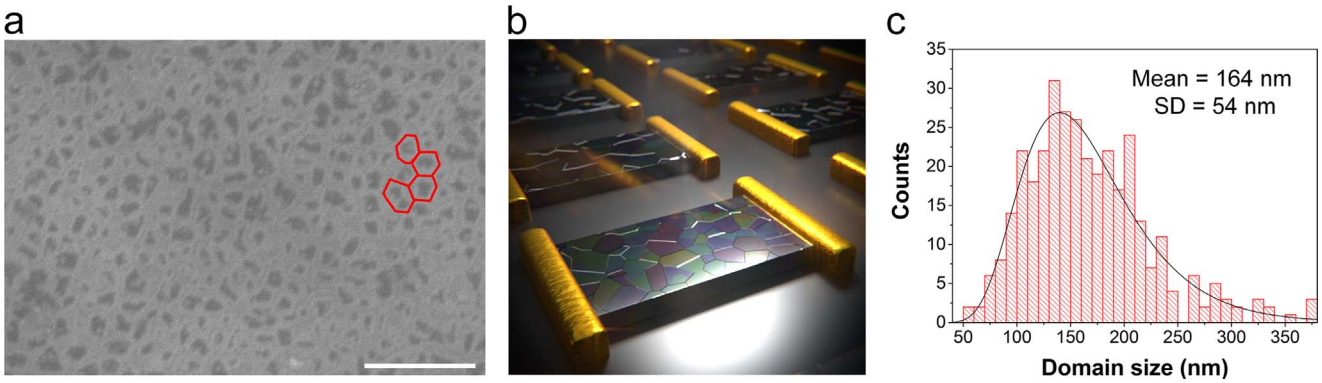

Fig. 9. (a) SEM image of the channel region after a 5 h long annealing at 300 °C in a vacuum of 0.57 Torr. The scale bar is 600 nm. This destructive treatment is useful for identification of the grain size in the MoS_2 sheets (highlighted in red). (b) Schematic representation of the matrix of phototransistors with polycrystalline MoS_2 channels. For clarity, the electrodes have been depicted rectangular instead squared. (c) Statistical analysis of the size of 320 domains (SD means standard deviation). The fitting corresponds to a lognormal distribution.

single back-gated FET can experience changes above one order of magnitude by altering just a few GBs boundaries within the channel. To corroborate this hypothesis, we evaluate the size of the grains in the MoS_2 sheets. GBs in 2D materials have been previously visualized with transmission electron microscopy [21], and if the material is conductive they can be also observed by scanning tunneling microscopy [37]. It should be highlighted that evaluating the size of a grain in the MoS_2 sheet by visualizing the entire GB that surrounds it is not doable, given the large area of the grain and the small area of the GB (i.e. to the best of our knowledge, this has never been reported). In our previous work [38,39] we kept a graphene/Cu stack exposed to air environment at room temperature, and we observed that after a few days oxygen atoms from the environment can bond at the defects of the 2D sheet. Since the defects in the 2D sheet are mainly concentrated at the GBs, this made possible their visualization by lower resolution techniques, such as AFM and SEM [38,39]. The use of other oxidative treatments (like soaking in H_2O_2) is nowadays widely used to evaluate the size of the GBs in 2D materials grown by CVD [38,39]. Following this strategy, we exposed the MoS_2 channels of our devices to air environment at room temperature during two weeks; the SEM images of the channels (Fig. S1 in SI) show a large density of white spots corresponding to absorbates on the surface of the MoS_2 [38,39]. Interestingly, these particles are not randomly distributed, but follow geometrical shapes surrounding areas with diameters between 100 and 200 nm. This behavior can be much better observed after doing a thermal anneal at 300 °C for 5 h. As the GBs in MoS_2 are defective locations, they offer less mechanical resistance leading to a faster damage and/or fracture due to the high temperatures. This allows to quantify the sizes of the domains very clearly, as displayed in Fig. 9a. By using the software Nano Measurer (version 1.2), we statistically analyze the size of more than 320 domains in this image, and find an average size of 164 ± 54 nm (see Fig. 9c). These values are considerably smaller than the grain size reported in other works (typically between 10 and 20 μm) [15,16,40], which could explain the strikingly low power consumption of our MoS_2 photodetectors. Therefore, the CVD approach can serve as a very useful methodology to achieve tunable MoS_2 device properties. It should be noted that another factor that may contribute to the low currents measured is the large channel length (L=40 μm), which is much larger than in other reports, as the number of GBs increases with the channel length.

In this investigation, more than 20 devices have been tested, and similar results have been obtained. Future works in the field of MoS_2 devices should include profound variability analyses, time-dependent variability studies, as well as the encapsulation of MoS_2 channels using also scalable methods. In the case of phototransistors, the encapsulating materials should be not only moisture resistant but also transparent.

4. Conclusions

Matrixes of MoS_2 photodetectors with ultra low power consumption (3.25×10^{-9} W under illumination) and high light/dark current ratios (up to 170) have been successfully fabricated using exclusively scalable techniques, i.e. CVD for 2D material growth and photolithography, electron beam evaporation for deposition of metal and plasma ion etching for channel patterning. Mechanical exfoliation and electron beam lithography have been intentionally avoided. The low power consumption is related to the small grain size of the MoS_2 used (164 ± 54 nm in diameter), which has been statistically proved by analyzing more than 320 domains. To the best of our knowledge the power consumption and light/dark current ratios are the lowest and highest reported in the literature (respectively). We also managed to reduce the hysteresis of our devices using an annealing step (2 h at 300 °C in a vacuum of 0.57 Torr). The CVD method used to grow the monolayer MoS_2 sheets allows tuning the properties of the devices, which can be very useful in different technologies.

Acknowledgements

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Appendix A. Supplementary material

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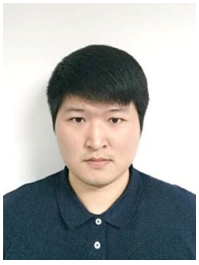

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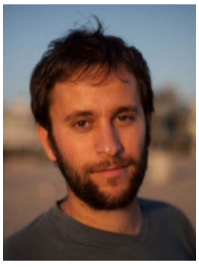

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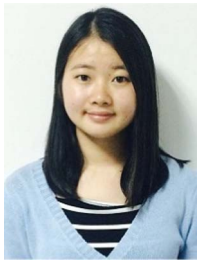

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