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The defect-centric perspective of device and circuit reliability—From gate oxide defects to circuits

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ABSTRACT

As-fabricated (time-zero) variability and mean device aging are nowadays routinely considered in circuit simulations and design. Time-dependent variability (reliability-related variability) is an emerging concern that needs to be considered in circuit design as well. This phenomenon in deeply scaled devices can be best understood within the so-called defect-centric picture in terms of an ensemble of individual defects. The properties of gate oxide defects are discussed. It is further shown how in particular the electrical properties can be used to construct time-dependent variability distributions and can be propagated up to transistor-level circuits.

1. Introduction

Variability of as-fabricated (i.e., time-zero) parameters of modern VLSI devices has been considered in circuit design tools for some time (Fig. 1a). With the exception of Time-Dependent Dielectric Breakdown (TDDB) [1,2], circuit lifetime estimation due to Field-Effect Transistor (FET) gate-oxide degradation (aging) mechanisms is presently based on projecting only the *mean* parameters shifts (Fig. 1b) [3]. The combination of both hitherto orthogonal efforts used in determining circuit operating margins is illustrated in Fig. 1c.

It has long been accepted that in mechanisms associated with FET *gate* current, such as Stress-Induced Leakage Current (SILC) and TDDB, only a handful of defects will cause significant current increases and can bridge the gate oxide, presently ~1 nm thick. Similarly, as lateral dimensions of VLSI devices are reduced toward the 10 nm range, just a few stochastically-behaving defects present in the FET gate oxide will have a sizable impact on the *drive* current as well. These phenomena result in additional, *time-dependent* variability in deeply-scaled devices, and their manifestation in the form of Random Telegraph Noise (RTN) has been extensively studied by many groups [4–13]. Here we build upon those observations and show how the same, physics-based considerations give rise to a new, *statistical* perception of other gate-oxide degradation mechanisms, such as Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI) [14–16]. This paradigm shift is illustrated in Fig. 2.

Since only a handful of defects (cf. $N_T = 12$ in Fig. 2b) will be responsible for the time-dependent effects in each deeply-scaled device, we maintain that understanding of degradation mechanisms at the level of individual defects is essential for simulations of time-dependent variability in circuits. This notion is indeed the basis of the so-called *defect-centric* picture and is hierarchically illustrated in Fig. 3. After defining basic variability terms, we review the properties of individual defects and show how to propagate these properties to higher hierarchical levels. We formalize the statistical description of time-dependent distributions (Fig. 1e) into simple equations and point out the parallels with time-zero variability. To estimate the full device and circuit parameter distributions at the end of useful lifetime, time-zero and time-dependent statistics have to be combined, as illustrated

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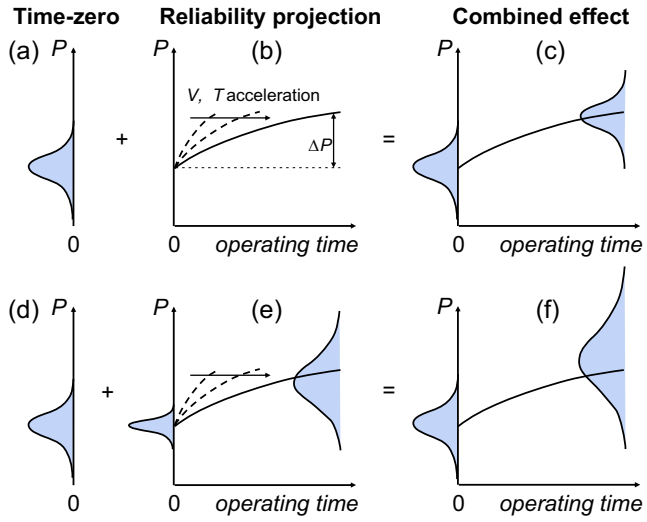

Fig. 1. A schematic representation of time-zero and time-dependent effects considered in circuit design. (a–c) Presently, time-zero variability of a device parameter P is considered together with the projection of the *mean* parameter shift ΔP (obtained by reliability engineers through bias and temperature accelerated tests) during aging. (d–f) Time-dependent variability is also considered, in contrast to (a–c).

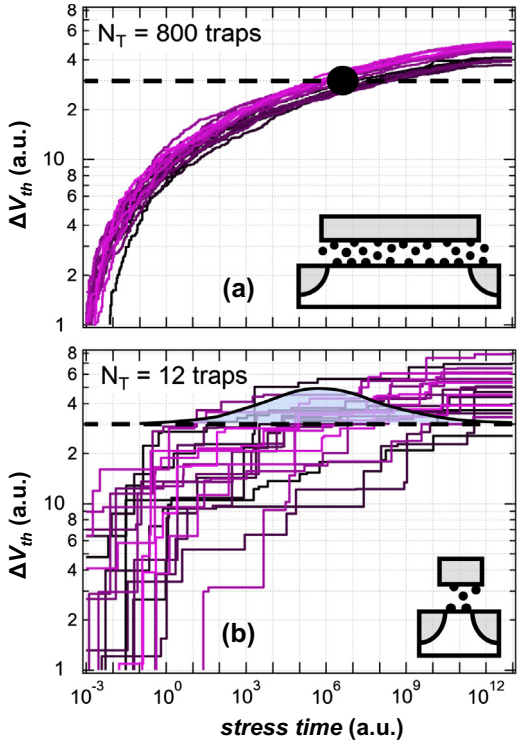

Fig. 2. (a) The random properties of many defects N_T in large devices average out, resulting in a well-defined lifetime while (b) the stochastic nature of a handful of defects in deeply-scaled devices becomes apparent, resulting in large variation in the lifetime. This also illustrates the paradigm shift in projecting reliability in deeply scaled devices (Fig. 1b and e) [17].

in Fig. 1d–f. Finally, we discuss how the combined variability can be propagated to and simulated at the circuit level.

2. Device variability

We refer to as-fabricated, *time-independent,* or *static,* device-to-device variability, as *time-zero* variability. *Time-dependent,* or *dynamic,* variability then refers to all variability due time-dependent effects. In this work, this is limited to effects due to defects (traps) present in FET gate dielectrics. The main emphasis of this Section is developing the time-dependent variability within the defect-centric picture. This is done Section 2.2. Subsections thereof then discuss the properties of individual traps (Section 2.2.1), both temporal and electric, the statistics of multiple traps (Section 2.2.2), and the experimental methods to characterize time-dependent variability (Section 2.2.3). The complete distribution (Section 2.3) is constructed from time-dependent variability and time-zero variability, discussed next.

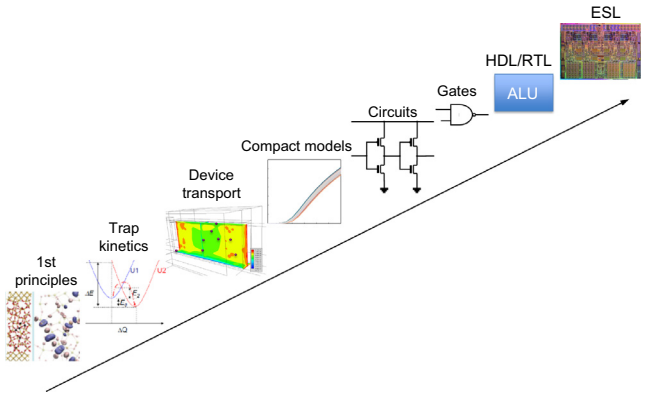

Fig. 3. Hierarchical levels of the defect-centric picture: Understanding of defect properties at the atomic level [18] can be propagated up to circuit design.

2.1. Time-zero variability

As-fabricated, i.e., time-zero variability, both systematic (process-induced) and random, is a well-known phenomenon in deeply-scaled VLSI technologies [19,20]. For example, the time-zero threshold voltages V_{th0} are assumed to be normally-distributed with mean $\langle V_{th0} \rangle$ and variance σ^2_{Vth0} [21]. Disregarding edge effects, the random component of σ^2_{Vth0} scales as

$$\sigma^2_{Vth0} \simeq \frac{A^2_{Vth}}{A_G} \tag{1}$$

where A_{Vth} is a scaling factor and A_G the total channel area [22,23]. It should be noted that some variation-inducing effects, such as Line-Edge Roughness, will result in a departure from this ideal scaling rule in deeply scaled devices [24].

A large number of nominally identical devices need to be typically measured to establish A_{Vth}, while organization of devices into matched pairs or local arrays is used to separate the systematic and the random components [25].

2.2. Time-dependent variability

Similarly to time-zero variability, time-dependent variability also has random and systematic components [25–28]. Because of the limited number of gate-oxide defects N_T present in modern deeply downscaled FETs (e.g., $N_T = 10$ with defect density $10^{12}\,\mathrm{cm}^{-2}$ and $A_G = W \times L = 100 \times 10\,\mathrm{nm}^2$), other degradation mechanisms, such as RTN/BTI and HCI will be distributed as well [14,16,29]. Based on this simple fact we claim that *the time-dependent variability in deeply scaled devices can be best understood in terms of an ensemble of individual defects and their time, voltage, and temperature dependent properties.* This is indeed the underlying foundation of the defect-centric approach. To develop this approach further, we now discuss some of the relevant properties of individual defects.

2.2.1. Properties of individual defects

The properties of each gate oxide defect (trap) are formed by the spatial location of the defect in the FET gate insulating layer, as well as the immediate configuration of atoms around it [18]. Because of the amorphous nature of the presently-used gate dielectrics, each defect will have substantially different structural properties, such as the ground level and the relaxation energy [30–32].

All these properties will then project into two main classes of parameters usable at higher abstraction levels, namely (a) the defect time constants (temporal) and (b) the defect impact on the FET parameters (electrical). An illustration of a distribution of these properties for two distinct defects in a deeply-scaled device is given in Fig. 4.

2.2.1.1. Temporal defect properties. The defect time constants τ_c and τ_e are the *mean times* for the gate defect to *capture* and *emit* a carrier. In addition, each capture and emission event will be stochastic and exponentially *distributed* around the respective mean value (cf. spread in individual emission times in Fig. 4). The values *of* τ_c and τ_e vary drastically from defect to defect, from at least tens of ns to years, based on the abovementioned defect structural and spatial (depth and lateral) properties, bias and temperature. *Distributions* of τ_c and τ_e can be inferred from a simulation of the FET device (Fig. 5) assuming distributions of the structural and spatial properties of the defects within the Non-radiative Multi-Phonon (NMP) theory [9,35]. The extracted distributions of τ_c and τ_e at varying gate voltages (for a given temperature, Fig. 6b and c) then allow to conveniently describe both RTN at any given *fixed* bias (Fig. 6a) [10] and BTI (stress and relaxation) at *arbitrary* biases. If the gate bias varies between two levels, e.g. 0 and the circuit supply voltage V_{DD}, as is the case in digital circuits, the τ_c^H at high bias (stress) and τ_e^L at low bias (relaxation) form the so-called Capture/Emission Times (CET) map (Fig. 6d) [37].

Encoding the BTI degradation in the form of a CET map allows to conveniently project the degradation of any device. The trap occupancy map (Fig. 6e) can be calculated in the same space for an arbitrary digital workload applied to the gate of the device. Analytic solutions exist for constant and periodic signals [40,41]. An algorithm has therefore been developed to partition an arbitrary workload signal into a sequence of constant and periodic phases [41], facilitating the occupancy calculation. The trap occupancy map is then convoluted with the CET map (Fig. 6d), yielding the occupied number of traps in the particular device [39,40].

The concept of time constants characterizing individual traps can be easily extended to defect generation, e.g. by assuming additional time to convert a precursor site into a trap [42].

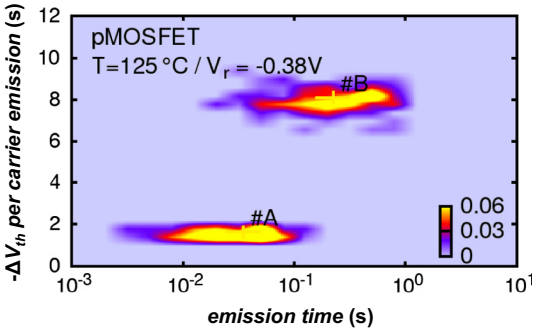

Fig. 4. An example of Time-Dependent Defect Spectroscopy (TDDS) spectrum of two traps (#A and #B) in a deeply-scaled pMOSFET device. The distribution of emission times and impacts on the FinFET V_{th} is apparent. The TDDS technique was developed specifically within the defect-centric approach [33,34].

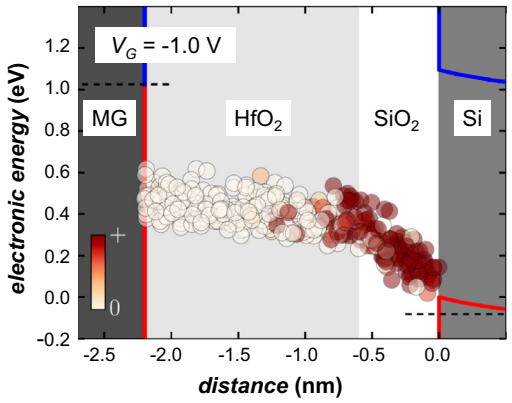

Fig. 5. A simulation of pFET device with a high-k/metal gate stack assuming a defect band. Large-area device is simulated to obtain average behavior. Capture and emission to/from both the substrate and the gate are considered [35,36].

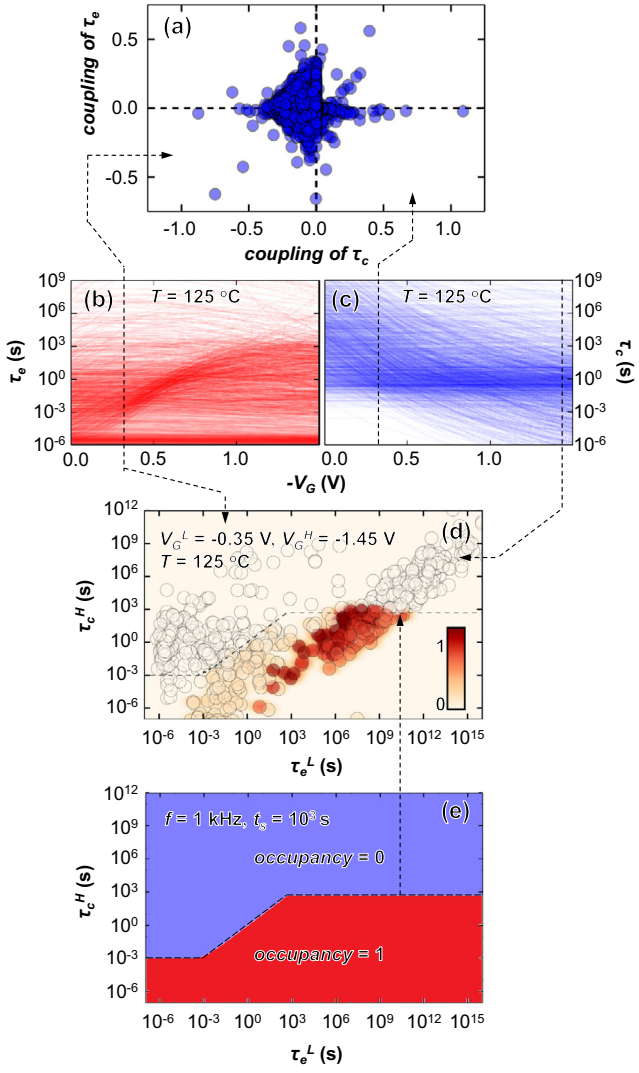

Fig. 6. Based on $\tau_c(V_G)$ and $\tau_e(V_G)$ dependences of a population of defects at given temperature T (b, c), both an RTN behavior (e.g., distributions of coupling factors $kT/q\ \partial\ln\tau/\partial V_G$) [10] (a) and BTI response in the form of a CET map (d) can be computed [37,38]. A trap occupancy map (e.g., for periodic AC signal) [39] (e) can be calculated for any digital workload in the same coordinates. Superimposing it over the CET map determines degradation of the device for that particular workload.

2.2.1.2. Electrical defect properties. In general, a defect can impact one or multiple FET properties. It can, e.g., act as a "stepping stone" between the FET body and the gate and thus contribute to gate leakage [44–46], or it can influence the channel current when charged [47]. Again, the impact will be distributed. E.g., the impact of charged defects on the drain current, for the sake of convenience converted into the threshold voltage shift ΔV_{th}, is approximately exponentially distributed (Fig. 7).

The expectation value of this distribution, η, represents the *mean* impact of a single trap and is the crucial parameter in the defect-centric model. To the first order (cf. considerations around Eq. (1) and e.g. [48]), it scales as

$$\eta = \frac{B_\eta}{A_G}, \tag{2}$$

where B_η is a scaling factor increasing with increasing gate oxide thickness and increasing channel doping N_A and A_G is the area of the device channel [49,50]. Other sources of variability randomizing the channel potential, such as fixed oxide charges and interface defects [51], are expected to take the place of N_A in low-doped channel devices (e.g., FinFETs). The dependence of A_G in FinFET devices is confirmed in Fig. 8 [52].

In Fig. 8, the value of η for p-channel devices (hole trapping) is approximately double the value of $\eta_0 = q/C_o$, the shift expected for a charge sheet at the Si/dielectric interface [48,52]. We have observed that in gate stacks on high-mobility substrates currently being considered for upcoming technology nodes, the ratio η/η_0 can both decrease, in case of p-channel SiGe FETs [53], and increase, in case of n-channel InGaAs [54]. We explained the decrease by trapping deeper in the SiGe-channel gate oxide [53,55]. The increase in the III–V devices we ascribed to more percolative channel conduction induced by still excessive interface and channel defectivity, potentially combined with larger channel carrier centroid displacement from the interface, induced by quantum effects in the low density-of-states semiconductor [54].

In nanolaminate high-k dielectrics used in modern FET devices, each trap "layer" will contribute with its own η value and the resulting distribution will be bi- or multimodal (cf. Fig. 7) [43,56–58].

The impact of a charged defect is obviously not limited to $V_G = -V_{th}$, and can vary with gate and drain biases (cf. τ_c and τ_e temporal dependences in Fig. 6). The V_G dependence is illustrated in Fig. 9 for both the impact on drain [52] and gate currents [35,36,46].

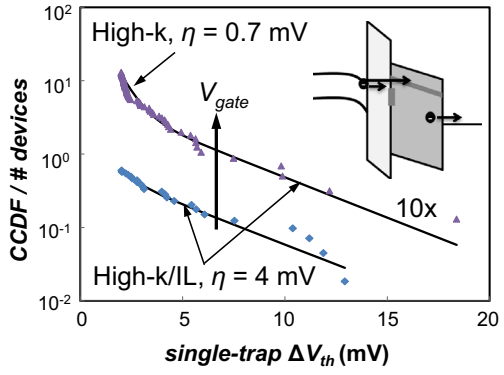

Fig. 7. Exponential distributions of V_{th} shifts ΔV_{th} due to single trapping events, collected from "step heights" in TDDS measurements on multiple nFET devices. The bimodal distribution corresponds to trapping in high-k and at IL/high-k interface [43] (inset; the infrequently-observed electron de-trapping also illustrated). At lower V_G, trapping at the IL/high-k interface is dominant.

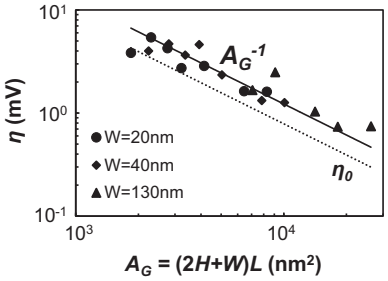

Fig. 8. The mean impact per trap η as A_G^{-1} in pFinFETs (high-k/MG, $t_{inv} \approx 1.7$ nm) with varying fin width W and gate length L (fin height H_{fin} is fixed). Each point is extracted from a monomodal TDDS distribution (cf. Fig. 7). The value of η is ~2× higher than the expected ΔV_{th} for a single charge from a charge sheet approximation $\eta_0 = q/C_{ox}$ [52].

2.2.2. Multiple defects: Defect-centric statistics

Identical stress of a population of deeply scaled devices will result in a *distribution* of FET parameter shifts, as illustrated in Fig. 10 (cf. Fig. 2b). Note that in a population of ~400 devices, the ΔV_{th} of some devices after identical BTI stress is negligible, while other devices shift by ~100 mV(!). This contrasts with the large-area devices of the past, in which identical stress resulted in identical degradation (cf. Fig. 2a). Understanding of BTI and HCI distributions in deeply-scaled devices therefore requires the new, defect-centric approach. The information presented so far in the previous sub-section is sufficient to achieve this goal.

As the individual gate oxide defects charge during operation, corresponding to RTN/BTI and/or HCI degradation, they will concurrently modify the channel current [59]. To describe their combined impact on V_{th} in a population of FETs, we simply assume that the number of charged defects varies from device to device following Poisson statistics with the mean number of defects per device N_T. When combined with the ΔV_{th} exponential distribution of each contributing charged defect (cf. Section 2.2.1.2), it can be

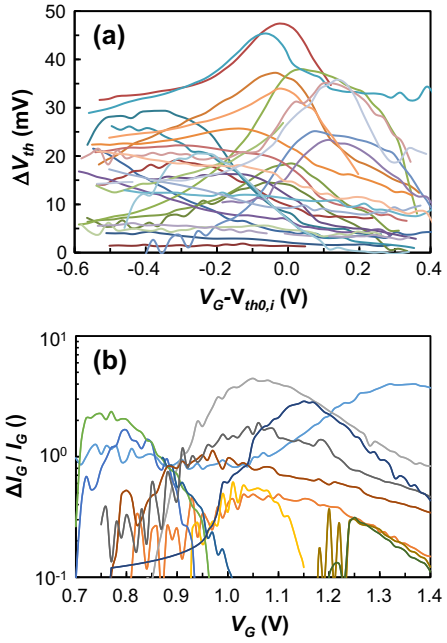

Fig. 9. (a) Different $\Delta V_{th}(V_G)$ defect characteristics are found when measuring 30 different (but nominally identical) pFETs before and after the capture of a single hole [52]. (b) Different $\Delta I_G(V_G)$ characteristics are found when measuring several (but nominally identical) nFETs before and after the activation of a single defect [46].

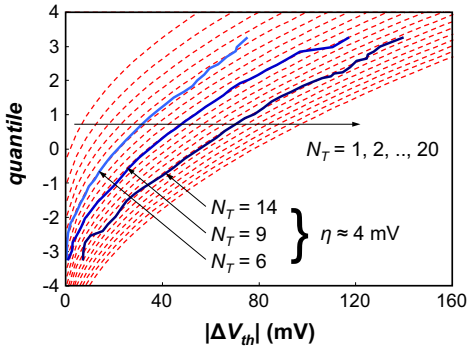

Fig. 10. Total ΔV_{th} distribution (Eq. (3)) for the average number of defects N_T from 1 to 20 (thin lines) rescaled to fit experimental distributions from Fig. 10 of Ref. [60], with the corresponding values of N_T and η readily extracted.

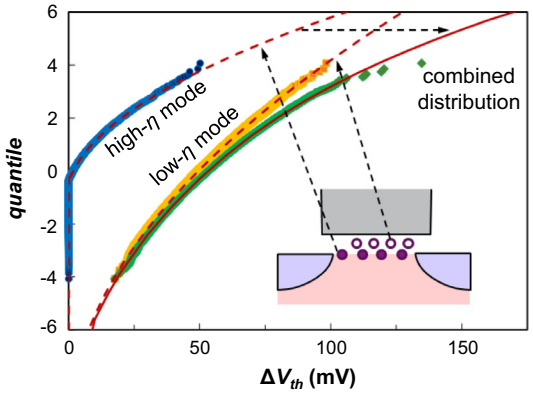

Fig. 11. Illustration of bimodal ΔV_{th} *defect-centric* distribution (cf. the bimodal distribution for *individual* defects, Fig. 7) [16]. Symbols: Monte Carlo, lines: analytic fit [16,58]. The high-σ tail of the full distribution is controlled by defects at the substrate (high η; inset: solid symbols).

shown that the resulting statistics will have a cumulative distribution given by [14,15,61]

$$H_{\eta,N_T}(\Delta V_{th}) = \sum_{n=0}^{\infty} \frac{e^{-N} N^n}{n!} \left[1 - \frac{n}{n!}\Gamma\left(n, \frac{\Delta V_{th}}{\eta}\right)\right]. \quad (3)$$

Note that the above *defect-centric* ΔV_{th} distribution is controlled by only two parameters, η (cf. Eq. (2)), and N_T, where the latter is simply linked to the defect density N_{ot} as $N_T = N_{ot} A_G$. As is apparent from Fig. 10, Eq. (3) excellently describes the measured distributions.

Having an analytical description of the ΔV_{th} distribution has several advantages. It allows to (i) make projections to high percentiles without the need to measure or simulated billions of devices, and (ii) provide a crucial link between the first two statistical moments of the ΔV_{th} distribution [14,15,61]

$$\sigma^2_{\Delta V_{th}}(t) = 2\eta \langle \Delta V_{th}(t) \rangle. \quad (4)$$

$\langle \Delta V_{th}(t) \rangle$ is the mean shift of the population, linked with the two parameters of Eq. (3) as $\langle \Delta V_{th}(t) \rangle = \eta\, N_T(t)$. $\langle \Delta V_{th}(t) \rangle$ is projected to operating conditions using established acceleration techniques. Eq. (3) also allows to extract η directly from measured ΔV_{th} distributions (typically at accelerated conditions), without having to analyze the statistics of individual steps, as will be discussed in the next section.

In devices with high-k dielectrics, trapping in multiple layers will be combined, resulting in a bi- or multi-modal distribution [57,58]. The high-percentile tail may be controlled by the defects low in density, but with high η value (i.e., closer to the substrate), as illustrated in Fig. 11 [16]. The analytical description of the multimodal defect-centric distribution has been also derived, allowing to correctly project the high-percentile tails [58].

The correct knowledge of B_η (Eq. (2)), combined with the projection of the expected degradation mean $\langle \Delta V_{th}(t) \rangle$, discussed in Section 2.2.1.1, then allows to make an educated prediction of *degradation distribution in the entire device population of the VLSI application* [16]. In the following we therefore understand the characterization of time-dependent variability to be equivalent to extracting B_η (i.e., η vs. A_C) for a given technology, analogously to extracting A_{vth} (Eq. (1)) for time-zero variability.

2.2.3. Characterization of time-dependent variability

The parameter η can be extracted from RTN or TDDS (Fig. 4) amplitudes of individual defects or from a ΔV_{th} distribution (Fig. 10), where multiple, Poisson-distributed number of defects contribute simultaneously. While actively-stimulating individual traps using TDDS is considerably more powerful than mere passive RTN measurements, we note that the analysis of individual defect steps is generally a highly elaborate process, involving step detection in time traces with experimental noise, complex "bookkeeping" to avoid double-counting of defects resulting in "stuffing" of amplitude distributions, and the uncertainty in fitting the distribution tail [28]. On the other hand, extraction of B_η from the defect-centric ΔV_{th} distribution using Eqs. (2) and (4) appears to be more pragmatic and more suitable for industrial and production environments.

Obviously, obtaining both time-zero and time-dependent variability distributions requires measurements on a sufficiently large number of devices. If these devices are distributed over a larger area, process-induced variations (e.g. across the wafer) will increase the observed variability. In order to extract the random variability component only, the additional process-induced variability can be corrected for by either using the so-called matched pairs or local arrays of a large number of closely-packed devices.

2.2.3.1. Matched pairs. Analogously to time-zero analysis [22], standard matched FET pairs (MPs), widely available in most test-chip layouts, can be used for the same task of extracting random time-dependent variability [27,28,62]. Resolution of η down to ~0.1 mV range can be achieved [28]. We define

$$\delta\Delta V_{th} = \Delta V_{th,L} - \Delta V_{th,R} \quad (5)$$

as the difference between the V_{th} shift of the left ("L") and the right ("R") devices of the MP. We now introduce additional systematic (process-induced) variability, represented by varying the originally constant mean number of defects per device N_T [28]. This *conceptually* mimics across-wafer variations in gate oxide defect density of traps due process variations, such as plasma-induced damage, or larger degradation in devices with locally thinner oxide. We see that the single-device defect-centric distribution is substantially dilated (Fig. 12a). A naive extraction of random variability from this distribution, represented by η, then leads to incorrect conclusions. (Such an error is analogous to obtaining $\sigma_{Vth0,r}$ from single-device time-zero V_{th0} distributions.) When systematic variability in MPs is simulated by using the randomized, but *identical* N_T *for both "L" and "R" devices of each pair*, the MP $\delta\Delta V_{th}$ distribution in Fig. 12b is not significantly changed. The *intrinsic*, i.e. random variance ($\sim\eta$, Eq. (4)) can be readily extracted from the difference distribution $\delta\Delta V_{th}$ obtained on MPs (Fig. 12b).

Fig. 13 illustrates the methodology applied to real silicon devices. It is apparent that for both *n* and *p*FinFET devices tested, the time-zero variances extracted from single devices (Fig. 13a and b, open symbols) are affected by systematic variability and

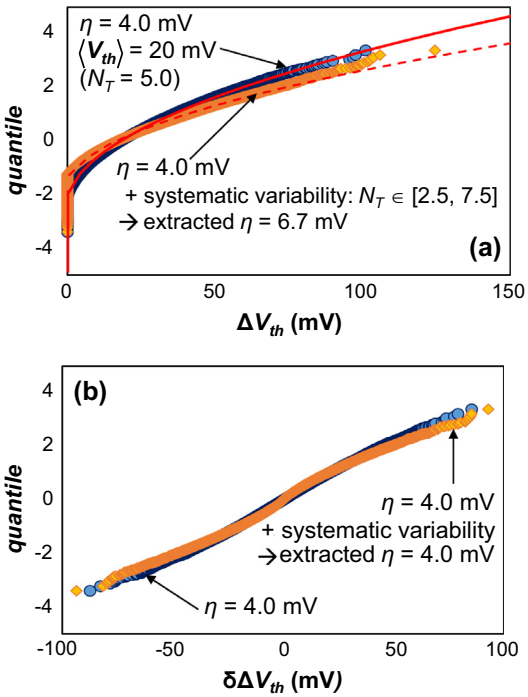

Fig. 12. Probit plots of Monte Carlo simulation of defect-centric distributions in (a) single devices and (b) matched pairs. *Additional systematic variability*, generated by distributing the defect density N_T, in single devices (a) *is fully compensated and the original η is restored* (b). Blue circles and orange diamonds: distributions *without* and *with* systematic variability included [28]. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

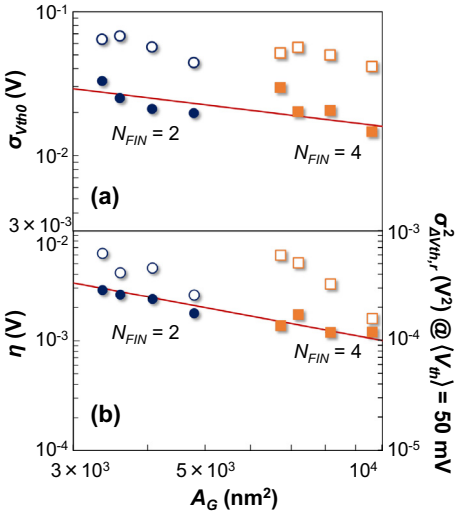

Fig. 13. The random components of both (a) time-zero and (b) time-dependent variabilities, extracted using matched pairs (solid symbols), follow area scaling (Eqs. (1) and (2), respectively, lines) in contrast to single nFinFET devices (open symbols), which are affected by systematic variability. Eq. (4) is used for the right-hand axis [28].

thus overestimate the random component extracted from MPs (solid symbols), which follow correct A_G scaling (line, Eq. (1)) [22,23,25]. Similarly for time-dependent variability, η obtained on nFinFETs (Fig. 13c) by naive extraction from single devices does not scale correctly with A_G. Thus extracted η overestimates the true value, as illustrated already in Fig. 12. However, when the MP methodology is used, the resulting η's scale excellently with device area and the parameter B_η (Eq. (2)) can be readily extracted.

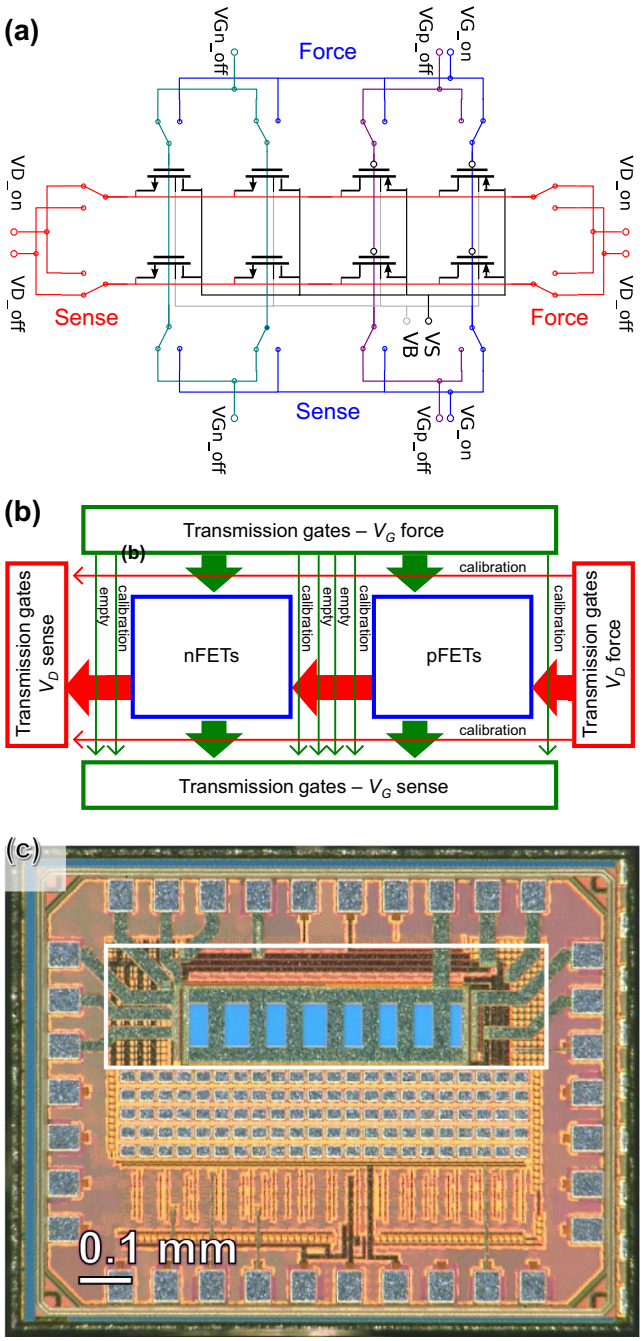

Fig. 14. (a) Reduced schematic of the array including both nFETs and pFETs, double transmission gates (shown as switches), Kelvin sensing for the drain and gate terminals, the body and the source connections. (b) Placing plan of the array. To reduce unwanted RTN signals and enable higher than nominal voltages on the test FETs, the switches are designed with sufficiently large IO devices. Two shift registers are used to address the transmission gates with level shifters, with the added capability to measure multiple test FETs in parallel. Calibration and open lines are included to characterize the leakage from the periphery, the parasitic resistances and as a sanity check for the programming of the chip during measurements. (c) Microphotograph of the chip with the array containing 54,432 devices is delineated (top). Similar area is occupied by a few tens of individually-accessible FETs (center). A pipelined array for parallelizing MSM sequences in hardware by up to 5× contains several hundred devices (bottom; discussed in [67,68]).

2.2.3.2. Local arrays. One of the first applications of closely-packed identical capacitors to separate across-wafer and random variabilities in TDDB measurements was proposed by Roussel et al. [26]. Kerber et al. have used simple, periphery-less 8 × 8 local FET arrays

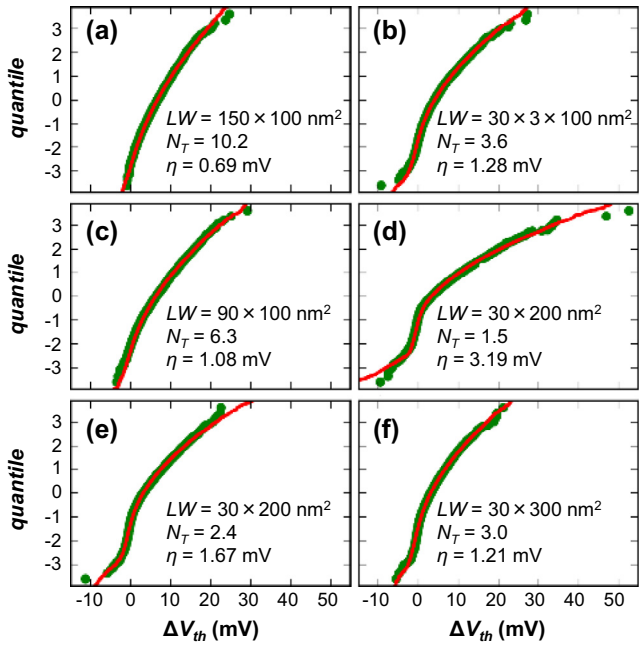

Fig. 15. ΔV_{th} distributions obtained on pFETs with 6 different areas in the array in Fig. 14 [24]. Opposite shifts are observed originating from RTN [33]. Symbols: measurements, curves: Monte Carlo (MC) fits of defect-centric distributions (Eq. (3)), including the RTN tails.

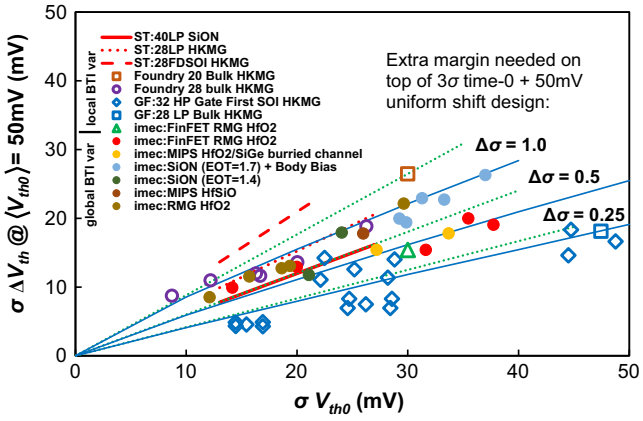

Fig. 16. pFET time-dependent variability (at 50 mV mean degradation) plotted against time-zero variability for various techologies. Results from the discussed array are designated "Foundry: 28 bulk HKMG". The isolines indicate the added margin ($\Delta\sigma$) on top of the standard 3σ margin for CMOS logic that the design needs to handle (i.e., $3\sigma + \Delta\sigma$) when factoring in time-zero variability + 50 mV mean BTI shift, using either a Normal approximation (dashed) or full defect-centric distribution (solid), cf. Fig. 17 [66].

to extract both time-zero and time-dependent variability and to separate across-wafer and random components [25]. Substantially larger arrays, allowing to map further into the tails of variability distributions, already require sophisticated control periphery [63,64]. Learning and results obtained with arrays with $\sim 10^4$ devices are demonstrated here [24,58,65,66].

The array, illustrated in Fig. 14, includes 54,432 individual test FETs [24,65]. Different transistor geometries are used, each of which contains $108 \times 42 = 4536$ single test FETs. All the test n and pFET devices share the source and body terminals, the gates are shared among the test FETs in rows, while the drains are shared in columns (Fig. 14a). The placement plan of the array is depicted

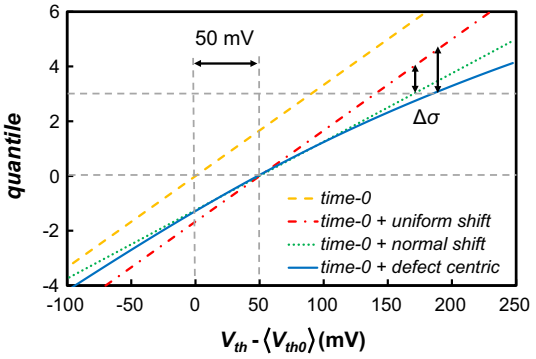

Fig. 17. Three possible ways of adding time-dependent variability to the time-zero distribution (dashed yellow): (i) a simple shift of $\langle \Delta V_{th}(t) \rangle$ in all devices (dot-dashed red), (ii) a Normal (Gaussian, dotted green), and (iii) the defect-centric statistics (Eq. (3), solid blue). The discrepancies between the defect-centric distribution and the approximations are evident at higher quantiles. Considering time-zero variability + 50 mV mean BTI shift, using either a Normal BTI approximation or defect-centric BTI can be expressed as additional margin ($\Delta\sigma$) needed on top of a 3σ margin in the conventional, time-zero-only design [61,66]. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

in Fig. 14b. The drawn area of the design is 0.18 mm² (Fig. 14c, highlighted in red[2]).

The array allows the standard characterization of time-zero variability, i.e., the extraction of σ_{Vth0}^2 for varying device gate areas A_G, and hence A_{Vth} (Eq. (1)). A Measure-Stress-Measure (MSM) sequence on each FET then allows to determine ΔV_{th} for each device. Typical ΔV_{th} distributions are shown in Fig. 15. The distributions have the distinct defect-centric shape (Fig. 10), allowing the extraction of η, and the time-dependent variability (Eq. (4)) for different device areas [24,65]. Opposite shifts are also observed, originating from RTN in the devices [58].

Both the time-zero and the time-dependent intrinsic variances are therefore obtained using the same array, allowing to characterize and benchmark the underlying technology. The variances are shown in Fig. 16, designated as "Foundry: 28 bulk HKMG" (6 open purple circles). Note that the variances per technology typically scale with device area, as per Eqs. (1), (2) and (4) [61,62]. Fig. 16 further illustrates the relatively wide spread in the σ_{Vth0}-$\sigma_{\Delta Vth}$ relationship [51], with values of $\sigma_{\Delta Vth}$ at $\langle \Delta V_{th} \rangle = 50$ mV (a typical CMOS logic degradation criterion) almost reaching their σ_{Vth0} counterparts for some technologies. This confirms the significance of considering the time-dependent variability—the main thesis of this paper.

2.3. Total variability

The combined knowledge of time-zero and time-dependent variability for a given technology is expressed through the tuple (σ_{Vth0}; $\sigma_{\Delta Vth}$ @ given $\langle \Delta V_{th} \rangle$), as in Fig. 16, or more generally through area-independent (A_{Vth}; B_η), cf. Eqs. (1) and (2). This combined information enables projections of the *total* distribution of a FET parameter after operation at nominal operating conditions, allowing the circuit designer a rigorously-derived control of the design margins.

As illustrated in Fig. 1f, the *total* distribution is simply a convolution of time-zero and time-dependent distributions [61,66,69,70]. Fig. 17 illustrates this convolution for 3 different cases: (i) no time-dependent variability (uniform shift, corresponds to Fig. 1c), (ii) Normally-distributed time-dependent variability [71], and (iii) Eq. (3) (defect centric). Note that the Normal

[2] For interpretation of color in Fig. 14, the reader is referred to the web version of this article.

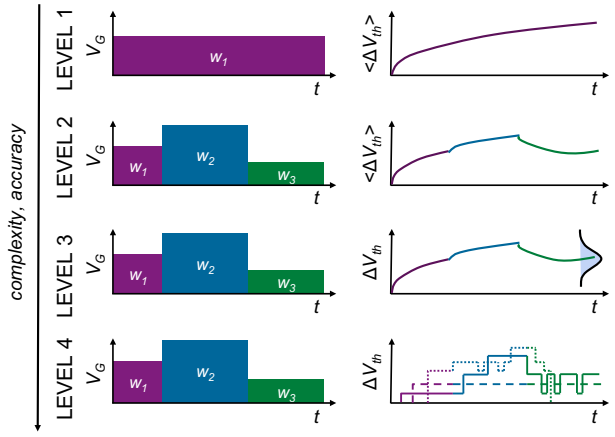

Fig. 18. Complexity/accuracy levels of incorporating device aging (specifically here, the threshold voltage shift) in circuit simulations. The full workload on each device can be *approximated* by a series of phases w_i with duration t, voltage V, duty factor DF, frequency f, and temperature T. (In reality the number of workload phases is typically very large.)

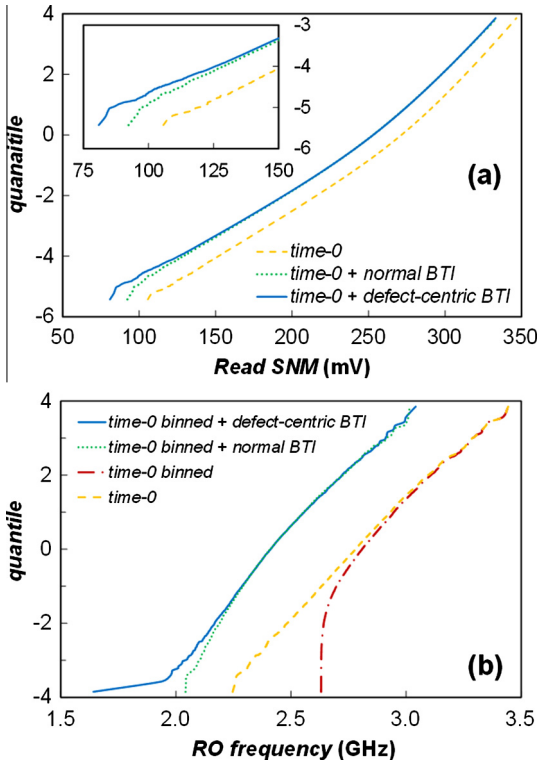

Fig. 19. (a) Probit plot of the Read Signal Noise Margin (RSNM) of 28 nm technology SRAM cell for an average 50 mV NBTI shift. Inset magnifies the discrepancy at higher quantiles. (b) Impact of binning at time-zero on a population of ring oscillators. The yield cut-off criterion of *mean* – 1σ of the ring oscillator frequency is used. The loss of the effect of binning due to time-dependent variability at low percentiles, as well as the choice of the time-dependent distribution (normal or defect-centric) are apparent [81].

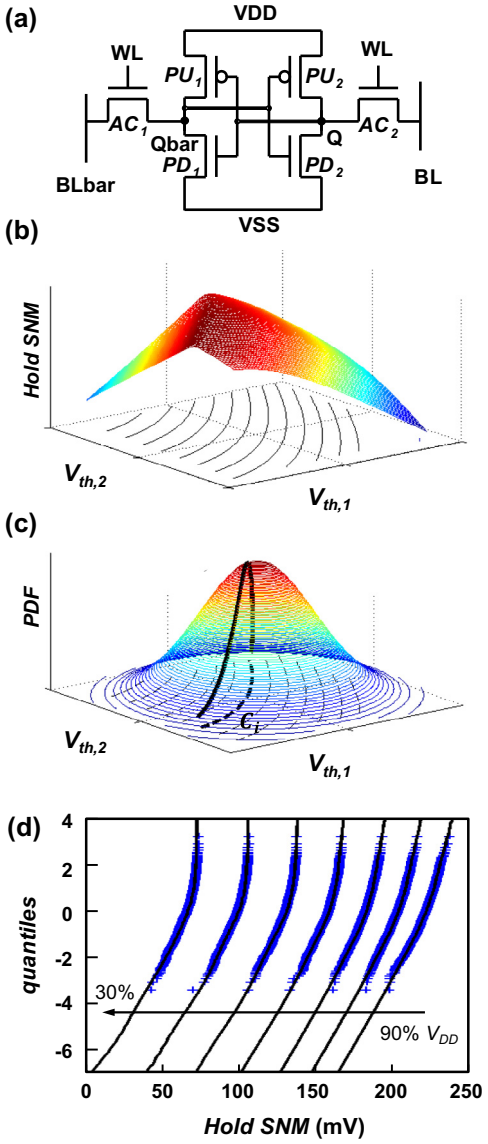

Fig. 20. (a) A schematic of a 6T-SRAM cell. (b) Any given circuit figure of merit, e.g., SRAM Hold SNM, is pre-characterized as a function of the 6 FET V_{th} values (dependence on $V_{th,1}$ and $V_{th,2}$ shown). (c) Projected total distributions after degradation (as discussed in Section 2.3.) of the 6 FET V_{th}'s is evaluated along the constant SNM isoline. (d) SNM distribution at decreasing supply voltage V_{DD}. Lines: the non-MC numerical propagation technique can predict the tails of the distribution up to -7σ. Symbols: MC simulation added for comparison shows excellent agreement with the non-MC method [83].

approximation is not entirely physical, as it is bound to cross the time-zero distribution (at low percentiles). On the other hand, the defect-centric model (Eq. (3)) predicts larger V_{th} shifts at high percentiles, again emphasizing the need to factor in time-dependent variability (cf. the definition of $\Delta\sigma$ in Fig. 17 and the isolines in Fig. 16).

We also note that in some cases, a correlation between time-zero and time-dependent variability may exist. This is because devices with higher V_{th} may degrade less at fixed gate bias as both the oxide field and self-heating effects driving the degradation will be lower [72]. Such correlations need to be factored into the convolution.

3. Application to circuits

The conventional reliability margins in modern technologies generally decrease due to the higher electric fields, while simultaneously, voltage-overdriving techniques are employed by designers to maximize performance [43]. Consequently, more elaborate reliability projection methods are needed to guarantee product reliability. The methods are based on the realization that (i) in real circuits, the devices seldom see constant stress at the supply voltage throughout their entire operating lifetime, as has been

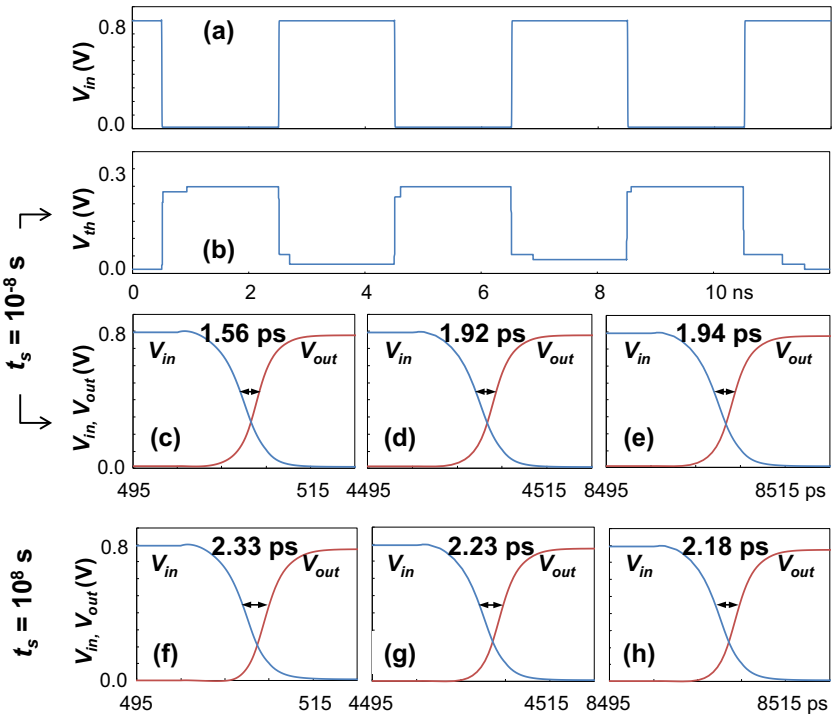

Fig. 21. Inverter degradation simulation transient snapshots. (a) Three periods of a $f = 250$ MHz input signal of the studied inverter. (b) Corresponding time-dependent pFET threshold voltage V_{th} after 10^{-8} s illustrates the modulation of V_{th} by defects. (Note that due to short channel effects, V_{th} is also modulated by V_D, i.e., the output signal of the inverter.) V_{th} after 10^8 s is further degraded due to the capture of charge in large-τ_c defects. Switching delay of the studied inverter during the three periods (c–e) after 10^{-8} s and (f–h) 10^8 s [4].

assumed in the past conservative technology reliability qualification, (ii) the failure criterion for each device will be different, depending on its function in the circuit, and (iii) the time-dependent variability needs to be considered in deeply-scaled technologies, as argued hitherto. All of these notions require *technology*- and *reliability-aware simulation* and *design*.

For the purposes of this paper, the different levels of implementation of device aging in circuit simulations are defined in Fig. 18. Level 1 corresponds to predicting the device degradation by assuming the device operates at a fixed "effective" workload throughout its entire lifetime in the circuit. Level 2, an improvement over Level 1, acknowledges that devices can be exposed to a sequence of different workloads throughout their operation, including e.g. short bursts of data activity (at ns – ms time scales) to "turbo", "sleep", and "off" modes (ms – day time scales) [73]. Implementations of Level 2 range from the so-called reaction-diffusion model [74] to CET map-based (cf. Fig. 6) [75,76]. Level 3 then adds the time-dependent variability parameter distributions, as derived above (Eq. (2)), on top of the projected mean parameter shift (cf. Level 3 in Figs. 18 and 1e) [41,77–80].

Level 1–3 circuit simulations evaluate the circuit at *static* degradation projected at a specified time. In contrast to that, Level 4 simulation incorporates the *temporal* stochastic behavior of individual traps and allows transient simulations. Level 3 and Level 4 simulations are now discussed.

3.1. Level 3 circuit simulations

Similarly to Level 2, Level 3 circuit simulations rely on projecting mean degradation $\langle \Delta V_{th}(t) \rangle$ for realistic workload for every device, as outlined in Section 2.2.1.1.

The significance of incorporating time-dependent variability in Level 3, and in particular, our defect-centric approach (Eq. (3)) in circuit simulations, is addressed in Fig. 19. For high-σ designs, such as large SRAM arrays [82], circuit simulations show that incorporation of time-dependent variability will influence the distribution tails [81], as was already alluded to in Fig. 17. The distribution tails determine the product failure rates in the field and correct incorporation of time-dependent variability is therefore essential.

For low-σ designs, such as logic data paths [71,78,79], we notice that the choice of the time-dependent variability distribution will be visible even at low σ values, if product binning is considered [81]. This is because this standard manufacturing procedure allows the manufacturer to compensate for time-zero variability, which, however, increases the relative weight of time-dependent variability, not present and not assessable in the product at time-zero. At the moment it appears that the Level 3 approach (cf. Fig. 18 and Fig. 1d–f) has the best chance of being integrated in commercial EDA tools.

To achieve the distributions in Fig. 19, simulations were repeated with the same circuit instantiated with the FET threshold voltages randomly selected from the total distribution (Fig. 17) in each iteration. This brute-force MC technique, however, does not scale well to offer insights into the distribution tails. We have therefore recently developed a fully *non*-MC technique, relying on first describing the circuit with a *response surface*, followed by numerically propagating the total V_{th} distribution (Fig. 17) through it. Using this method, projections to $\pm 7\sigma$ (Fig. 20) can be made with a modest CPU effort for certain circuits [83].

3.2. Level 4 circuit simulations

Level 4 (Fig. 18) allows transient circuit simulations with the impact of individual traps, allowing to study e.g. RTN effect on circuits, such as sensor arrays [63], after aging. It is physically the most accurate, but also correspondingly more CPU intensive. To initialize the simulation, Level 3 simulation can be first performed up to the simulated age of the circuit. Then, each device is instantiated with a Poisson-distributed number of traps and each trap is instantiated with $\tau_e(V_G)$, $\tau_c(V_G)$, and ΔV_{th}, taken from the

corresponding distributions (Figs. 6 and 10) [17,84]. The impact on ΔV_{th} is adjusted according Eq. (2). During the simulation, the trap occupancies are dynamically evaluated in each simulation time step depending on $\tau_e(V_G)$ and $\tau_c(V_G)$ of each trap.

Fig. 21 shows snapshots of one instance of the inverter simulation at the beginning of its operating lifetime (Fig. 21b–e) and after 10^8 s (Fig. 21f–h). Fig. 21b shows the pFET threshold voltage V_{th} behavior at the beginning of the circuit operation. V_{th} is changing as single holes are captured in two fast "cyclo-stationary RTN" [85] defects when the inverter input is low (i.e., the pFET gate is stressed), and subsequently emitted when the inverter input is high (i.e., pFET $V_G = V_S$). The same two defects are still active after 10^8 s of the circuit operation (Fig. 21f); note, however, the pFET V_{th} is further degraded with respect to its initial value (Fig. 21b) due to the charge capture in slow defects. This latter behavior thus naturally emulates the "classical" BTI degradation.

The inverter switching transients are also illustrated in Fig. 21. It is apparent that there is a variation in the inverter switching delay from period to period (see Fig. 21c–e and f–h), resulting in the so-called delay jitter [86]. The overall slowdown of the inverter after 10^8 s of operation is also apparent (cf. Fig. 21c–e and f–h).

4. Conclusions

We have argued that time-dependent variability (reliability variability) is an emerging concern that needs to be considered in circuit design in addition to time-zero variability and mean device degradation [87]. We moreover have claimed that the time-dependent variability in deeply scaled devices can be best understood in terms of an ensemble of individual defects and their time, voltage, and temperature dependent properties. We have discussed the properties of gate oxide defects and have shown how, within the so-called defect-centric picture, these properties can be used to construct time-dependent variability distributions and can be propagated up to transistor-level circuits. At the moment it appears that the approach presented as Level 3 in Section 3.1 is the most suitable for being integrated in commercial EDA tools. The necessary formalism has been presented.

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