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2016 Jpn. J. Appl. Phys. 55 04ED14

(http://iopscience.iop.org/1347-4065/55/4S/04ED14)

Japanese Journal of Applied Physics **55**, 04ED14 (2016)
http://doi.org/10.7567/JJAP.55.04ED14

REGULAR PAPER

On the limits of applicability of drift-diffusion based hot carrier degradation modeling

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Received September 30, 2015; revised December 18, 2015; accepted January 14, 2016; published online March 16, 2016

We study the limits of the applicability of a drift-diffusion (DD) based model for hot-carrier degradation (HCD). In this approach the rigorous but computationally expensive solution of the Boltzmann transport equation is replaced by an analytic expression for the carrier energy distribution function. On the one hand, we already showed that the simplified version of our HCD model is quite successful for LDMOS devices. On the other hand, hot carrier degradation models based on the drift-diffusion and energy transport schemes were shown to fail for planar MOSFETs with gate lengths of 0.5–2.0 μm. To investigate the limits of validity of the DD-based HCD model, we use planar nMOSFETs of an identical topology but with different gate lengths of 2.0, 1.5, and 1.0 μm. We show that, although the model is able to adequately represent the linear and saturation drain current changes in the 2.0 μm transistor, it starts to fail for gate lengths shorter than 1.5 μm and becomes completely inadequate for the 1.0 μm device.

1. Introduction

Hot carrier degradation (HCD) is one of the key issues in the field of reliability of microelectronic devices, in particular of MOSFETs.[1)] However, for a proper physics-based description of this complex phenomenon, one needs a detailed knowledge about the carrier transport in the targeted devices.[2–13)] Hot-carrier degradation is accepted to be driven by the generation of traps at or near the Si/SiO_2 interface. These traps are assumed to be generated by the dissociation of pristine Si–H bonds. This process can be induced either by cold or hot carriers[2,5,7,9)] which trigger the multiple- or single-carrier bond-breakage mechanisms. Note that in a real device subjected to hot-carrier stress both cold and hot carriers are present, and thus both mechanisms contribute.[14,15)] As a consequence, to evaluate the rates of these two competing processes one needs to distinguish between "cold" and "hot" carriers. Therefore, the key point in HCD modeling is to know how carriers are distributed over energy.

This information is provided by the carrier energy distribution functions (DFs), which can be obtained from a solution of the Boltzmann transport equation (BTE).[8,16)] Usually the BTE is solved either by a stochastic Monte-Carlo method,[16)] or a deterministic method based on a spherical harmonics expansion (SHE)[8,17)] of the carrier DFs. However, even for ultra-scaled planar CMOS devices these methods are computationally challenging and time consuming. Thus, the former one requires substantial computational effort, while the latter one requires a massive amount of memory to store all variables.[16)] Devices with larger dimensions or non-planar interfaces and geometrical features, like LDMOS devices, dramatically aggravate this situation, making the modeling of HCD intricate. As a result, simplified approaches to the BTE solution have attracted attention.[12,18–23)] These simplified techniques are often based on the moments of the Boltzmann transport equation, usually the drift-diffusion (DD) scheme, and are computationally far more inexpensive than the aforementioned ones.

We have recently proposed an HCD model for LDMOS transistors based on the DD scheme,[22,24,25)] which uses an analytic expression that considers both high and low energy carriers. The problem, of course, is that the energy distribution functions in LDMOS devices have different shapes compared to those in planar nMOSFET structures. In Ref. 19 it was suggested that the DD scheme is applicable to devices with gate lengths longer than 0.5 μm. However, as we have shown in Ref. 21, drift-diffusion and even hydrodynamic approaches can be inadequate for modeling HCD in nMOSFETs with gate lengths of 2.0 μm. Thus, in this context, the analysis of the limits of the validity of the DD-based model is a very important task. For this purpose, we use a series of planar nMOSFET structures of a similar architecture but with different gate lengths.

2. Simulation framework

Our HCD model covers and links the three main aspects of hot-carrier degradation: carrier transport treatment in the semiconductor with the evaluation of the carrier energy distribution function, a microscopic description of the defect generation kinetics at the Si/SiO_2 interface, and simulation of the degraded device. First the carrier DFs are computed for a particular device geometry and given stress/operating conditions. These DFs are then used to evaluate the bond-breakage rates, and hence to simulate the interface state density N_{it} as a function of the lateral coordinate x for each stress time step t. The obtained $N_{it}(x, t)$ profiles are then used to simulate the characteristics of the degraded devices.

In this work we compare the results of two versions of our HCD model which differ only in the way the carrier energy distribution functions are obtained. The reference model employs the BTE solution produced by the open source deterministic BTE solver ViennaSHE, which is based on the spherical harmonics expansion of the carrier DF.[26)] The second version of the model is computationally less expensive and relies on an analytic expression for the carrier DF based on macroscopic device quantities obtained from the DD scheme.[22,24)]

2.1 Carrier transport

The carrier energy distribution function is the most important information and one of the two main constituents of our physics-based HCD model. The full version of our model employs the deterministic solver ViennaSHE for evaluating the DFs and is used as a reference for validating the DD-based approach. The DD approach represents the DFs by an analytic expression with the parameters linked to

the moments of the BTE.[22,24] In recent years extensive efforts were made to develop different analytical approaches/expressions trying to mimic the shape of the DF in different regions. Some of such expressions are the heated Maxwellian,[27] the approach developed by Cassi et al.,[18] Hasnat et al.[19] and the Reggiani approach.[12] Our model uses the following expression for the DF:[24]

$$f(\varepsilon) = A\exp\left[-\left(\frac{\varepsilon}{\varepsilon_{\mathrm{ref}}}\right)^{b}\right] + C\exp\left(-\frac{\varepsilon}{k_{\mathrm{B}}T_{\mathrm{L}}}\right), \qquad (1)$$

where the first term accounts for hot carriers in the ensemble and the second, Maxwellian term, represents the contribution of cold, thermalized, carriers. The parameters A, C, and $\varepsilon_{\mathrm{ref}}$ are determined by the moments of the BTE and the DFs normalization criterion:

$$\int_0^\infty f(\varepsilon)\,d\varepsilon = 1,$$
$$\int_0^\infty f(\varepsilon)g(\varepsilon)\,d\varepsilon = n,$$
$$\int_0^\infty Ef(\varepsilon)g(\varepsilon)\,d\varepsilon = \frac{3}{2}nk_{\mathrm{B}}T_{\mathrm{n}}. \qquad (2)$$

Further knowledge about the density of states $g(\varepsilon)$ and the carrier temperature T_{n} is required. The density of states is modeled by an expression proposed in Ref. 28:

$$g(\varepsilon) = g_0\sqrt{\varepsilon}(1+\eta\varepsilon), \qquad (3)$$

which provides an excellent approximation to the typically used non-parabolic model of Kane but has the advantage of being analytically integrable Under quasi-equlibrium conditions in long channel devices, the carrier temperature can be approximately obtained by

$$T_{\mathrm{n}} = T_{\mathrm{L}} + \frac{2}{3}\frac{q}{k_{\mathrm{B}}}\tau\mu F^2, \qquad (4)$$

where T_{L} is the lattice temperature, τ the energy relaxation time, F the electric field, and μ the carrier mobility. All of these parameters can be evaluated from the drift-diffusion simulation. It is worth to emphasize that in our recent publication[23] we have compared our analytic expression for the carrier DF against those used in the aforementioned models in the context of hot-carrier degradation. It was shown that our model is the most suitable one for an adequate description of HCD and will thus be used in the following.

2.2 Defect generation

The second important sub-module of our physics-based HCD model is the detailed microscopical description of defect generation. Si–H bonds at the Si/SiO_2 interface can be excited and eventually broken by electrons and holes of different energies. These bonds will be converted into electrically active interface traps which, when occupied, disturb the electrostatics and degrade the mobility due to additional charged scattering centres.

In our model these Si–H bonds are treated within the truncated harmonic oscillator model (see Fig. 1), which can be excited via two main competing pathways. The first one is called "AB-process". It can occur if a solitary high-energetic carrier hits the bond. In this scenario one of the bonding electrons is excited to an antibonding (AB) state. The second pathway is related to multivibrational excitations (MVE) of the bond and is referred to as the "MVE-process". In this case the bond is subsequently bombarded by a series of carriers with energies below the threshold for triggering the AB-mechanism and is therefore able to climb up the ladder of eigenstates of the harmonic oscillator. Note that we also consider all possible superpositions of the AB- and MVE-mechanism. This means that the bond can be preheated, i.e., excited to an intermediate level, by a cascade of colder carriers. The potential barrier, separating the bonded and the transport state, is reduced and the probability of finding a single carrier with sufficient energy to overcome this barrier is higher.

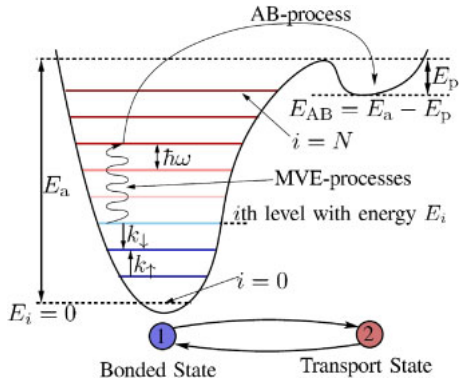

Fig. 1. (Color online) A schematic representation of the truncated harmonic oscillator model used for the derivation of our physics-based HCD model. The Si–H bond is ruptured at the transition from the bonded state 1 to the transport state 2. The required activation energy E_{a} for overcoming this barrier can be effectively lowered by the interplay between the AB- and the MVE-mechanism.

Two additional factors, which affect the trap generation rates, are also implemented in our HCD model. First, the reduction of the activation energy E_{a} due to the interaction of the oxide field with the dipole moment of the bond,[6,29] and second, stochastic variations of E_{a} caused by structural disorder.[30,31]

The corresponding rates for the AB- and MVE-process are determined by the carrier acceleration integral (AI):[9,10,32,33]

$$I_{\mathrm{AB/MVE}} = \int_0^\infty f(\varepsilon)g(\varepsilon)v(\varepsilon)\sigma_0(\varepsilon-\varepsilon_{\mathrm{th}})^p\,d\varepsilon, \qquad (5)$$

where $f(\varepsilon)$ is the DF, $g(\varepsilon)$ the density of states (DOS), $v(\varepsilon)$ the carrier group velocity, and $\sigma_0(\varepsilon)$ the reaction cross section.

2.3 Simulations of the degraded devices

The $N_{\mathrm{it}}(x,t)$ profiles generated using the information of the carrier DFs, are then loaded into the device and circuit simulator MiniMOS-NT[34] (based on the drift-diffusion and energy transport schemes) used in the GTS framework,[35] which models the characteristics of the degraded devices. One of the important ingredients needed for the simulations of the degraded devices is a proper mesh. This mesh should be fine enough in all crucial device segments but still contain a moderate number of elements. To achieve this goal the adaptive meshing framework ViennaMesh, which generates meshes based on the gradient of the built-in potential containing a reasonable number of cells, is used.[36,37]

In our recent work we have already presented and validated both versions of the model in the context of hot-carrier degradation in LDMOS devices.[15,22] N- and

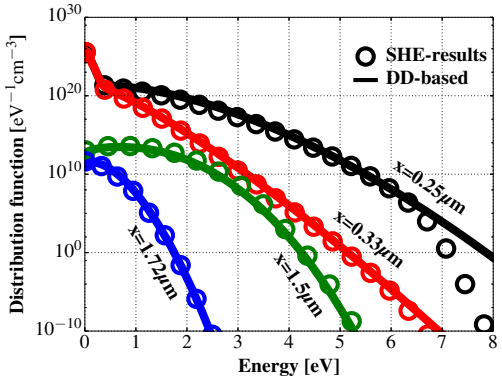

Fig. 2. (Color online) Electron DFs simulated for $V_{GS} = 18\,V$ and $V_{DS} = 2.0\,V$ at different values of the lateral coordinate for the nLDMOS device with the deterministic solver ViennaSHE (symbols) and with the DD-based analytical approach (lines).

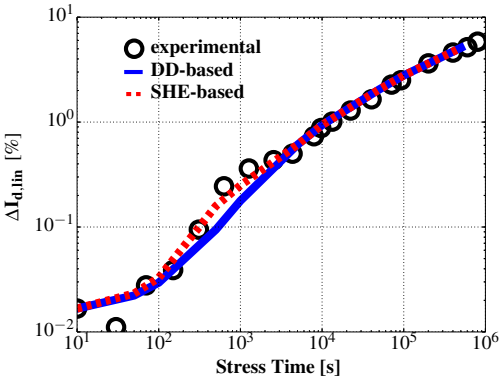

Fig. 3. (Color online) $\Delta I_{D,lin}(t)$ degradation traces: experiment (symbols) vs simulation using the full (dashed)- and the DD-based (solid) model.

p-channel LDMOS transistors were stressed at different combinations of V_{GS} and V_{DS} voltages and the changes of the linear and saturation drain current ($\Delta I_{D,lin}$ and $\Delta I_{D,sat}$) were recorded. Figure 2 shows the carrier energy distribution functions simulated for the nLDMOS transistor for different device sections, i.e., at the bird's beak and near the drain, with ViennaSHE and the DD-based analytical model for $V_{GS} = 18\,V$ and $V_{DS} = 2.0\,V$. As can be seen, the agreement between the DFs is very good. Figure 3 shows the characteristics of the nLDMOS devices stressed at the same voltages as those used in Fig. 2 within a stress time window of up to 1 Ms. One can see that the simulated DFs with different approaches are in very good agreement as both versions of the model lead to very similar theoretical $\Delta I_{D,lin}(t)$ and $\Delta I_{D,sat}(t)$ traces and can properly represent the experimental data.

In order to analyze whether the DD-based model is able to capture HCD in planar structures with shorter channel lengths, we have generated a series of three devices with a similar topology but different gate lengths L_G, namely 2.0, 1.5, and 1.0 μm. To generate the structure of these devices we used the Sentaurus process simulator.[38)]

3. Results and discussion

While applying both versions of our HCD model to planar nMOSFETs, we have used more typical stress voltages for these transistors as compared to the reference nLDMOS device, i.e., $V_{GS} = 7.5\,V$ and $V_{DS} = 2.5\,V$, see Refs. 32, 39, and 40. We simulated electron DFs, interface state density profiles $N_{it}(x)$, and degradation traces $\Delta I_{D,lin}(t)$ as well as $\Delta I_{D,sat}(t)$ for up to 50 ks.

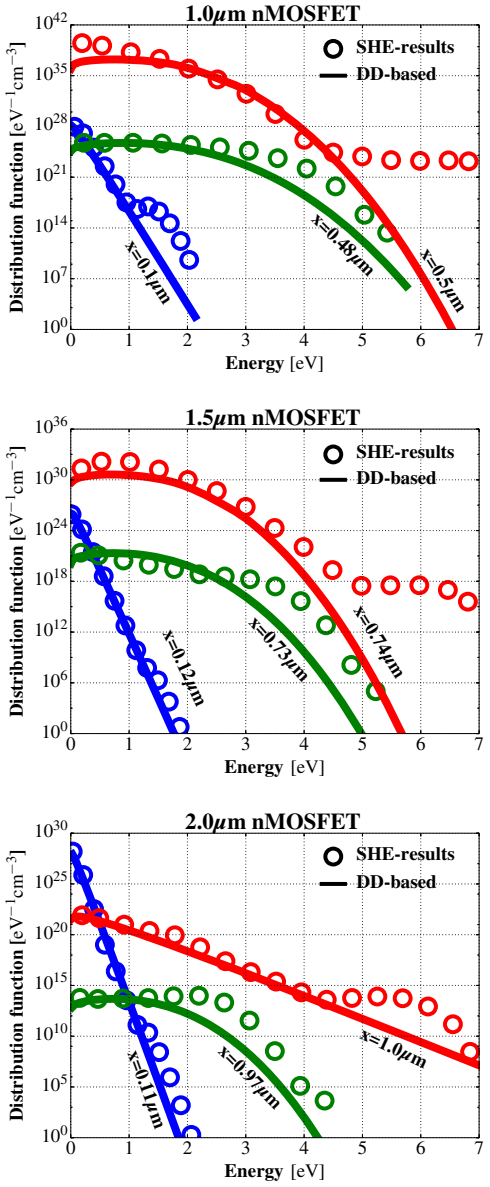

Fig. 4. (Color online) Electron distribution functions at different lateral positions along the channel for the three nMOSFETs with $L_G = 1.0$, 1.5, and 2.0 μm simulated with ViennaSHE and the DD-based version of the model. Symbols correspond to ViennaSHE results, solid lines to results obtained with the analytic approach.

Figure 4 summarizes the simulated electron energy distribution functions obtained with ViennaSHE and the DD-based approach at different lateral coordinates along the channel. At low and moderate energies the DFs computed with the analytic approach Eq. (1) reasonably mimic the DFs obtained from a BTE solution of ViennaSHE. However, at higher energies, the curvatures of the DFs evaluated with the two approaches are different. It can be seen that the accuracy deteriorates for shorter channel lengths. On the other hand, the occupation numbers at these energies have already dropped by several orders of magnitude, and it is not obvious whether this discrepancy in the DFs translates into a sizeable error in the interface state profiles $N_{it}(x)$ and the $\Delta I_{D,lin/sat}$ degradation traces.

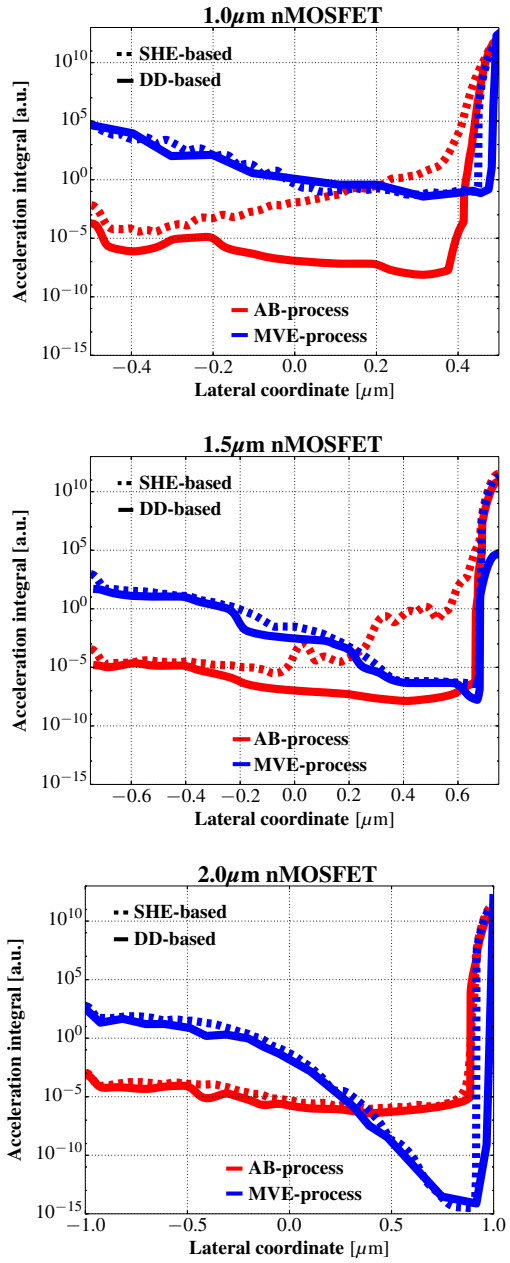

Fig. 5. (Color online) Acceleration integrals for the AB- and the MVE-process calculated from the DFs obtained from the DD-based model (solid lines) and ViennaSHE (dashed lines) for $V_{GS} = 7.5\,V$ and $V_{DS} = 2.5\,V$.

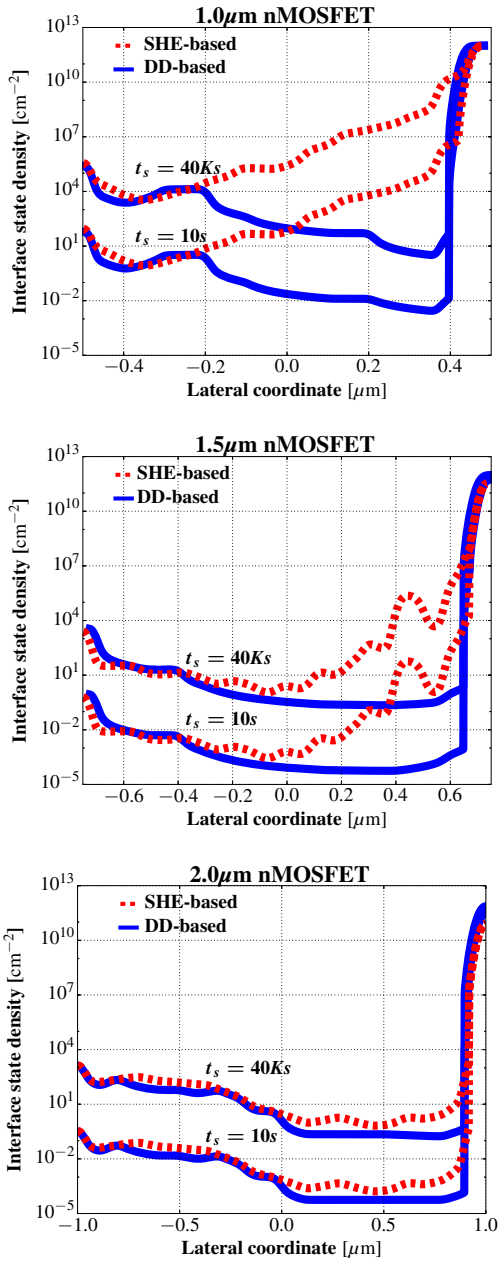

Fig. 6. (Color online) $N_{it}(x)$ profiles evaluated for the three nMOSFETs with gate lengths $L_G = 1.0$, 1.5, and 2.0 μm by both versions of the model for stress times of 10 s and 40 ks.

To check this in a greater detail we plot the acceleration integrals, which determine the corresponding rates, for the AB- and the MVE-mechanism simulated along the Si/SiO_2 interface with both versions of the model (see Fig. 5). For the 2 μm device the bond-breakage rates for the AB- and MVE-process are almost the same. This reflects the good agreement of the DFs in Fig. 4. For the shorter structures, the acceleration integrals of both mechanisms calculated with the two versions of the model are significantly different. Since in these devices the interface state profiles $N_{it}(x)$, and therefore also the degradation, are mainly determined by the AB-process, the DD-based version of our model should be able to properly capture the HCD traces for the 1.5 μm structure. The situation deteriorates for the shortest device. Although the contribution of the MVE-mechanism is properly represented by the simplified approach, the bond-breakage rates of the AB-process are profoundly underestimated. While the SHE-based versions predicts a significant build up of interface states in the channel, triggered by the interplay between the AB- and MVE-mechanism, which is not adequately described by the DD-based approach.

In order to investigate the mismatch of the DFs (Fig. 4) and the impact of the bond-breakage rates (Fig. 5) onto the interface trap profiles, we plot the $N_{it}(x)$ values simulated with both versions of the model (see Fig. 6). One can see that in the case of the longest device, i.e., the 2 μm nMOSFET structure, the $N_{it}(x)$ profiles are very similar. This is caused by the fact that the electron DFs are properly approximated by the DD-based model as can be seen in Fig. 4. The situation starts to change for the shorter structure with $L_G = 1.5\,\mu m$, i.e., agreement between both models deteriorates. For the device with $L_G = 1.5\,\mu m$ the discrepancy between the $N_{it}(x)$ values is visible at $N_{it} \sim 10^8\,cm^{-2}$. The N_{it} peak at the drain side becomes broader and is shifted towards the channel as

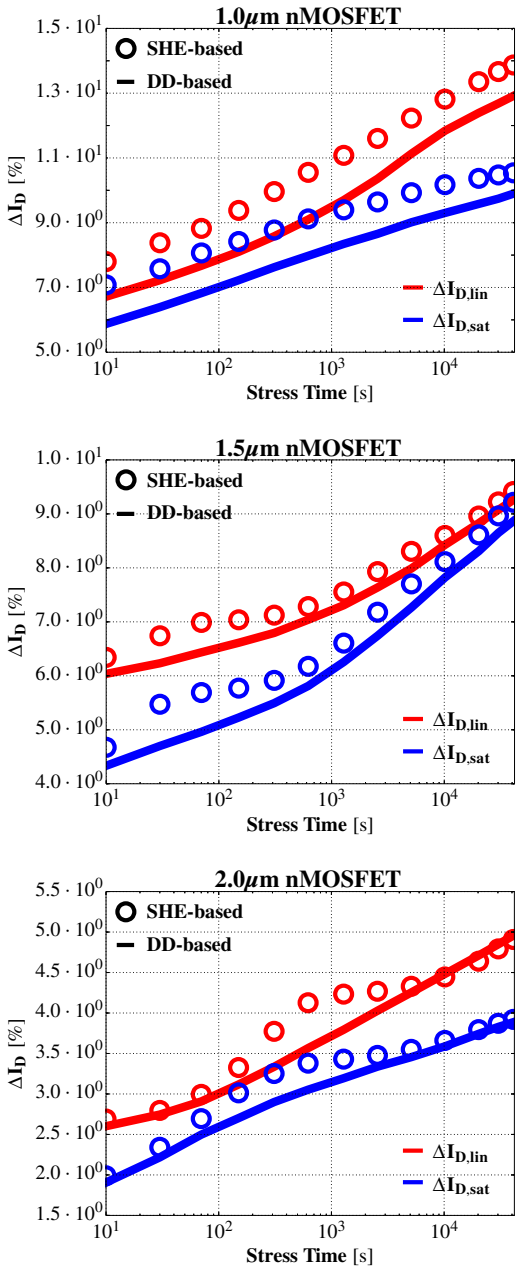

Fig. 7. (Color online) $\Delta I_{D,lin}$ and $\Delta I_{D,sat}$ degradation curves obtained for the three nMOSFETs with both versions model.

can be concluded from Fig. 5. The DD-based approach is not able to capture this trend. Since N_{it} values of $\sim 10^8\,cm^{-2}$ do not contribute to the total device degradation, a significant deviation between the $\Delta I_{D,lin/sat}$ degradation curves simulated by the two model versions is not expected. For the shortest device, however, the interface trap densities already differ by about $\sim 10^{12}\,cm^{-2}$. Such large values provide a considerable contribution to HCD and lead to a visible discrepancy between the drain current degradation traces.

As a result, best correspondence between $\Delta I_{D,lin/sat}$ obtained with the SHE- and DD-based models is achieved for the 2.0 µm nMOSFET (see Fig. 7). Note, however, that even for this device the analytic model leads to lower $\Delta I_{D,lin/sat}$ values at short stress times. This is because, as we showed in Refs. 22 and 25, short-term HCD is determined by the DFs at the drain, which are underestimated by the DD-based model (see Fig. 4). The same argument also holds for the 1.5 µm device where the agreement is still reasonable. Hot carrier degradation is slightly underestimated over the whole stress time range due to the mismatch of the interface state profiles visible in Fig. 6. For the shortest device the DD-based model completely fails to properly reproduce the data evaluated with the full model. This already becomes evident in Figs. 4–6 where one can see that the DD-based model is not capable of reasonable mimicking the ViennaSHE results, respectively the big discrepancies between the shape of the interface state profiles.

4. Conclusion

We have found that the drift-diffusion based hot-carrier degradation model works reasonably well in terms of the carrier distribution functions, bond-breakage rates, interface state density profiles, and changes of device characteristics such as the saturation and drain currents for MOSFETs with channels longer than 1.5 µm. The reason is that the DD-based model is not able to catch more complicated DF shapes visible in shorter devices. This is especially pronounced at high energies because the DFs simulated with ViennaSHE and by the DD-based HCD model have different curvatures.

In the case of the 2 µm device the curvature change occurs only when the DF values have dropped by several orders of magnitude, and therefore such a discrepancy does not translate into mismatches between bond-breakage rates, $N_{it}(x)$ profiles and $\Delta I_{D,lin}(t)$, $\Delta I_{D,sat}(t)$ degradation traces. As for shorter devices, the discrepancy in the DF curvature appears at higher population numbers, and thus is related to more pronounced errors. In the device with $L_G = 1.5$ µm this results in a mismatch in $N_{it}(x)$ profiles visible at $10^8\,cm^{-2}$, and thereby does not substantially impact the $\Delta I_{D,lin}(t)$, $\Delta I_{D,sat}(t)$ changes. As for the shortest nMOSFET, N_{it} values differ severely at values of $10^{12}\,cm^{-2}$, and hence the changes of the linear and saturation drain currents simulated with the two versions of the model are completely inconsistent. To summarize, our DD-based model for hot-carrier degradation works properly for the device with $L_G = 2.0$ µm, it is still applicable in the case $L_G = 1.5$ µm, and fails for $L_G = 1.0$ µm.

Acknowledgments

The authors acknowledge support by the Austrian Science Fund (FWF), Grant P23598 and by the European Union FP7 projects ATHENIS 3D (Grant No. 619246) and MoRV (Grant No. 619234).

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