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Electronic properties of dislocations

M. Reiche[1,a], M.Kittler[2,b], E. Pippel[1,c], H. Kosina[3,d], A. Lugstein[4,e], and H. Uebensee[5,f]

[1]Max Planck Institute of Microstructure Physics, Halle, Germany,

[2]Brandenburg University of Technology Cottbus-Senftenberg, Cottbus, Germany

[3]Institute for Microelectronics, Vienna University of Technology, Vienna, Austria

[4]Institute of Solid State Electronics, Vienna University of Technology, Vienna, Austria

[5]CIS Research Institute of Microsensorics, Erfurt, Germany

[a]reiche@mpi-halle.de (corresponding author), [b]kittlerm@tu-cottbus.de; [c]epip@mpi-halle.mpg.de, [d]kosina@iue.tuwien.ac.at, [e]alois.lugstein@tuwien.ac.at, [f]huebensee@cismst.de

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Abstract. Dislocations are one-dimensional crystal defects. Their dimension characterize the defects as nanostructures (nanowires). Measurements on defined dislocation arrays proved numerous exceptional electronic properties. A model of dislocations as quantum wires is proposed. The formation of the quantum wire is a consequence of the high strain level on the dislocation core modifying locally the band structure.

Introduction

Defect engineering has a widespread and sophisticated application in the fabrication of microelectronic devices. Entering nanoscale, however, changes the concept of defect engineering dramatically. Actual 22 nm technologies already implemented three-dimensional transistor structures (FinFETs) characterized by fin widths of about 10 nm as well as lengths and heights of about 30 nm, respectively, resulting in a volume of an individual fin of $9 \cdot 10^{-18}$ cm^3 corresponding to about $5.4 \cdot 10^6$ atoms. Assuming typical channel doping within the low 10^{-18} cm^{-3} regime [1] no more than 10 doping atoms are present per fin. This indicates that defect engineering moves to single atom treatments and a consequent transition to single electron transistors including the employment of quantum mechanical properties associated to the wave behavior of single excess carriers [2].

The continuous scaling requires strong efforts on technology combined with enormous economic resources. Therefore, it is obvious to consider alternative device concepts. One could be the conscious application of dislocations having diameters of a few square nanometers, i.e. in the same order as channel widths of FinFETs in the near future. Dislocations are electrically active, even if they are free of impurities. For instance, the diode characteristics of individual edge dislocations running through the whole wafer was demonstrated some time ago [3,4]. More recent studies proved an increase of the diode current of five orders of magnitude, or more, if defined dislocations arrays are applied. The current density through a single dislocation was estimated to be $3.8 \cdot 10^{12}$ A/cm^2. This corresponds to a resistivity of $1 \cdot 10^{-8}$ Ωcm which is about eight orders of magnitude lower than of the surrounding silicon matrix and indicates a supermetallic behavior of dislocations [5]. An increase of the current was proved for dislocations in n- and p-type Si, suggesting the transport of electrons or holes via identical defects. The present paper deals with the question, why different carriers are transported via dislocations having the same atomic structure.

Fabrication of defined dislocation arrays

Studies of individual or a few dislocations require methods to generate defined types and numbers of these defects and their integration into an efficient measurement device. A technique to realize

two-dimensional arrays of dislocations in thin layers (semiconductor wafer bonding) was described elsewhere [5,6]. Silicon-on-insulator (SOI) wafers (diameter 150 mm, <100> orientation, buried oxide (BOX) thickness 60 nm, device layer thickness 30 nm) were used. Bonding two of them (hydrophobic conditions were applied) and subsequent annealing result in a new SOI wafer having a device layer thickness of 60 nm containing a two-dimensional dislocation network close to the middle (Fig. 1a, b).

MOSFETs were prepared on such SOI substrates using standard CMOS processes [5,6]. The gate length L was fixed to 1 µm, while different gate widths W were applied in order to study the effect of different dislocation numbers under the same conditions. Devices were fabricated parallel to both <110> directions, i.e. parallel to both sets of dislocations (Fig. 1c).

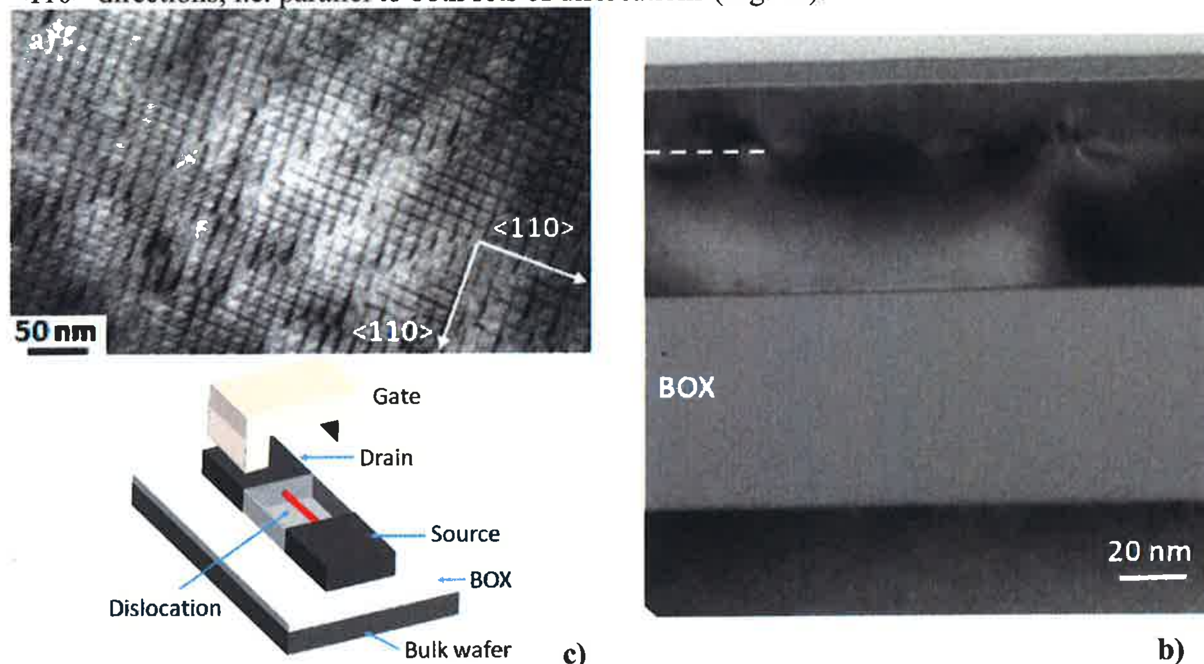

Fig. 1: *TEM plan view of a periodic dislocation network (a) and the corresponding cross-section image ({110}-plane) through the SOI stack with the dislocation network (dotted line) in the 60 nm thick device layer (b). Schema of a MOSFET with a dislocation (red line) in the channel (c). The gate was lifted for clearness. Devices are fabricated parallel to both <110> directions, i.e. parallel to the dislocation line directions.*

Structure and electrical characterization

Different electron microscopy techniques have been applied to analyze the structure of individual dislocations in two-dimensional arrays [7]. Weak beam techniques performed on {100} plane-view samples as well as high-angle annular dark field (HAADF) imaging on {110}-oriented cross-sections indicate the dissociation of screw dislocations into two 30° partials (Fig. 2a). Local strain field measurements by peak-pairs analysis (PPA) [5] proved high amounts of strain ε on the cores of the partial dislocations which are significantly higher than in the strain field surrounding the defect. For 30° partials the strain close to the core is uniaxial tensile and exceeds $\varepsilon \cong +0.1$ (10%). Furthermore, reactions of (dissociated) screw and 60° dislo-

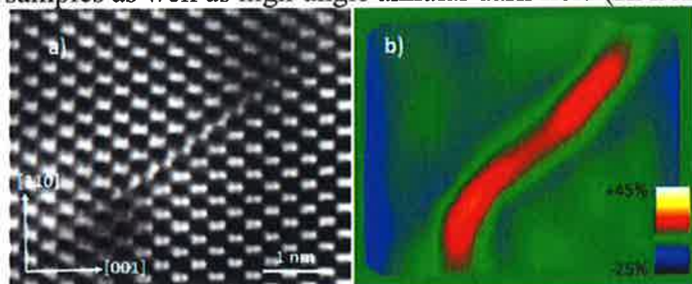

Fig. 2: *HAADF cross-section image (a) of a dissociated screw dislocation (a) and corresponding strain measured by PPA (b). Red colour indicates tensile strain of $\varepsilon \cong +0.1$.*

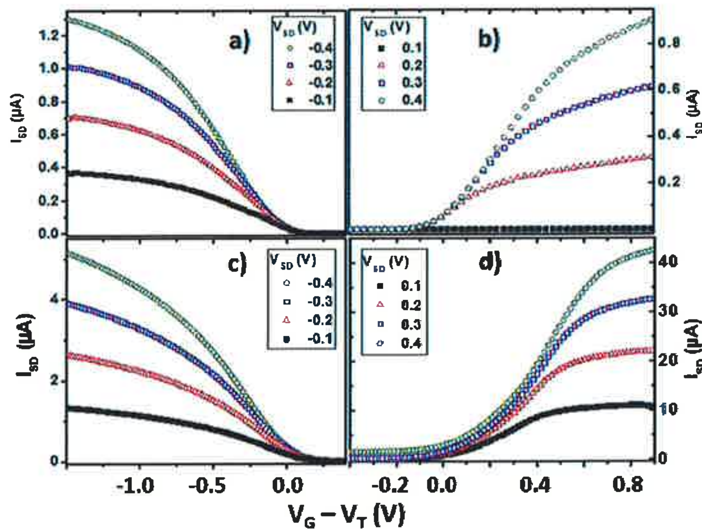

Fig. 3: *Transfer characteristics (I_{SD}-V_G) of p- and nMOSFETs without (a, b) and with dislocations in the channel (c, d). V_G is represented as difference V_G-V_T as the threshold voltage. The channel length and width, resp., are 1 µm for all devices.*

cations result in new defects having uniaxial tensile ($\varepsilon \cong +0.1$) and uniaxial compressively strained ($\varepsilon \cong -0.1$) branches [8].

Electrical measurements performed on n- and pMOSFETs result in a significant increase of the drain current I_{SD} if dislocations are present in the device channel (Fig. 3). An increase of the drain current by a factor of five is obtained for pFETs, while I_{SD} increases by a factor of 40, or more, for nFETs. The increase of the drain current depends not only on the dislocation type (screw dislocations for nFETs and dislocations with edge components for pFETs), but also on the number of dislocations in the channel [6]. The largest increase of I_{SD} is obtained if only one dislocation exists in the channel [5].

The interpretation of the increase of I_{SD} by dislocations is complex. First, as noted before, the dislocation type effects the drain current increase. For instance, pure screw dislocations result in the highest increase of I_{DS} for nFETs suggesting that electrons are predominantly transported via this dislocation type. On the other hand, I_{SD} decreases significantly for pFETs if screw dislocations are present. This is explained by recombination of injected holes with existing electrons on screw dislocations [9]. The increase of I_{SD} might be also caused by higher carrier concentrations and/or mobilities. Low-temperature measurements demonstrated the presence of an one-dimensional electron gas (1DEG) and single-electron transitions (Coulomb blockades) on screw dislocations [10]. Indications to the existence of an one-dimensional hole gas (1DHG) have been also observed for mixed dislocations [8]. These findings demonstrate that dislocations are nanowires having exceptional electronic properties.

Quantum mechanical simulations

The remarkable increase of the transport of electrons or holes along dislocations cannot be explained by different (atomic) structures of these defects. TCAD simulations of the output and transfer characteristics of nMOSFETs having screw dislocations in the channel refer to about 200 electrons per micrometer dislocation length. This corresponds to the maximum number of electrons on a dislocation [11]. Assuming a homogeneous distribution along the dislocation line, the distance between free electrons on the dislocation core would be about 5 nm, which is significantly smaller than the distance of dislocation nodes in the network (about 30 nm) and means that electrons are located on straight dislocation segments. Furthermore, the location of free carriers on core defects (kinks) or hopping processes of carriers along the dislocation core are also neglected [9]. Therefore the assumption of a metallic-like behavior caused by a one-dimensional carrier confinement along dislocation lines appears most reasonable and confirms experimental findings as well as conclusions drawn by other authors [12,13]. The reason of the carrier confinement is the exceptional high strain on the dislocation core, which exceeds 10 % and is about two orders of magnitude higher than in the strain field surrounding a dislocation (e.g. [14]). Such high strain values cause dramatic changes of the band structure and therefore of the electronic properties.

Quantum mechanical simulations were performed to study the effect of strain on the band structure. Here, the nextnano^3 simulation package [15] was applied. The bulk band structure was calcu-

lated using 6- and 8-band-**k.p** models and an empirical $sp^3d^5s^*$ tight binding model [16] taking into account strain and deformation potentials. Both, tight binding and **k.p** methods are frequently applied to calculate band structures in strained systems [17,18]. Shifts of the conduction and valence bands at the Γ- and L points as well as band warping exist with increasing uniaxial tensile strain. The conduction band minimum at Δ is nearly unchanged with increasing tensile strain, If $\varepsilon = +0.1$, the lowest conduction band at the Γ point is equal to the position of the lowest conduction band at Δ of the unstrained Si (Fig. 4a). As a result, the band gap energies of the indirect and direct transitions are equal for such high tensile strain and silicon changes from the indirect into a direct semiconductor. This is in agreement with previously reported data [19]. Furthermore, the shift of the conduction band minimum at the L point results in an additional indirect transition in the presence of high uniaxial tensile strain with a band gap energy of about 0.9 eV. This causes that the dislocation forms a quantum wire in the unstrained silicon channel. The cross-section through the dislocation yields a quantum well (Fig. 4b) formed by the minimum of the lowest conduction band at the L point (E_{CB}^{L}) of the tensile strained silicon and that of Δ of the surrounding unstrained silicon (E_{CB}^{Δ}). Solving the Schrödinger equation for an infinite cylindrical potential to model one-dimensional wires, on obtains solutions for quantized energy levels [20]

$$E_i = \frac{\hbar^2}{2m_e}\frac{J_0(x)^2}{R^2} \quad , \qquad (1)$$

with $J_0(r)$ as the first root of the Bessel function, $\hbar$ the reduced Planck constant and R as the radius of the quantum wire. With $m_e = 0.19m_0$ and $R = 2.5$ nm, one obtains the lowest energy levels $E_1 = 38.4$ meV and $E_2 = 203$ meV. Both are inside the quantum wire formed by the dislocation (Fig. 4b).

Increasing uniaxial compressive strain yields that the indirect transition between the minimum of the lowest conduction band at the Δ point and the valence band maximum at the Γ point decreases continuously (Fig. 4a). The gap is only 40 meV if an uniaxial compressive strain of $\varepsilon = -0.1$ is applied. The minima at the lowest conduction bands at Γ and L are also shifted down with increasing compressive strain. But the band gap at the Γ point is about 1.2 eV for $\varepsilon = -0.1$. An equivalent value is measured for the second indirect transition between L and Γ points. Besides shifts of the conduction bands, shifts of the valence bands combined with splitting and warping appear if uniaxial

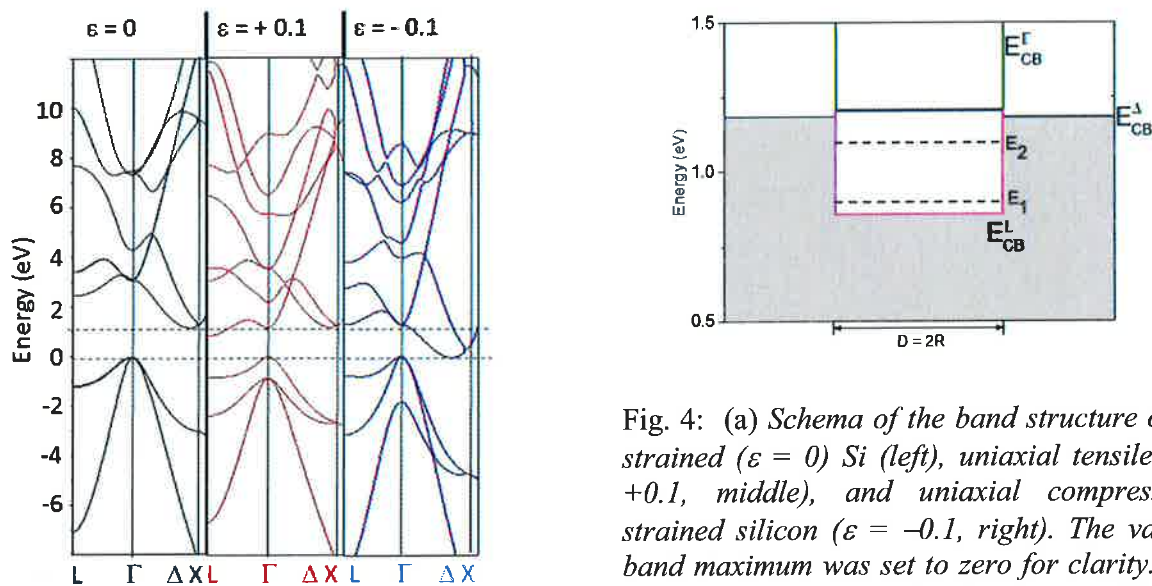

Fig. 4: (a) *Schema of the band structure of unstrained (ε = 0) Si (left), uniaxial tensile (ε = +0.1, middle), and uniaxial compressively strained silicon (ε = –0.1, right). The valence band maximum was set to zero for clarity. Dotted lines characterize the band gap of the unstrained Si.*
(b) Conduction bands forming the quantum wire of diameter D. Uniaxial tensile strain of ε = +0.1 is assumed for dislocation. Dashed lines characterize the first energy levels calculated for the quantum wire.

compressive strain is applied [8]. The upward shift of the valence band maxima of heavy and light holes result also in a quantum wire.

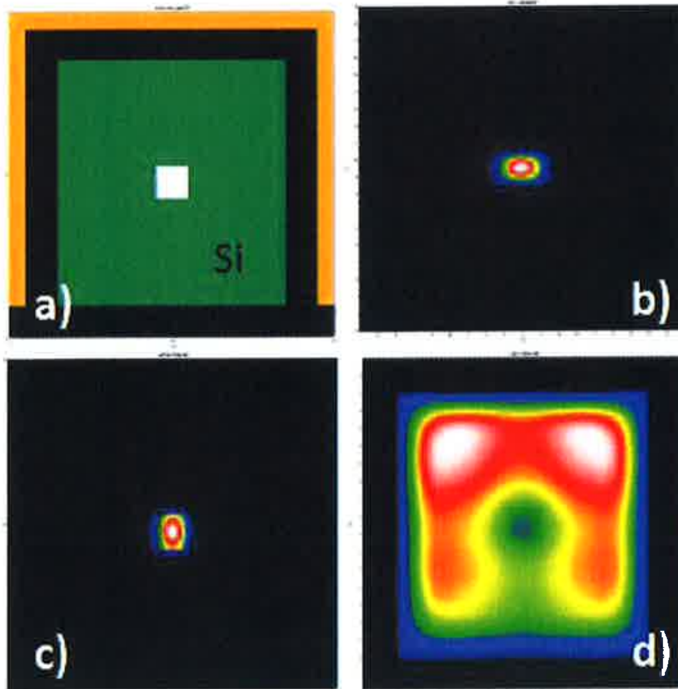

Fig. 5: *Two-dimensional quantum mechanical device simulation. Schema of the nMOSFET with channel width and height of 20 nm (a). The channel (green) is unstrained silicon with a dislocation (2nm x 2 nm) in the center (white). Gate oxide and BOX are drawn in black, while the gate electrode is shown in yellow colour. The first wave function is localized in the dislocation if uniaxial tensile strain (ε = +0.1) is applied (b). Electron densities for devices with a dislocation in the center (c) and an unstrained Si channel (d). Red colour means the highest and black the lowest electron densities. The gate voltage is $V_G = 0.5V$.*

The most important result of band structure calculation is that uniaxial tensile or compressive strain cause band alignments resulting in confinement effects of carriers along dislocations (quantum wire). The effect of the carrier confinement on the MOSFET characteristics was also studied by device simulations. Here, a two-dimensional quantum mechanical device simulation package (nextnano^3) was applied allowing the self-consistent solution of the two-dimensional Poisson, Schrödinger, and current equations. The device used for simulation is schematically shown in Fig. 5a. An unstrained silicon channel (20 nm x 20 nm) is used. A dislocation is assumed as a square of 2 nm x 2 nm in the center of the channel. Adapting the modified band parameters resulting from a uniaxial tensile strained dislocation (ε = +0.1) cause a localization of the first wave function inside the dislocation (Fig. 5b). This leads to the highest electron concentration inside the dislocation (Fig. 5c) and therefore to the dominant current flow through the defect. On the other hand, the highest electron density is close to the gate if an unstrained silicon channel without a dislocation is used (Fig. 5d). Note that a preferred current flow through the dislocation is only obtained by the carrier confinement because of band alignment induced by the high uniaxial strain. Mobility enhancement only by reduced effective masses is not the primary reason.

Conclusions and prospective applications

Caused by their dimensions, dislocations represent native nanostructures embedded in a perfect crystalline matrix. Their exceptional electronic properties are attributed to carrier confinement by high uniaxial strain in the defect core, which modifies dramatically the band structure. The strain in a dislocation core exceeds 10% and can be either tensile (for screw dislocations) or compressive for edge dislocations. Branches with tensile and compressive components exist for mixed dislocations. The latter allows the simultaneous transport of electrons and holes via the same defect.

The exceptional electronic properties of defined arrangements of dislocations provide numerous potential applications in novel silicon-based devices. For instance, the existence of a two-dimensional net of 1DEGs on dislocation networks suggests the realization of single electron transistors. Single electron transitions related to dislocations were proved at low temperatures [10]. The detection at higher temperatures, however, is missing up to now. On the other hand, low-temperature operation of MOSFETs is an important issue for several cryogenic applications [21].

The high carrier concentration on dislocations enables also MOSFET operation without additional doping even at $T \leq 5$ K. This is mainly caused by reduced freeze out of carriers.

Besides the integration of dislocations into transistors as a tool to increase their performance, other application areas were discussed. One could be the utilization as thermoelectric material. Bulk silicon is a poor thermoelectric (figure of merit of $ZT_{300\,K} \cong 0.01$) but an increase of ZT by a factor of 100 was expected for Si nanowires because of a decrease of the thermal conductivity due to increased phonon scattering [22]. The electrical resistivity and Seebeck coefficient, however, are not affected for nanowires. The incorporation of defined dislocations in thin SOI layers promises also an increase of ZT but assumes a different approach. As described above, the incorporation of defects into thin silicon layers reduces the electrical resistivity ρ considerably. While $ZT \sim 1/\rho$, a significant increase of ZT follows. Moreover, an increase of the Seebeck coefficient by incorporation of dislocations is expected resulting in an additional increase of the figure of merit [23].

References

[1] C.H. Lin, R. Kambhampati, R.J. Miller, T.B. Hook, A. Bryant, W. Haensch, P. Oldiges, I. Lauer, T. Yamashita, V. Basker, T. Standaert, K. Rim, E. Loeobandung, H. Bu, and M. Khare, *2012 Symposium on VLSI Technology, Digest*, 15 (2012).
[2] E. Prati and T. Shinada, *IEDM Techn. Digest*, 1.2.1. (2014).
[3] F. Calzecchi, P. Gondi, and F. Schintu, *Nuovo Cimento* **58B**, 376 (1968).
[4] V.G. Eremenko, V.I. Nikitenko, and A.B. Yakimov, *Sov. Phys. - JETP* **40**, 570 (1975).
[5] M. Reiche, M. Kittler, W. Erfurth, E. Pippel, K. Sklarek, H. Blumtritt, A. Haehnel, and H. Uebensee, *J. Appl. Phys.* **115**, 194303 (2014).
[6] M. Reiche, M. Kittler, D. Buca, A. Hähnel, Q.-T. Zhao, S. Mantl, and U. Gösele, *Jpn. J. Appl. Phys.* **49**, 04DJ02 (2010).
[7] M. Reiche, M. Kittler, H. Uebensee, E. Pippel, and S. Hopfe, *Adv. Nano Research* **2** (1), 1 (2014).
[8] M. Reiche, M. Kittler, E. Pippel, W. Erfurth, A. Haehnel, and H. Uebensee, *Phys. Stat. Sol. (c)*, in press (2015).
[9] M. Reiche, M. Kittler, M. Krause, and H. Übensee, *Phys. Stat. Sol. (c)* **10**, 40 (2013).
[10] M. Reiche, M. Kittler, M. Schmelz, R. Stolz, H. Uebensee, M. Kehrmann, and T. Ortlepp, *J. Phys. Conf. Ser.* **568**, 052024 (2014).
[11] V. Kveder and M. Kittler, *Mat. Sci. Forum* **590**, 29 (2008).
[12] R. Labusch and W. Schröter, in *Dislocations in Solids*, F.R.N. Nabarro, Editors, Vol. 5, pp. 127, North-Holland, Amsterdam (1980).
[13] E. Abrahams, S.V. Kravchenko, and M.P. Sarachik, *Rev. Mod. Phys.* **73**, 251 (2001).
[14] M. Couillard, G. Radtke, and G.A. Botton, *Phil. Mag.* **93**, 250 (2013).
[15] S. Birner, T. Zibold, T. Andlauer, T. Kubis, M. Sabathil, A. Trellakis, and P. Vogl, *IEEE Trans. Electron. Dev.* **54**, 2137 (2007).
[16] J.-M. Jancu, R. Scholz, F. Beltram, and F. Bassani, *Phys. Rev. B* **57**, 6493 (1998).
[17] M.V. Fischetti, Z. Ren, P.M. Solomon, M. Yang, and K. Rim, *J. Appl. Phys.* **94** (2), 1079 (2003).
[18] V. Sverdlov, *Strain-induced effects in advanced MOSFETs*, Springer, Wien (2011).
[19] S.Z. Karazhanov, A. Davletova, and A. Ulyashin, *J. Appl. Phys.* **104**, 024501 (2008).
[20] W. Lu, J. Xiang, B.P. Timko, Y. Wu, and C.M. Lieber, *PNAS* **102**, 10046 (2005).
[21] M. Reiche, M. Kittler, H. Uebensee, E. Pippel, and W. Erfurth, *ECS Trans.* **64(11)**, 267 (2014).
[22] A.I. Hochbaum, R. Chen, R.D. Delgado, W. Liang, E.C. Garnett, M. Najatian, A. Majumdar, and P. Yang, *Nature*, 163 (2008).
[23] N. Neophytou, X. Zianni, H. Kosina, S. Frabboni, B. Lorenzi, and D. Narducci, *Nanotechnology* **24**, 205402 (2013).

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10.4028/www.scientific.net/SSP.242

Electronic Properties of Dislocations
10.4028/www.scientific.net/SSP.242.141

DOI References

[1] C.H. Lin, R. Kambhampati, R.J. Miller, T.B. Hook, A. Bryant, W. Haensch, P. Oldiges, I. Lauer, T. Yamashita, V. Basker, T. Standaert, K. Rim, E. Loeobandung, H. Bu, and M. Khare, 2012 Symposium on VLSI Technology, Digest, 15 (2012).
10.1109/vlsit.2012.6242438
[3] F. Calzecchi, P. Gondi, and F. Schintu, Nuovo Cimento 58B, 376 (1968).
10.1007/bf02711811
[5] M. Reiche, M. Kittler, W. Erfurth, E. Pippel, K. Sklarek, H. Blumtritt, A. Haehnel, and H. Uebensee, J. Appl. Phys. 115, 194303 (2014).
10.1063/1.4876265
[6] M. Reiche, M. Kittler, D. Buca, A. Hähnel, Q. -T. Zhao, S. Mantl, and U. Gösele, Jpn. J. Appl. Phys. 49, 04DJ02 (2010).
10.1143/jjap.49.04dj02
[7] M. Reiche, M. Kittler, H. Uebensee, E. Pippel, and S. Hopfe, Adv. Nano Research 2 (1), 1 (2014).
10.12989/anr.2014.2.1.001
[8] M. Reiche, M. Kittler, E. Pippel, W. Erfurth, A. Haehnel, and H. Uebensee, Phys. Stat. Sol. (c), in press (2015).
10.1002/pssc.201400298
[9] M. Reiche, M. Kittler, M. Krause, and H. Übensee, Phys. Stat. Sol. (c) 10, 40 (2013).
10.1002/pssc.201200537
[10] M. Reiche, M. Kittler, M. Schmelz, R. Stolz, H. Uebensee, M. Kehrmann, and T. Ortlepp, J. Phys. Conf. Ser. 568, 052024 (2014).
10.1088/1742-6596/568/5/052024
[13] E. Abrahams, S.V. Kravchenko, and M.P. Sarachik, Rev. Mod. Phys. 73, 251 (2001).
10.1103/revmodphys.73.251
[15] S. Birner, T. Zibold, T. Andlauer, T. Kubis, M. Sabathil, A. Trellakis, and P. Vogl, IEEE Trans. Electron. Dev. 54, 2137 (2007).
10.1109/ted.2007.902871
[16] J. -M. Jancu, R. Scholz, F. Beltram, and F. Bassani, Phys. Rev. B 57, 6493 (1998).
10.1103/physrevb.57.6493
[17] M.V. Fischetti, Z. Ren, P.M. Solomon, M. Yang, and K. Rim, J. Appl. Phys. 94 (2), 1079 (2003).
10.1063/1.1585120
[18] V. Sverdlov, Strain-induced effects in advanced MOSFETs, Springer, Wien (2011).
10.1007/978-3-7091-0382-1_3
[19] S.Z. Karazhanov, A. Davletova, and A. Ulyashin, J. Appl. Phys. 104, 024501 (2008).
10.1063/1.2940135
[20] W. Lu, J. Xiang, B.P. Timko, Y. Wu, and C.M. Lieber, PNAS 102, 10046 (2005).
10.1073/pnas.0504581102
[21] M. Reiche, M. Kittler, H. Uebensee, E. Pippel, and W. Erfurth, ECS Trans. 64(11), 267 (2014).

10.1149/06411.0267ecst
[22] A.I. Hochbaum, R. Chen, R.D. Delgado, W. Liang, E.C. Garnett, M. Najatian, A. Majumdar, and P. Yang, Nature, 163 (2008).
10.1038/nature06381
[23] N. Neophytou, X. Zianni, H. Kosina, S. Frabboni, B. Lorenzi, and D. Narducci, Nanotechnology 24, 205402 (2013).
10.1088/0957-4484/24/20/205402