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Electromigration Induced Voiding and Resistance Change in Three-Dimensional Copper Through Silicon Vias

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***Abstract*—Open through silicon vias are direct vertical connections between different integration levels of a chip which provide higher performances per unit area in three-dimensional integrated circuits. The reliability of such structures in integrated circuits constitutes an important issue in microelectronics. This paper deals with electromigration reliability and lifetime evaluation of open copper through silicon vias. The model for electromigration induced voiding is proposed to describe the resistance change with time during the reliability analysis. The model is derived by considering two distinctive failure phases, namely void initiation and void evolution, and their contributions on the complete interconnect lifetime estimation. Numerical calculations are carried out to reproduce the physical phenomenon. The resistance trace shows the typical initial flat constant part followed by non-linear time increase. Therefore, simulation results provide a good description of the time resistance change and, consequently, the electromigration lifetime evaluation in open copper through silicon vias.**

***Keywords*-Through Silicon Via; electromigration; time-to-failure; resistance trace; void**

I. Introduction

Today, three-dimensional (3D) integration technology has become one of the major development avenues for the fabrication of integrated circuits, which go beyond the conventional performances and capabilities achieved with planar two-dimensional (2D) architectures. 3D integrated circuits extensively utilize the third dimension to connect the multiple layers of active devices by using short wires in 3D designs [1]. These shorter wires are expected to alleviate the delay-related problems in planar 2D technologies by bringing the interconnect on-chip [2]. A number of new enabling technologies are introduced into the existing fabrication process flow to make 3D integration a reality. The most innovative way to exploit the vertical dimension efficiently is to employ the through silicon via (TSV), an electrical connection from the top to the bottom of a silicon wafer. 3D TSVs consist of short conducting vias that pass through a silicon wafer in order to minimize the chip size as well as to achieve greater interconnect density than wire bonding. Typically, the interplane via is etched and filled with rather thick copper [2]. Besides its several advantages, big concerns in 3D integration with TSVs are influences of

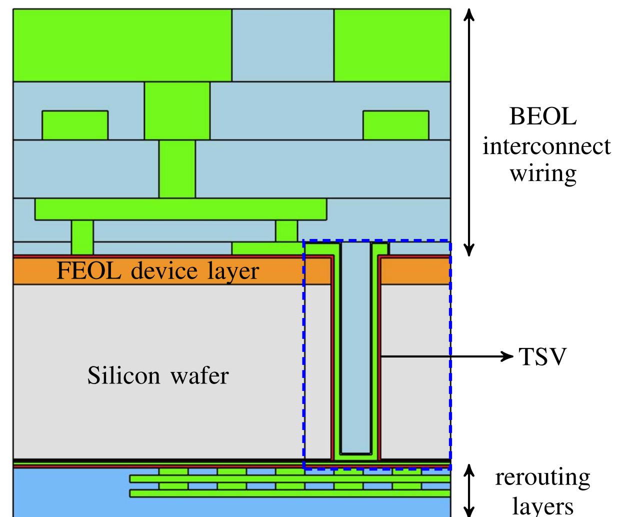

Figure 1: General cross section view of the 3D integration technology. The portion of the structure considered for simulations is highlighted (dashed blue rectangle).

metal contamination and mechanical stress generated in the region surrounding the TSV [3]. In particular, significant thermo-mechanical stresses are induced around the TSV, when the structure is subjected to temperature loadings, due to the large mismatch in coefficients of thermal expansion between the copper TSV and the silicon wafer. These stresses can be sufficiently high to influence the reliability of TSV-based 3D integration technologies. As a solution to overcome the thermo-mechanical issues induced by the material properties, a new concept for wafer-to-wafer integration based on open TSV technology has been introduced [4]. Figure 1 shows a schematic overview of a 3D integration technology using open TSV, front-end of line (FEOL) device layer, rerouting layers and back-end of line (BEOL) interconnects. Although 3D open TSVs show distinguishing advantages and the TSV process has almost reached the status of being a full-grown progress [4], reliability concerns may always occur in these new emerging technologies.

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Electromigration (EM) is one of the key reliability issues in BEOL interconnects. It mainly refers to the wear-out failure mechanism caused by the material transport due to current flow in metal lines. Typically, EM wear-out mechanism is characterized by the nucleation of voids that grow and trigger chip failure. In 3D TSV technologies, geometric features and material properties of the diverse metallic layers can lead to EM induced voiding under the TSV. Voids nucleate especially at those locations in the structure where the adhesion between the copper line and the surrounding layer is weak. These sites are generally observed close to the metallization barrier between the TSV and the adjacent metal level [5]. Consequently the void nucleation interfaces are the key items regarding the beginning of the interconnect failure mechanism.

The EM failure development is normally described by the interconnect resistance change with time. The EM resistance trace can be obtained by monitoring the electrical resistance of an interconnect under accelerated test conditions of increased temperature and current [5]. The interconnect resistance as a function of time is typically divided in two parts (Figure 2). The first part, namely void initiation phase, is characterized by the nucleation of a void which remains electrically undetectable. Therefore the interconnect resistance remains constant during the entire void initiation period. The nucleation of a void is the beginning of the second part, which is called void evolution phase. During this phase, the void evolution mechanism leads to a rapid nonlinear interconnect resistance increase. The interconnect fails after a maximum tolerable resistance level is reached. Time-to-failure (TTF) is defined as the time needed to achieve this maximum resistance value. Consequently, the prediction of the EM TTF becomes crucial for the assessment of the interconnect reliability.

In this work we investigate the EM reliability issues in a 3D open copper TSV structure. First, we identify the locations with the highest probability of void nucleation in such interconnect structures by solving the EM model equations employing the finite element method (FEM). Then, the resistance change due to the growing void in the TSV is modeled based on 3D numerical simulations. The interconnect EM TTF estimation is consequently studied by proposing an analytic expression based on the void evolution kinetic. Finally, the comparison between simulation results and Black's equation provides a good agreement in the lifetime estimation for open copper TSV technology.

II. Modeling

EM failure mechanism is characterized by the development of the resistance as a function of time in the interconnect line. Two periods are observed in the EM resistance trace: a first flat constant part, followed by a sudden nonlinear increase period. During the first period a small void nucleates and does not influence the current flow in the interconnect. As soon as the void size becomes larger, a measurable resistance increase with time begins. Thus, the complete EM failure time evaluation of the given BEOL interconnect requires both void initiation and void evolution times. The contribution of each component in the EM TTF estimation depends on different kinetic and physical effects. The analysis of both failure phases is necessary for a better understanding of the EM problem in interconnects. In the following sections we analyze in detail the EM modeling of each phase of failure development and their impact on the interconnect lifetime evaluation.

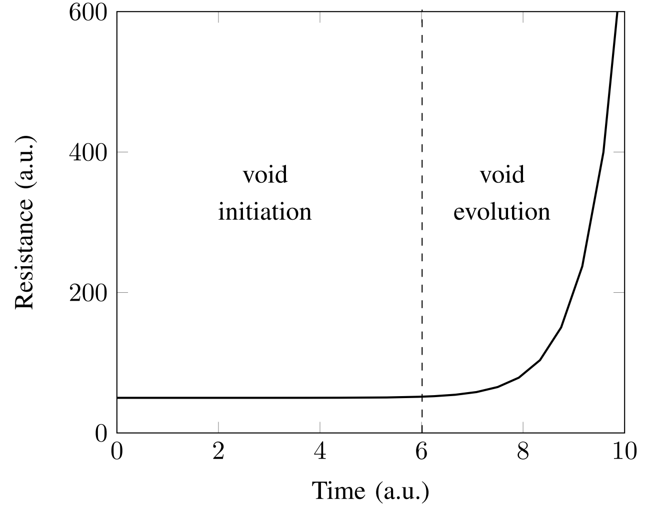

Figure 2: Typical EM resistance change with time for a given interconnect. Two EM failure phases are shown.

A. Void Initiation

EM refers to the migration of atoms in the direction of the electron flow in a metal line. The atomic flux creates material accumulation on one end of the line and material depletion on the opposite side. Material depletion is generally described by vacancy accumulation, which is due to the transport of vacancies in the opposite direction of the electron flow in the line. The accumulation of vacancies leads to void nucleation and to the beginning of the wear-out failure mechanism in the interconnect. The vacancy flux $\vec{J}_{\mathrm{v}}$ responsible for EM void nucleation failure in the conductor is induced by different driving forces [6] and can be written as

$$\vec{J}_{\mathrm{v}} = D_{\mathrm{v}} \left(\frac{e|Z^*|C_{\mathrm{v}}\rho\vec{j}}{k_{\mathrm{B}}T} - \nabla C_{\mathrm{v}} - \frac{f\Omega C_{\mathrm{v}}\nabla\sigma}{k_{\mathrm{B}}T} \right), \qquad (1)$$

where e is the elementary charge, Z^* is the effective valence, k_{B} is the Boltzmann constant, T is the temperature, D_{v} is the vacancy diffusion coefficient, C_{v} is the vacancy concentration, ρ is the metal resistivity, $\vec{j}$ is the electrical current density, f is the vacancy relaxation factor, Ω is the atomic volume, and σ is the hydrostatic stress. The first

flux term on the right-hand side represents the flux induced by EM, while the other terms are components of the back-flux [7]. The change of vacancy concentration caused by the vacancy flux in the metal structure can be commonly expressed by the continuity equation

$$\frac{\partial C_{\mathrm{v}}}{\partial t} = -\nabla \cdot \vec{J}_{\mathrm{v}} + G, \tag{2}$$

where G is the Rosenberg-Ohring function [8] that models creation and annihilation of vacancies at particular sites inside the line. In addition, the flux and the creation/annihilation of vacancies are accompanied by the development of inelastic strain in the line, which is the connection to the solid mechanics simulation [6]. The inelastic strain ϵ_{v} dynamics due to the pile up and the generation/annihilation of vacancies is given by

$$\frac{\partial \epsilon_{\mathrm{v}}}{\partial t} = \Omega\left[(1-f)\nabla \cdot \vec{J}_{\mathrm{v}} + fG\right]. \tag{3}$$

Metal responds to inelastic strains by deformations or the build-up of stresses. The development of mechanical stresses in the structure is calculated by solving (2) and (3) together with the mechanical equilibrium equation, and also by coupling the standard electro-thermal equations [9]. The time evolution of the EM induced stress in a metal interconnect typically follows a square root time dependence [10]. As soon as the stress build-up due to EM reaches a threshold magnitude σ_{thr}, void nucleation can occur at the sites of weakest adhesion in the structure. Gleixner *et al.* [11] derived a simple equation for the prediction of the threshold stress value for a given BEOL interconnect, which is dependent on material interfacial properties and initial nucleus radius. The time required to reach the threshold value is called void initiation time. It should be pointed out that the interconnect resistance change is practically negligible for the whole void initiation time period because small initial nucleus radii do not affect the electrical performances of the interconnect.

B. Void Evolution

Once the location of void nucleation is identified in the interconnect structure, EM induced failure is ultimately caused by the growth of the fatal void. During this step, the void growth is governed by vacancy diffusion. It has been shown that the electron wind is the most dominant driving force in the vacancy flux responsible for the EM void evolution failure [12]. Therefore, in this context, the back-flux term in (1) can be neglected. The EM flux increases the void volume by feeding it with vacancies. The void volume V_{v} change in time due to the captured vacancies by the void is given by

$$\frac{\partial V_{\mathrm{v}}}{\partial t} = f\Omega A_{\mathrm{i}}\vec{J}_{\mathrm{v}} = f\Omega A_{\mathrm{i}}\frac{e|Z^*|D_{\mathrm{v}}C_{\mathrm{v}}\rho\vec{j}}{k_{\mathrm{B}}T}, \tag{4}$$

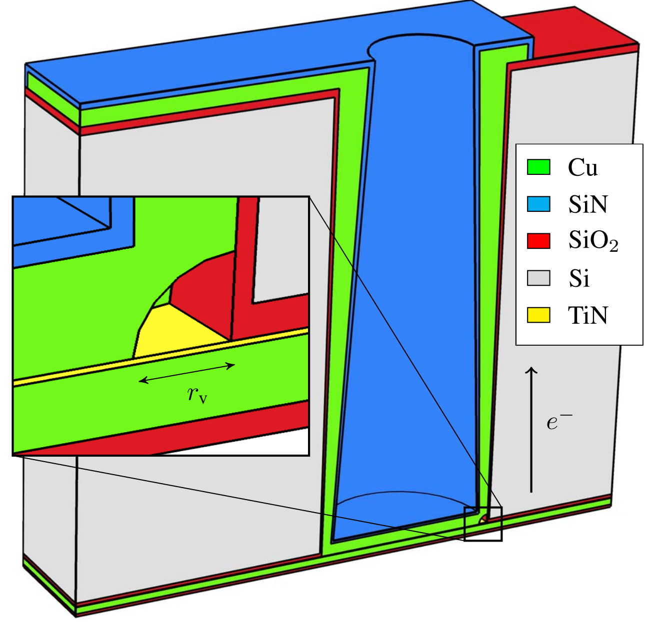

Figure 3: Profile view of the analyzed open copper TSV structure. The upper part of the interconnect layout is known as TSV top while the lower side is the TSV bottom. The TSV aspect ratio is 2.5:1 (TSV height / TSV width). The arrow shows the direction of the current flow. The zoomed-in detail view of the TSV bottom depicts the location of the initial spherical void.

where A_{i} is the cross sectional area of the given interconnect. Considering the case of an initial spherical void spanning the open TSV thickness (Figure 3), we can approximate its evolution, for local geometric features, as a quarter-spherical void growth as

$$\frac{\partial V_{\mathrm{v}}}{\partial t} = \pi r_{\mathrm{v}}^2\frac{\partial r_{\mathrm{v}}}{\partial t}, \tag{5}$$

where r_{v} is the void radius. Using (4) and (5), the void radius change in time is written as

$$\frac{\partial r_{\mathrm{v}}}{\partial t} = f\Omega A_{\mathrm{i}}\frac{e|Z^*|D_{\mathrm{v}}C_{\mathrm{v}}\rho\vec{j}}{\pi r_{\mathrm{v}}^2 k_{\mathrm{B}}T}. \tag{6}$$

The flux of vacancies captured by the void strongly depends on its size influencing the changes in current density and vacancy concentration distributions around the void itself as well [13]. Assuming a variable vacancy flux and integrating (6), the analytical model describing the time t necessary to grow a void of a given void radius becomes

$$t = t_0 + \frac{\pi}{\alpha}\int_{r_0}^{r}\frac{r_{\mathrm{v}}^2}{A_{\mathrm{i}}(r_{\mathrm{v}})C_{\mathrm{v}}(r_{\mathrm{v}})\vec{j}(r_{\mathrm{v}})}dr_{\mathrm{v}}, \tag{7}$$

where

$$\alpha = f\Omega\frac{e|Z^*|D_{\mathrm{v}}\rho}{k_{\mathrm{B}}T}, \tag{8}$$

and r_0 is the initial void radius corresponding to the time t_0. For each void size, the interconnect resistance is calculated

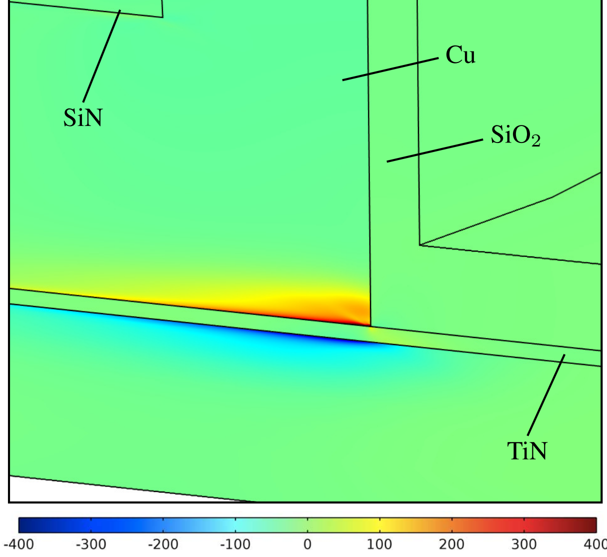

Figure 4: Profile view of the mechanical stress distribution (MPa) at the open copper TSV bottom after 10000 hours of current flow. The maximum tensile stresses are located at the Cu/TiN/SiO_2 layer intersection.

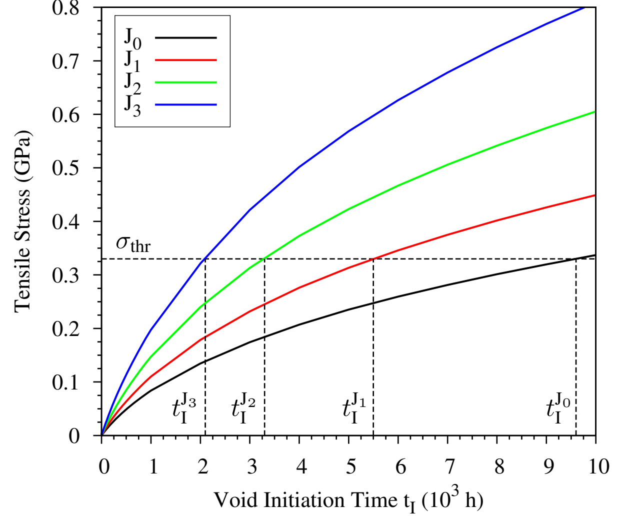

Figure 5: Time evolution of the maximum tensile stress in the analyzed structure for different applied current densities. The EM void initiation times t_{I} obtained for each curve profile are shown in the x-axis.

by coupling numerical solutions of the current density and electrical potential ψ distributions in the structure, respectively obtained from Ohm's law

$$\vec{j}(r_{\mathrm{v}}) = -\gamma_{\mathrm{E}} \nabla \psi(r_{\mathrm{v}}), \tag{9}$$

and Laplace equation

$$\nabla \cdot (\gamma_{\mathrm{E}} \nabla \psi(r_{\mathrm{v}})) = 0, \tag{10}$$

where γ_{E} is the electrical conductivity. During the void evolution phase, the resistance of the interconnect rises by following non-linear time dependence leading to an abrupt open circuit failure. Typically, the interconnect is considered failed when a resistance increase of 20% is reached. The time necessary to achieve the maximum tolerable resistance value is defined as void evolution time.

C. TTF Evaluation

The two aforementioned failure phases give important contributions to the total EM lifetime estimation of an interconnect. The EM interconnect failure time can be expressed as the sum of void initiation time t_{I} and void evolution time t_{E}

$$TTF = t_{\mathrm{I}} + t_{\mathrm{E}}. \tag{11}$$

The void initiation time is defined as the time needed to reach the threshold stress for void nucleation, while the void evolution time is related to the time elapsed until the achievement of the maximum resistance failure criterion. Normally, Black's law is used to link the EM TTF and stress conditions of temperature and current density [9] as follow

$$TTF = A j^{-n} \exp\left(\frac{E_{\mathrm{a}}}{k_{\mathrm{B}} T}\right), \tag{12}$$

where A is a constant, n is the current density exponent, and E_{a} is the vacancy activation energy. Therefore, a comparison with Black's equation provides a more precise reliability assessment by determining the most dominant mechanism in EM failure. Following this approach, we have applied the full EM physical model to the study of EM in open copper TSVs.

III. Results and Discussion

Due to the complexity of the mathematical model describing the physical phenomena presented in Section II, application of numerical simulations is necessary. Fully 3D numerical simulations are carried out by solving the model equations using FEM. TCAD studies can significantly contribute to the comprehension of EM failure mechanisms in the open copper TSV technology depicted in Figure 3. A detailed description of the geometry considered in the FEM simulations is shown in [14]. Operating conditions for EM simulations are set by imposing boundary conditions over appropriate regions of the case studied. All external surfaces of the structure are assumed to be under isothermal conditions. The outer materials surrounding the copper lines are taken to be rigid while the inner surface of the TSV (silicon nitride layer) is free to move. For the electrical loading, the left side of the copper at the TSV top is maintained at $J_0 = 1$ MA/cm^2 and the right side of the

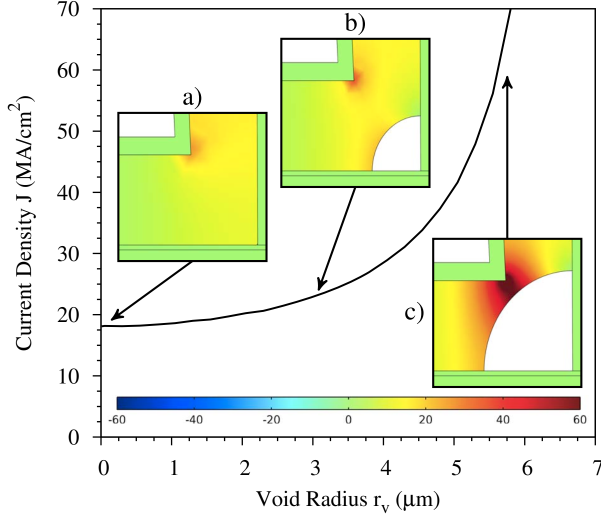

Figure 6: Current density dependence on void radius for the initial applied electrical loading J_0. The cross section views of the current density distribution are shown for three different void radii r_v: a) 10nm, b) 3μm and c) 6μm. Current crowding increases as soon as the void becomes larger.

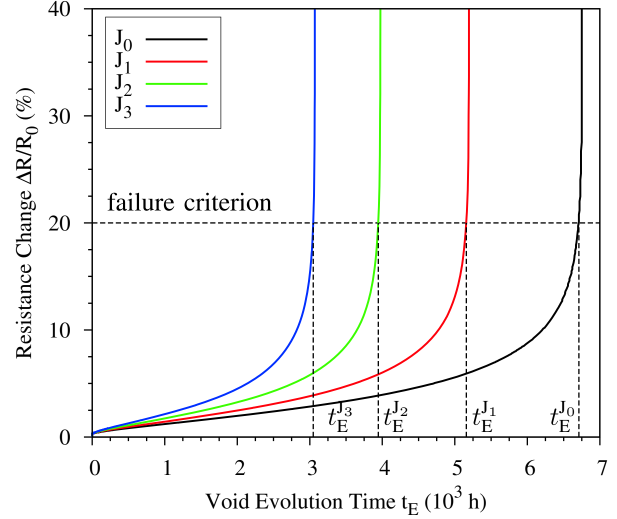

Figure 7: Interconnect resistance change as a function of time for different applied current densities. The failure criterion is 20% of resistance increase. The EM void evolution times t_E obtained for each curve profile are shown in the x-axis.

copper rerouting layer under the TSV bottom is set at ground.

As discussed before, the EM void initiation mechanism is described by the mechanical stress build-up due to EM in the case study. Figure 4 shows the mechanical stress distribution in the simulated TSV structure. A high tensile stress develops at the TSV bottom, where the TSV intersect the capping and the barrier layers. The copper line is surrounded by titanium nitride layer (barrier) at the bottom and by silicon dioxide layer (capping) at the sides. These interfaces act as blocking boundaries for the EM vacancy flux causing accumulation of vacancies at this location. Vacancy accumulation produces volume contraction of the structure resulting in the development of tensile stress at these areas. In turn, at the specular interface sides, a compressive stress is observed due to the volume expansion of the structure produced by vacancy depletion. Therefore, the Cu/TiN/SiO_2 layer intersection is identified as the location with the highest probability of void formation in the open copper TSV structure. It has been shown that this is the typical site for void nucleation in copper dual-damascene structures with TSVs mainly due to the lower cohesive energies of the surrounding layers and fabrication defects [5].

The stress distribution at such sites in the structure is monitored by increasing the current density of 30%. From the simulation results we obtain the time evolution of the stress build-up due to EM for a total of four current densities (Figure 5). As expected [10], the maximum tensile stress increases with the square root of time, until it reaches the threshold value for void initiation. By following [11], the threshold stress σ_thr calculated for the particular case study is 0.33 GPa. The EM void initiation time t_I for a given applied current density is determined as the time needed to reach the limit. For lower current density values a longer time is needed to reach the threshold stress for void nucleation than for higher current densities. Furthermore, during this time period the TSV resistance does not change. The void has been nucleated and its small size is not able to produce a significant increase of the electrical interconnect resistance.

After a void has nucleated, a rapid increase of the interconnect resistance takes place. The resistance change is associated to the growth of a void located at the Cu/TiN/SiO_2 layer intersection at the TSV bottom. The volumetric growth of the void is due to the changes in the vacancy concentration distribution in the structure driven by the electron wind force. Therefore, the growing void depends on the rate of vacancies reaching the void which is caused by current density changes around it. As soon as the void becomes larger, current density divergences are more prominent close to that area. By following the modeling approach described in Section II.B, an initial spherical void is placed at the location of void nucleation and its radius is increased (Figure 3). Figure 6 shows the current density distribution close to the void initiation location for different void sizes in the simulated structure. The electron flow leads to current crowding towards the corner between void, copper, and barrier layer even if the void radius size is small (Figure 6a). Current crowding arises especially at the TSV bottom close to the sites of void nucleation because of the different geometries and electrical conductivity values of the diverse layers [14].

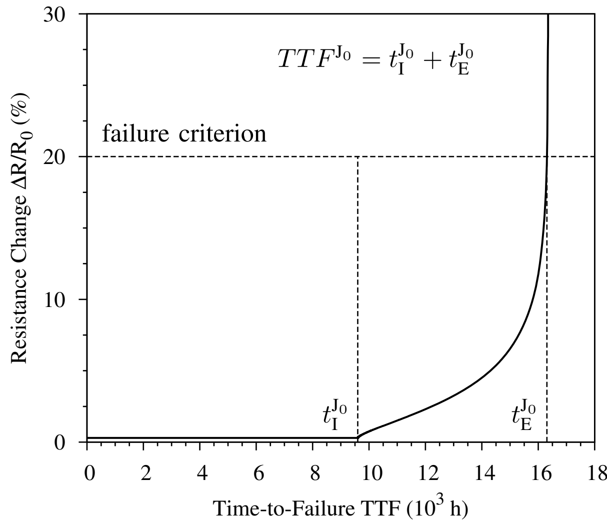

Figure 8: Complete EM resistance trace profile for the initial applied current density J_0. Two EM failure times are shown in the x-axis.

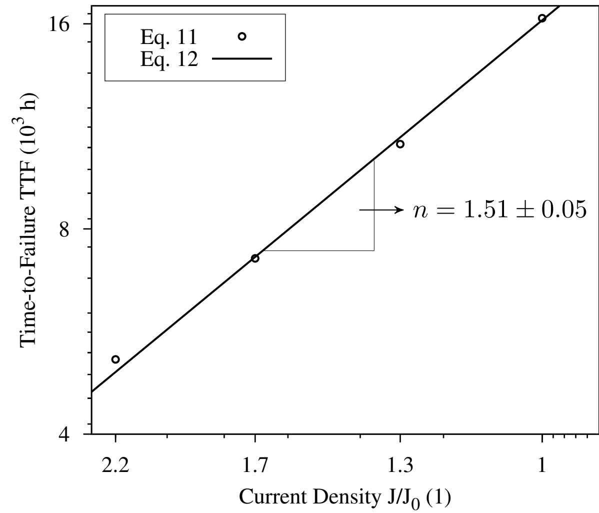

Figure 9: Time-to-failure dependence on current density. The line indicates the fitting according to Black's equation and n is its angular coefficient.

The current flow tends to fed the void with vacancies implying an increase of the void volume. The growing void causes reduction of the effective TSV conducting area at the bottom leading to higher current crowding in these regions (Figure 6b-c). The numerical simulation results of the flux of vacancies captured by the void which produce current density and vacancy concentration distributions changes around it are inserted into (7). By performing a numerical integration we are able to obtain the time necessary to grow a void of a given volume. Furthermore, numerical solutions of (9) and (10) allow to determine the interconnect resistance change during the void evolution period. In this way a relationship between the open copper TSV resistance and time for different initial electrical loadings can be shown in Figure 7. At the beginning, the resistance change with time associated with the growing void is very small. Then, a sudden non-linear resistance increase that leads to an abrupt open circuit failure is observed. After a resistance increase of 20% we normally consider the interconnect failed. The EM void evolution times t_E for different applied current densities are determined as the times needed to reach the maximum tolerable resistance level. In addition, for higher initial applied current densities a shorter time is needed to reach the resistance failure criterion than for lower current densities. Here, the resistance increase is accelerated because of the more intense EM flux induced by the higher current density.

Once both void initiation and void evolution times are determined, the EM failure time evaluation of the open copper TSV structure can be completed. By following (11), the total EM TTF can be expressed as the sum of void initiation time and void evolution time. Figure 8 shows the interconnect resistance as a function of the complete EM TTF for a given applied current density. As expected, the resistance curve is divided in two parts. The latency period is characterized by the void initiation phase. During this period the void is nucleating and is electrically undetectable. After a void has nucleated, the void evolution phase begins. The resistance of the TSV progressively rises with time. The void is growing and its size influences the electric performances of the interconnect. After the non-linear time dependence increase, an abrupt jump of the interconnect resistance is observed. At this stage, the open circuit failure due to EM is already effective and the electric current does not flow in the interconnect. The void initiation and void evolution times are of about the same order of magnitude. This highlights the importance of including both contributions in the complete EM TTF estimation of the given interconnect structure. The result is clearly in good agreement with the experimental analysis presented in [13] for a copper dual damascene TSV structure.

By fitting the TTF/current density curves to Black's equation (12), the current density exponent n is estimated. The result yields a value between 1 and 2 which confirms that both void nucleation and void evolution are important mechanisms in EM failure [9]. Therefore, the development of the EM model based on the combination of void nucleation together with the void growth mechanism well describe the EM failure analysis in open copper TSV technologies. Furthermore, the EM TTF estimation in such structures follows Black's behavior as shown in Figure 9.

IV. Conclusion

In this work we have analyzed the resistance change due to EM induced voiding in open copper TSVs in order to estimate the EM lifetime of the given BEOL interconnect. For this purpose a two-step approach based on the full EM model has been followed. Model equations have been solved by means of FEM. In the first step, the locations with the highest probability of void nucleation are identified by monitoring the stress build-up due to EM in the TSV structure. The EM void initiation time is determined as the time necessary to reach the threshold stress value for void nucleation. Then, the second step is characterized by the void evolution. An initial small void is placed at the void nucleation site and its evolution is traced including the resistance increase. An analytic model based on the void radius dependence of the incoming vacancy flux due to EM is proposed to describe the time needed to grow a void of a given volume. The interconnect resistance changes in time until it reaches the common failure criterion of 20% resistance increase. The EM void evolution time is related to the time elapsed until this value is achieved. The EM lifetime of the open copper TSV structure is given by the sum of both void initiation and void evolution times. Simulations are carried out for different current densities and fitted to Black's equation. The model based on the combination of kinetics of void nucleation and growth provides a good description of the EM TTF estimation and the results are in good agreement with Black's equation.

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